Parallel Output (642-3137-001)

Rockwell International

instructions

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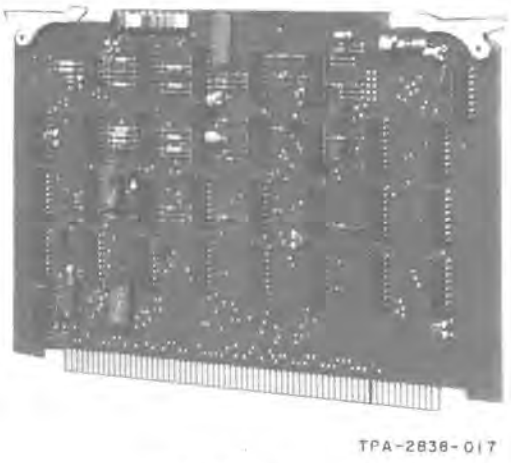
1. DESCRIPTION

Parallel Output 642-3137-001, shown in figure 1, is a 2-layer planar card with a 130-pin (2 layers, 65 pins each) edge-on connector. All test points are mounted at the top edge of the card for easy access with the card installed in the unit.

The parallel output card consists of 6 primary circuits: 16 serial-to-parallel shift registers (4 for each parallel output word), 4 power-on-clear flip-flops, a strobe multiplexer, an rf gain control, a fault indicator flasher, and an update/busy indicator/address gate (ADRG) generator.



Parallel Output
Figure 1

2. PRINCIPLES OF OPERATION (Refer to figure 2.)

2.1 General

The parallel output card receives the serial input data from the serial interface card. The shift registers convert the serial data to parallel outputs for application to front panel indicators. The rf gain control circuit is only used in the remote mode of the receiver circuits. The power-on-clear circuit initially sets all the outputs to clear. After initial turn-on, update, address gate, and busy indicator signals are continually generated for use by control unit circuits.

2.2 Power-On-Clear (Refer to figure 2 and figure 3, the schematic diagram.)

When power is applied to the parallel output card, the rc time constants of C15 and R28, and C19 and R37, generate a logic 1 voltage for approximately 1 second. These momentary logic 1's are applied to the set terminals of flip-flops U5B, U17A, U17B, and U5A. The logic 1 at the set inputs drives the $\overline{Q}$ output to a logic 0. The logic 0 is applied to the enable lines of the 16 shift register, clearing all the shift registers to an initial open-circuit condition.

2.3 Serial-to-Parallel Shift Registers

The 16 shift registers are electronically arranged in 4 groups of 4. Each group of shift registers represents one word, each shift register represents one character of the word, and each register output represents one of the eight data bits of the word. (This information is shown in detail in the table of the schematic diagram (figure 3).)

When the local enable signal at P1-16 is logic 0, the enable input to all the shift registers is logic 1 which

enables their operation. In this condition, the data input (P1-89) is applied to the character-5 register of each word group. The clock input (P1-88) clocks the data serially through each of the registers in a word group. When all 8 bits of characters 2 through 4 are loaded, a strobe signal at the register strobe inputs will cause the data to be stored in the registers. With the enable inputs at logic 1, the stored data is applied through buffers to the eight outputs of the shift registers.

Strobe signals to each of the word groups of registers are generated by multiplexer U7. Outputs from this 8-channel multiplexer are determined by the inputs to the A (STA 1) and B (STA 2) control inputs (P1-83 and -81).

2.4 Fault Indicator Flasher (Refer to figure 2 and the schematic diagram.)

Free-running astable multivibrator U8, positive edge trigger monostable multivibrator U32, and exclusive OR gate U12B develop an on-off (flash) signal to indicate a receiver-exciter fault. During normal operation, the strobe signal to the U32 retrigger input occurs at a rate that keeps the multivibrator continuously triggered. The output of U32 is connected to the external reset of U8. The output of U8 (a logic 1) is synchronized with the strobe signal and applied to exclusive OR gate U12B.

The other input to exclusive OR gate U12B is connected to either U16 or U15 using E6. When connected to U16, word 4, character 4, bit 1 (2-channel receiver/exciter fault bit) is applied to U12B. When connected to U15, word 4, character 2, bit 5(4-channel receiver/exciter fault bit) is applied to U12B.

When the receiver/exciter fault bit is logic 0 and the output from multivibrator U8 is logic 1, a fault indication (logic 1) is produced at the output of exclusive OR gate U12B-4. Since multivibrator U8 if free-running, the fault indication will be an on-off (flashing) signal. A steady fault indication is provided at connector P1-105.

In the event a malfunction interrupts monitor data transmission between the control and remote units (interconnection interruption or serial interface card malfunction, for example) the strobe signal to the U32 retrigger input goes to logic 0 allowing multivibrator U8 to free run at a 0.25-Hz rate.

2.5 RF Gain Control (Refer to figure 2 and the schematic diagram.)

The rf gain control circuits develops a dc voltage output proportional to the binary input signals to multiplexers U2 and U10. Control input signals (pins A, B, and C) to the multiplexers are obtained from serial-to-parallel shift register U18. The various dc output levels are developed by changing the input resistors to U1A.

In the remote mode of operation, the inputs to U9A and B are at logic 0. The rf gain (U18-7) signal is logic 0; this causes multiplexer U10 to be enabled and U2 to be inhibited. When the rf gain level is adjusted to the point where the rf gain signal goes to logic 1, U10 is inhibited and U2 is enabled (through inverter U11E). Thus the various input resistor values are selected to control the dc output level from amplifiers U1A and U1B.

2.6 Update/Busy Indicator/Address Gate Generator

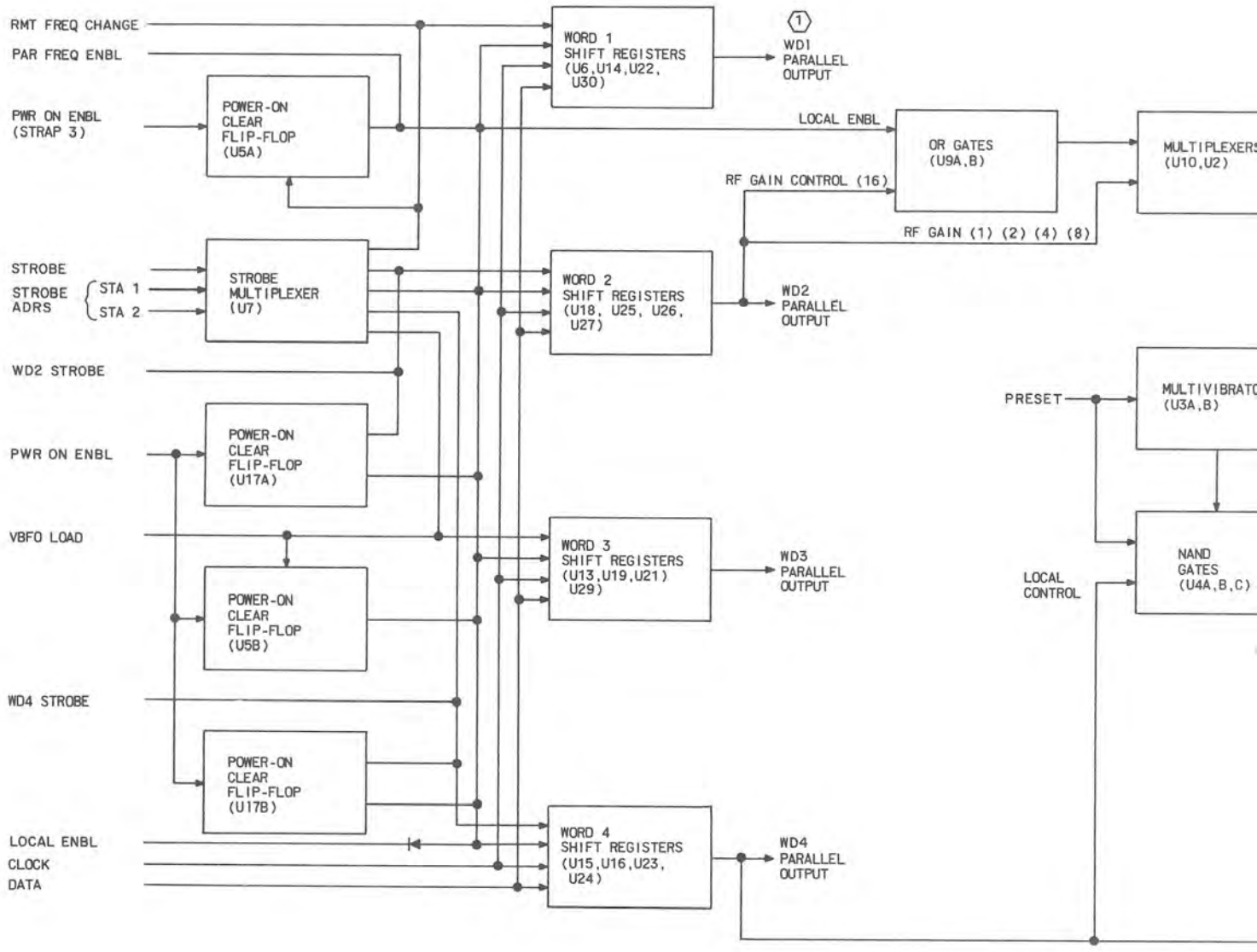
This circuit develops address gate and update pulses, and a driving voltage for the unit front-panel BUSY indicator. (These signals are used in the control unit only.)

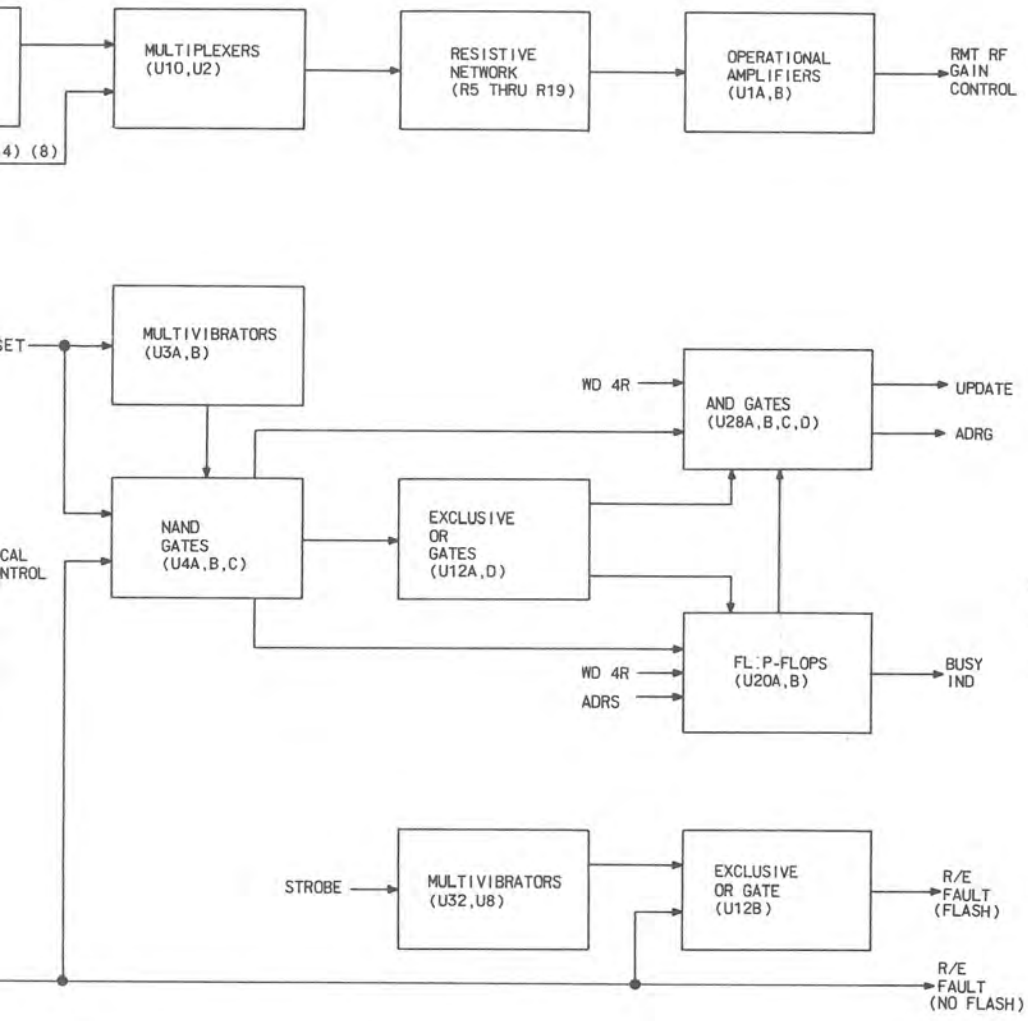
Whith the unit front-panel CONT switch in NORM and no busy signal input from the unit being controlled, the input to U4A-1 is logic 0 and the input to U4A-2 is logic 1. This develops a logic 0 from exclusive OR gate U12D and AND gate U28B preventing the BUSY indicator on the unit front panel from lighting. This same signal is clocked through U20A to inhibit U28D from gating out WD4R pulses which are used as update requests.

When a busy signal input is received in the monitor data, the input to U4A-1 goes to logic 1. This develops a logic 1 to U28A-2 and to the busy indicator output causing the BUSY indicator to light and causing an output of continuous WD4R pulses as an address gate signal. The input to U28C-8 is logic 0 keeping the update output inhibited.

When the front panel CONT switch is changed from NORM to TEST in a not-busy condition, U4A-1 is logic 0 keeping the busy indicator output at logic 0. Switching from NORM to TEST causes U12C to develop a momentary output pulse that triggers U3A, causing a logic 0 output from U4B-4. This causes the exclusive OR gate to momentarily go to logic 1 and set U20A-1 to logic 1. The momentary logic 1 at U28D-13 permits one WD4R pulse to be gated out (P1-66) as an update pulse.

With a busy signal present (U4A-1 at logic 1) when the CONT switch is placed in the TEST position, the


RMT FREQ CHANGE
PAR FREQ ENBL
PWR ON ENBL (STRAP 3)
POWER-ON CLEAR FLIP-FLOP (U5A)
WORD 1 SHIFT REGISTERS (U6,U14,U22, U30)
1
WD1 PARALLEL OUTPUT
LOCAL ENBL
OR GATES (U9A,B)
MULTIPLEXERS (U10,U2)
RF GAIN CONTROL (16)
RF GAIN (1) (2) (4) (8)
STROBE
STROBE ADRS
STA 1
STA 2
STROBE MULTIPLEXER (U7)
WORD 2 SHIFT REGISTERS (U18, U25, U26, U27)
WD2 PARALLEL OUTPUT
WD2 STROBE
PRESET
MULTIVIBRATO (U3A,B)
PWR ON ENBL
POWER-ON CLEAR FLIP-FLOP (U17A)
VBFO LOAD
WORD 3 SHIFT REGISTERS (U13,U19,U21) U29)
WD3 PARALLEL OUTPUT
LOCAL CONTROL
NAND GATES (U4A,B,C)
POWER-ON CLEAR FLIP-FLOP (U5B)
WD4 STROBE
POWER-ON CLEAR FLIP-FLOP (U17B)
LOCAL ENBL
CLOCK
DATA
WORD 4 SHIFT REGISTERS (U15,U16,U23, U24)
WD4 PARALLEL OUTPUT



NOTES:

1. REFER TO THE SCHEMATIC DIAGRAM FOR WORD FORMAT.
2. NONSTANDARD ABBREVIATIONS:
   ADRG = ADDRESS REGISTER
   R/E = RECEIVER/EXCITER

TPA-2833-014

Parallel Output, Block Diagram
Figure 2

set pulse to U20A-6 is developed as previously described; however, the resulting logic 1 from U4A-3 causes U12D-11 to be logic 0. This switches off the front-panel BUSY indicator, and causes the Q output from U20A to go to logic 0. The resulting update output is one logic 1 pulse and the ADRG output is inhibited.

When the front-panel CONT switch is changed from TEST to NORM, the logic 1 output pulse from U3B-10 is developed as previously described. With a not-busy signal present, U4A-3 is logic 1 enabling U28C to gate the WD4R pulses to U28D. The logic 1 at U12D-13 inhibits gate U28B. The logic 0 output from U28B-4 is the BUSY indicator output, the D input to U20A, and an inhibiting input to U28A. The resulting Q output from U20A inhibits gate U28D, developing a logic 0 update output.

With a busy signal present when the CONT switch is set to NORM, U4A-3 is logic 0 which causes the update output to be logic 0. The logic 1 outputs a logic 1 BUSY indicator signal and enables gate U28A. The WD4R input to U28A-1 is then gated out as continuous ADRG pulses.

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the parallel output card are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in tables 1 and 2 check the total performance of the parallel output card. The procedures in table 1 are for the following equipments:

HF-8010/8010A Exciter
HF-8050/8050A Receiver
HF-8070/8070A Receiver-Exciter
851S Receiver
HF-8090, HF-8091, HF8092, and HF-8095 Controls.

The procedures in table 2 are for the following equipments:

HF-8014/8014A Exciter
HF-8054/8054A Receiver
HF-8093 and HF-8094 Controls.

These procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic diagram (figure 3) to trace the source of the fault.

Table 1. Parallel Output, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	*Note* The testing and troubleshooting procedures herein are for 1- or 2-channel configurations of the HF-8010/8010A, HF-8050/8050A, HF-8070/8070A, 851S, HF-8090, HF-8091, HF-8092, and HF-8095. These testing and troubleshooting procedures are based on using a control unit and an associated local unit. The most effective method of testing and troubleshooting is obtained by installing the questionable parallel output in the control unit. During these tests when a control unit is referred to it is a receiver-exciter control, or a receiver control. When a local unit is referred to it is a receiver-exciter, an exciter, or a receiver.		

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. (Cont)	a. Remove top cover of unit containing the parallel output that is to be tested. b. Remove parallel output. Strap pin pair E6 between middle and right pins. Install it on an extender card and place it in the control unit. c. Set control unit and local unit LINE SELECTOR switches to 115 V. d. Connect control unit and local unit to 115-V ac power source and set power on. e. Measure dc voltages, on the card under test, between the following pins and ground (TP1, brown): P1-45 P1-65 P1-114 f. Strap local unit for address 0. g. Connect local unit to control unit.	 +15 ±1.0 V dc. +5 ±0.5 V dc. -15 ±1.0 V dc.	 Check associated power supply.
2. Data inputs, word 1 (Cont)	a. Set control unit CONT switch to TEST. *Note* Word 1 tests can also be accomplished with the control unit CONT switch in NORM and local unit CONT switch in LCL. Then set local unit controls to positions indicated. b. Set control unit FREQUENCY KHZ controls for 29 999.9(9).	 Frequency display reads 29 999.9(9). Refer to chart for logic levels and associated parallel output pin numbers.	 Measure logic levels as indicated in chart.

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	c. Set control unit FREQUENCY KHZ controls for 16 666.6(6).	Frequency display reads 16 666.6(6). Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	d. Set control unit FREQUENCY KHZ controls for 02 000.0(0).	Frequency display reads 02 000.0(0). Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	Note Logic 1 = NLT +3.0 V dc. Logic 0 = NMT 0.5 V dc.		

BCD OUTPUT SIGNAL	PARALLEL OUTPUT PIN NO P1-( )	LOGIC LEVELS 29 999.9(9)	16 666.6(6)	02 000.0(0)	IF ABNORMAL CHECK
10 MHz (2)	129	1	0	0	U6, U5, U7, U11, and associated circuits.
10 MHz (1)	64	0	1	0	
1 MHz (8)	128	1	0	0	
1 MHz (4)	63	0	1	0	
1 MHz (2)	127	0	1	1	
1 MHz (1)	62	1	0	0	
100 kHz (8)	126	1	0	0	U14, U5, U7, U11, and associated circuits.
100 kHz (4)	61	0	1	0	
100 kHz (2)	125	0	1	0	
100 kHz (1)	60	1	0	0	
10 kHz (8)	124	1	0	0	
10 kHz (4)	59	0	1	0	
10 kHz (2)	123	0	1	0	
10 kHz (1)	58	1	0	0	

(Cont)

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)			

BCD OUTPUT SIGNAL		PARALLEL OUTPUT PIN NO P1-( )	LOGIC LEVELS 29 999.9(9)	16 666.6(6)	02 000.0(0)	IF ABNORMAL CHECK
1 kHz	(8)	122	1	0	0	U22, U5, U7, U11, and associated circuits.
	(4)	57	0	1	0	
	(2)	121	0	1	0	
	(1)	56	1	0	0	
100 Hz	(8)	120	1	0	0	
	(4)	55	0	1	0	
	(2)	119	0	1	0	
	(1)	54	1	0	0	
10 Hz (with no 10-Hz tuning)	(8)	118	0	0	0	U30, U5, U7, U11, and associated circuits.
	(4)	53	0	0	0	
	(2)	117	0	0	0	
	(1)	52	0	0	0	
10 Hz (with 10-Hz tuning)	(8)	118	1	0	0	
	(4)	53	0	1	0	
	(2)	117	0	1	0	
	(1)	52	1	0	0	
1 Hz (with no 1-Hz tuning)	(8)	116	0	0	0	U30, U5, U7, U11, and associated circuits.
	(4)	51	0	0	0	
	(2)	115	0	0	0	
	(1)	50	0	0	0	
1 Hz (with 1-Hz tuning)	(8)	116	1	0	0	
	(4)	51	0	1	0	
	(2)	115	0	1	0	
	(1)	50	1	0	0	

Note

If a processor control is used, the 1-Hz outputs can be checked in the same manner that the other frequency outputs are checked.

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. Data inputs, word 2 (Cont)	a. Set control unit CONT switch to TEST. *Note* Word 2 tests can also be accomplished with the control unit CONT switch in NORM and local unit CONT switch in REM. Then measure voltages at local unit or control unit parallel output card (the card being tested). Rf gain test, steps b and c, is applicable to receiver and receiver-exciter controls only. b. Set control unit RF GAIN control to MAX. c. Connect a dvm to TP5 (green).	Note dc levels as shown in chart for different RF GAIN positions.	Check U18, U9, U11, U1, and associated circuits. Check also circuit indicated in chart.

RF GAIN CONTROL SETTINGS		TP5 (DC VOLTS)	IF ABNORMAL CHECK
MAX	1	0.000 ±0.010	None
↓	*	-0.158 ±0.010	R20
	2	-0.316 ±0.010	R19
	*	-0.475 ±0.020	R19, R20
	3	-0.634 ±0.020	R18
	*	-0.792 ±0.030	R18, R20
rotated	4	-0.950 ±0.030	R17
from MAX	*	-1.108 ±0.040	R17, R20
ccw toward	5	-1.266 ±0.040	R16
MIN	*	-1.417 ±0.050	R16, R20
↓	6	-1.568 ±0.050	R15
	*	-1.712 ±0.060	R15, R20
	7	-1.855 ±0.060	R14
	*	-2.022 ±0.070	R14, R20
	8	-2.188 ±0.070	R13
MIN	*	-2.332 ±0.080	R13, R20

(IF ABNORMAL CHECK: and U10.)

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL

3. (Cont)

RF GAIN CONTROL SETTINGS		TP5 (DC VOLTS)	IF ABNORMAL CHECK
MAX	9	-2.465 ±0.080	R12
↓	*	-2.619 ±0.090	R12, R20
	10	-2.773 ±0.090	R11
	*	-3.002 ±0.100	R11, R20
	11	-3.130 ±0.100	R10
	*	-3.283 ±0.110	R10, R20
rotated	12	-3.439 ±0.110	R9
from MAX	*	-3.570 ±0.120	R9, R20
ccw toward	13	-3.700 ±0.120	R8
MIN	*	-3.886 ±0.130	R8, R20
↓	14	-4.072 ±0.130	R7
	*	-4.218 ±0.140	R7, R20
	15	-4.363 ±0.140	R6
	*	-4.532 ±0.150	R6, R20
↓	16	-4.700 ±0.150	R5
MIN	*	-4.858 ±0.160	R5, R20

and U2.

*Controlled by least significant bcd input for rf gain control, available only on processor controls. Bcd for least significant bcd signal at MAX setting is bit wt 0. Bcd signal for most significant bcd signal at one step beyond MIN setting is bit wt 31.

Note

AGC tests, steps d through f, are applicable to the receiver and receiver-exciter controls only.

d. Set control unit AGC switch to FAST. — Check logic levels at the associated parallel output pin numbers as shown in chart.

e. Set control unit AGC switch to OFF. — Check logic levels at the associated parallel output pin numbers as shown in chart.

f. Set control unit AGC switch to SLOW. — Check logic levels at the associated parallel output pin numbers as shown in chart.

(Cont)

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>3. (Cont)</td><td>
Note
Logic 1 = NLT +3.0 V dc.
Logic 0 = NMT 0.5 V dc.
<table>
<tr><th rowspan="2">PARALLEL OUTPUT</th><th rowspan="2">PIN NO P1-( )</th><th colspan="3">AGC SWITCH POSITION</th><th rowspan="2">IF ABNORMAL CHECK</th></tr>
<tr><th>FAST</th><th>OFF</th><th>SLOW</th></tr>
<tr><td>CH A AGC OFF</td><td>84</td><td>0</td><td>1</td><td>0</td><td rowspan="4">U26, U17, U7, U11, and associated circuits.</td></tr>
<tr><td>CH A AGC FAST</td><td>85</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>CH B AGC OFF</td><td>19</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>CH B AGC FAST</td><td>20</td><td>1</td><td>0</td><td>0</td></tr>
</table>
Note
Bandwidth tests, steps g and h, are applicable to the receiver control only.
g. Set control unit MODE switch to SSB/CW.
h. Set control unit BANDWIDTH switch to each of its positions.
</td><td>The display associated with the BANDWIDTH switch positions lights. Refer to chart for logic levels and associated parallel output pin numbers.</td><td>Measure logic levels as indicated in chart.</td></tr>
<tr><td>(Cont)</td><td>
Note
Logic 1 = NLT +3.0 V dc.
Logic 0 = NMT 0.5 V dc.
</td><td></td><td></td></tr>
</table>

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL

3. (Cont)

PARALLEL OUTPUT	PIN NO P1-( )	BANDWIDTH SWITCH POSITION								IF ABNORMAL CHECK
		16	A	B	USB	LSB	C	D	E	
FL8	100	1	0	0	0	0	0	0	0	U27, U17, U7, U11, and associated circuits.
FL3	33	0	1	0	0	0	0	0	0	
FL4	98	0	0	1	0	0	0	0	0	
FL1	32	0	0	0	1	0	0	0	0	
FL2	97	0	0	0	0	1	0	0	0	
FL5	34	0	0	0	0	0	1	0	0	
FL6	35	0	0	0	0	0	0	1	0	
FL7	99	0	0	0	0	0	0	0	1	

Note

Mode tests, step i, are applicable to the receiver control only.

i. Set MODE switch (receiver control only) to each of its positions.

The display associated with the MODE switch position lights. Refer to chart for logic levels and associated parallel output pin numbers.

Measure logic levels as indicated in chart.

Note

Logic 1 = NLT +3.0 V dc.
Logic 0 = NMT 0.5 V dc.

(Cont)

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)			

PARALLEL OUTPUT	PIN NO P1-( )	MODE SWITCH POSITION			IF ABNORMAL CHECK
		*SSB/CW	*AM	ISB	
SSB EN	72	1	0	1	U25, U17, U7, U11, and associated circuits.
AM EN	8	0	1	0	
FM EN	73	0	0	0	
CW EN	9	0	0	0	
ISB EN	74	0	0	1	

*In these positions the display and logic levels associated with the BANDWIDTH switch position are also activated.

Note

Mode tests, step j, are applicable to the exciter and receiver-exciter controls only.

j. Set MODE switch (exciter and receiver-exciter controls only) to each of its positions.

The display associated with the MODE switch position lights. Refer to chart for logic levels and associated parallel output pin numbers.

Note

Logic 1 = NLT +3.0 V dc.
Logic 0 = NMT 0.5 V dc.

(Cont)

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>3. (Cont)</td><td colspan="3">
<table>
<tr><th rowspan="2">PARALLEL OUTPUT</th><th rowspan="2">PIN NO P1-( )</th><th colspan="5">MODE SWITCH POSITION</th><th rowspan="2">IF ABNORMAL CHECK</th></tr>
<tr><th>CW</th><th>LSB</th><th>USB</th><th>AM</th><th>ISB</th></tr>
<tr><td>SSB EN</td><td>72</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td rowspan="5">U25, U17, U7, U11, and associated circuits.</td></tr>
<tr><td>AM EN</td><td>8</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>FM EN</td><td>73</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>CW EN</td><td>9</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>ISB EN</td><td>74</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>FL1 (USB) EN</td><td>32</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="2">U27, U17, U7, U11, and associated circuits.</td></tr>
<tr><td>FL2 (LSB) EN</td><td>97</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>4. Data inputs, word 3

(Cont)</td><td>a. Set control unit CONT switch to TEST.

Note

Word 3 tests can also be accomplished with control unit CONT switch in NORM and local unit CONT switch in REM. Then measure voltages at local unit parallel output card (the card being tested).

Pa tests, steps b through e, are applicable to the exciter and receiver-exciter controls only.

b. Set control unit PA PWR switch to OFF.

c. Set control unit PA PWR switch to STBY.

d. Set control unit PA PWR switch to HIGH PWR.</td><td>Check logic levels at the associated parallel output pin numbers as shown in chart.

Check logic levels at the associated parallel output pin numbers as shown in chart.

Check logic levels at the associated parallel output pin numbers as shown in chart.</td><td></td></tr>
</table>

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>4. (Cont)</td><td>e. Set control unit PA PWR switch to LOW PWR.

Note

Logic 1 = NLT +3.0 V dc.
Logic 0 = NMT 0.5 V dc.</td><td>Check logic levels at the associated parallel output pin numbers as shown in chart.</td><td></td></tr>
<tr><td></td><td>
<table>
<tr><th rowspan="2">PARALLEL OUTPUT</th><th rowspan="2">PIN NO P1-( )</th><th colspan="4">PA PWR SWITCH POSITION</th><th rowspan="2">IF ABNORMAL CHECK</th></tr>
<tr><th>OFF</th><th>STBY</th><th>HIGH PWR</th><th>LOW PWR</th></tr>
<tr><td>PA LV EN</td><td>79</td><td>0</td><td>1</td><td>1</td><td>1</td><td rowspan="3">U19, U5, U7, U11, and associated circuits.</td></tr>
<tr><td>PA HV EN</td><td>14</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>LO PWR EN</td><td>78</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
</table>
</td><td></td><td></td></tr>
<tr><td></td><td>Note

Pilot carrier tests, steps f and g, are applicable to the exciter and receiver-exciter controls only.

f. Set control unit P CAR switch to OFF.

g. Set control unit P CAR switch to ON.</td><td>Logic level 0 at P1-82 (NMT 0.5 V dc).

Logic level 1 at P1-82 (NLT +3.0 V dc).</td><td>Check U19, U5, U7, U11, and associated circuits.</td></tr>
<tr><td>(Cont)</td><td>Note

Dvbfo tests, steps h through k, are applicable only to the receiver and receiver-exciter controls with a dvbfo option installed.

h. Set the control unit MODE switch to SSB/CW or CW and BFO switch to VAR.</td><td></td><td></td></tr>
</table>

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	i. Set digital VBFO controls for +9990 Hz.	VBFO frequency display reads +9990. Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	j. Set digital VBFO controls for -6660 Hz.	VBFO frequency display reads -6660. Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	k. Set digital VBFO controls for +1000 Hz.	VBFO frequency display reads +1000. Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	Note Logic 1 = NLT +3.0 V dc. Logic 0 = NMT 0.5 V dc.		
(Cont)			

BCD OUTPUT SIGNAL		PARALLEL OUTPUT PIN NO P1-( )	LOGIC LEVELS +9990	LOGIC LEVELS -6660	LOGIC LEVELS +1000	IF ABNORMAL CHECK
DVBFO 1 kHz	(8)	48	1	0	0	U29, U5, U7, U11, and associated circuits.
	(4)	113	0	1	0	
	(2)	47	0	1	0	
	(1)	112	1	0	1	
DVBFO 100 Hz	(8)	46	1	0	0	U21, U5, U7, U11, and associated circuits.
	(4)	111	0	1	0	
	(2)	110	0	1	0	
	(1)	44	1	0	0	
DVBFO 10 Hz	(8)	109	1	0	0	
	(4)	43	0	1	0	
	(2)	108	0	1	0	
	(1)	42	1	0	0	
DVBFO SIGN		107	1	0	1	U29, U5, U7, U11, and associated circuits.

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	***Note*** Analog vbfo tests, steps l and m, are applicable only to the receiver and receiver-exciter controls with an analog vbfo option installed. l. Set the control unit MODE switch to SSB/CW or CW and BFO switch to VAR. m. Rotate the BFO control through its complete range.	Check logic levels at the associated parallel output pin numbers as shown in chart.	

BCD OUTPUT SIGNAL		LOGIC LEVELS — PARALLEL OUTPUT PIN NO P1-( ) 48	113	47	112	LOGIC DISPLAY	IF ABNORMAL CHECK
- (Full ccw)	1	1	1	1	1		U29, U5, U7, U11, and associated circuits.
	2	1	1	1	0		
	3	1	1	0	1		
	4	1	1	0	0		
	5	1	0	1	1		
	6	1	0	1	0		
	7	1	0	0	1		
Rotated from - cw toward +	8	1	0	0	0		
	9	0	1	1	1		
	10	0	1	1	0		
	11	0	1	0	1		
	12	0	1	0	0		
	13	0	0	1	1		
	14	0	0	1	0		
	15	0	0	0	1		
+ (Full cw)	16	0	0	0	0		

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. Data inputs, word 4	a. Set control unit CONT switch to NORM.		
	b. Set local unit CONT switch to LCL.		
	Note		
	System key test, steps c and d, is applicable only to exciter and receiver-exciter controls.		
	c. Set local unit KEY switch to LOCK.	Control unit KEY display lights. Logic level 1 at P1-68 (NLT +3.0 V dc).	Check U15, U17, U7, U11, and associated circuits.
	d. Set local unit KEY switch to NORM.	Control unit KEY display goes out. Logic level 0 at P1-68 (NMT 0.5 V dc).	
	e. Set local unit PWR switch off and back on.	Control unit EXCTR FAULT, RCV FAULT, or R/E FAULT lights. Logic level 1 at P1-12 (NLT +3.0 V dc).	Check U16, U12, U32, U8, U17, U7, U11, and associated circuits.
	f. Change any frequency control on local unit front panel.	Control unit EXCTR FAULT, RCV FAULT, or R/E FAULT goes out. Logic level 0 at P1-12 (NMT 0.5 V dc).	
	Note		
	Receive overload test, steps g and h, is applicable only to receiver and receiver-exciter controls.		
	g. Connect +5 V dc to local unit J16-27.	Control unit RCV OVERLOAD lights. Logic level 1 at P1-67 (NLT +3.0 V dc)	Check U16, U17, U7, U11, and associated circuits.
	h. Remove +5 V dc from local unit J16-27.	Control unit RCV OVERLOAD goes out. Logic level 0 at P1-67 (NMT 0.5 V dc).	Same as step g.
	Note		
(Cont)	Coupler fault test, steps i and j, is applicable only to exciter and receiver-exciter controls.		

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	i. Connect +5 V dc to local unit J15-1.	Control unit COUPLER FAULT lights. Logic level 1 at P1-13 (NLT +3.0 V dc).	
	j. Remove +5 V dc from local unit J15-1.	Control unit COUPLER FAULT lights. Logic level 0 at P1-13 (NMT 0.5 V dc).	
	Note Rf out test, steps k and l, is applicable only to exciter and receiver-exciter controls.		
	k. Connect ground signal to local unit J15-5.	Control unit RF OUT lights. Logic level 1 at P1-5 (NLT +3.0 V dc).	
	l. Remove ground signal from local unit J15-5.	Control unit RF OUT goes out. Logic level 0 at P1-5 (NMT 0.5 V dc).	Same as step g.
	Note Pa fault test, steps m and n, is applicable only to exciter and receiver-exciter controls.		
	m. Connect +5 V dc to local unit J15-3.	Control unit PA FAULT lights. Logic level 1 at P1-77 (NLT +3.0 V dc).	
	n. Remove +5 V dc from local unit J15-3.	Control unit PA FAULT goes out. Logic level 0 at P1-77 (NMT 0.5 V dc).	
	Note Pa ready test, steps o and p, is applicable only to exciter and receiver-exciter controls.		
(Cont)	o. Connect ground signal to local unit J15-21.	Control unit PA READY lights. Logic level 0 at P1-69 (NMT 0.5 V dc).	

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	p. Remove ground signal from local unit J15-21.	Control unit PA READY goes out. Logic level 0 at P1-69 (NMT 0.5 V dc).	Same as step g.
	q. Press and hold local unit CONT switch to MON.	Logic level 1 at P1-30 (NLT +3.0 V dc).	Check U24, U17, U7, U11, and associated circuits.
	r. Set local unit CONT switch to REM.	Logic level 0 at P1-30 (NMT 0.5 V dc).	
	s. Set local unit CONT switch to LCL.	Logic level 1 at P1-95 (NLT +3.0 V dc).	
		Control unit BUSY indicator lights. Logic level 1 at P1-7 (NLT +3.0 V dc).	Check U28, U20, U12, U4, U24, U17, U7, U11, and associated circuits.
	t. Set local unit CONT switch to REM.	After short delay logic level 0 at P1-95 (NMT 0.5 V dc).	Same as step s.
		After short delay control unit BUSY indicator goes out. Logic level 0 at P1-7 (NMT 0.5 V dc).	
	u. Set local unit CONT switch to LCL.		
	v. Apply a ground to local unit A13U51A-6.		
	w. Apply a ground to local unit A13U51A-3.		
	x. Remove ground from local unit A13U51A-3.		
	y. Apply ground to local unit A13U16A-1, 2, 8.		
	z. Remove ground from local unit A13U16A-1, 2, 8.	Logic level 1 at P1-29 (NLT +3.0 V dc).	Same as step q.
	aa. Remove ground from local unit A13U51A-6.		
(Cont)	ab. Apply ground to local unit A13U42A-3.	Logic level 0 at P1-29 (NMT 0.5 V dc).	

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	ac. Remove ground from local unit A13U42A-3.		
	ad. Apply +5 V dc to local unit J16-8.	Control unit PRESEL FAULT lights. Logic level 1 at P1-28 (NLT +3.0 V dc).	Same as step q.
	ae. Remove +5 V dc from local unit J16-8.	Control unit PRESEL FAULT goes out. Logic level 0 at P1-28 (NMT 0.5 V dc).	

Table 2. Parallel Output, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	**Note** The testing and troubleshooting procedures herein are for 1-, 2-, 3-, and 4-channel configurations of the HF-8014/8014A, HF-8054/8054A, HF-8093, and HF-8094 These testing and troubleshooting procedures are based on using a control unit and an associated local unit. The most effective method of testing and troubleshooting is obtained by installing the questionable parallel output in the control unit. During these tests when a control unit is referred to it is an exciter control, or a receiver control. When a local unit is referred to it is an exciter, or a receiver.		
	a. Remove top cover of unit containing the parallel output that is to be tested.		
	b. Remove parallel output. Strap pin pair E6 between middle and left pins. Install it on an extender card and place it in the control unit.		
	c. Set control unit and local unit LINE SELECTOR switches to 115 V.		
	d. Connect control unit and local unit to 115-V ac power source and set power on.		
	e. Measure dc voltages, on the card under test, between the following pins and ground (TP1, brown):		
	P1-45 P1-65 P1-114	+15 ±1.0 V dc. +5 ±0.5 V dc. -15 ±1.0 V dc.	Check associated power supply.
	f. Strap local unit for address 0.		
	g. Connect local unit to control unit.		
2. Data inputs, word 1	a. Set control unit CONT switch to TEST.		
	Note Word 1 tests can also be accomplished with the control unit CONT switch in NORM and local unit CONT switch in LCL. Then set local unit controls to positions indicated.		
	b. Set control unit FREQUENCY KHZ controls for 29 999.9(9).	Frequency display reads 29 999.9(9). Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
(Cont)			

Table 2. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	c. Set control unit FREQUENCY KHZ controls for 16 666.6(6).	Frequency display reads 16 666.6(6). Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	d. Set control unit FREQUENCY KHZ controls for 02 000.0(0).	Frequency display reads 02 000.0(0). Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	Note Logic 1 = NLT +3.0 V dc. Logic 0 = NMT 0.5 V dc.		

BCD OUTPUT SIGNAL		PARALLEL OUTPUT PIN NO P1-( )	LOGIC LEVELS 29 999.9(9)	16 666.6(6)	02 000.0(0)	IF ABNORMAL CHECK
10 MHz	(2)	129	1	0	0	U6, U5, U7, U11, and associated circuits.
	(1)	64	0	1	0	
1 MHz	(8)	128	1	0	0	
	(4)	63	0	1	0	
	(2)	127	0	1	1	
	(1)	62	1	0	0	
100 kHz	(8)	126	1	0	0	U14, U5, U7, U11, and associated circuits.
	(4)	61	0	1	0	
	(2)	125	0	1	0	
	(1)	60	1	0	0	
10 kHz	(8)	124	1	0	0	
	(4)	59	0	1	0	
	(2)	123	0	1	0	
	(1)	58	1	0	0	

(Cont)

Table 2. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)			

BCD OUTPUT SIGNAL		PARALLEL OUTPUT PIN NO P1-( )	LOGIC LEVELS 29 999.9(9)	16 666.6(6)	02 000.0(0)	IF ABNORMAL CHECK
1 kHz	(8)	122	1	0	0	U22, U5, U7, U11, and associated circuits.
	(4)	57	0	1	0	
	(2)	121	0	1	0	
	(1)	56	1	0	0	
100 Hz	(8)	120	1	0	0	
	(4)	55	0	1	0	
	(2)	119	0	1	0	
	(1)	54	1	0	0	
10 Hz (with no 10-Hz tuning)	(8)	118	0	0	0	U30, U5, U7, U11, and associated circuits.
	(4)	53	0	0	0	
	(2)	117	0	0	0	
	(1)	52	0	0	0	
10 Hz (with 10-Hz tuning)	(8)	118	1	0	0	
	(4)	53	0	1	0	
	(2)	117	0	1	0	
	(1)	52	1	0	0	
1 Hz (with no 1-Hz tuning)	(8)	116	0	0	0	U30, U5, U7, U11, and associated circuits.
	(4)	51	0	0	0	
	(2)	115	0	0	0	
	(1)	50	0	0	0	
1 Hz (with 1-Hz tuning)	(8)	116	1	0	0	
	(4)	51	0	1	0	
	(2)	115	0	1	0	
	(1)	50	1	0	0	

Note

If a processor control is used, the 1-Hz outputs can be checked in the same manner that the other frequency outputs are checked.

Table 2. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. Data inputs, word 2 (Cont)	a. Set control unit CONT switch to TEST. *Note* Word 2 tests can also be accomplished with the control unit CONT switch in NORM and local unit CONT switch in REM. Then measure voltages at local unit or control unit parallel output card (the card being tested). Rf gain test, steps b and c, is applicable to receiver controls only. b. Set control unit RF GAIN control to MAX. c. Connect a dvm to TP5 (green).	Note dc levels as shown in chart for different RF GAIN positions.	Check U18, U9, U11, U1, and associated circuits. Check also circuit indicated in chart.

RF GAIN CONTROL SETTINGS		TP5 (DC VOLTS)	IF ABNORMAL CHECK
MAX	1	0.000 ±0.010	None
↓	*	-0.158 ±0.010	R20
	2	-0.316 ±0.010	R19
	*	-0.475 ±0.020	R19, R20
	3	-0.634 ±0.020	R18
	*	-0.792 ±0.030	R18, R20
rotated	4	-0.950 ±0.030	R17
from MAX	*	-1.108 ±0.040	R17, R20
ccw toward	5	-1.266 ±0.040	R16
MIN	*	-1.417 ±0.050	R16, R20
↓	6	-1.568 ±0.050	R15
	*	-1.712 ±0.060	R15, R20
	7	-1.855 ±0.060	R14
	*	-2.022 ±0.070	R14, R20
	8	-2.188 ±0.070	R13
MIN	*	-2.332 ±0.080	R13, R20

(IF ABNORMAL CHECK: "and U10." applies to all rows.)

Table 2. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)			

RF GAIN CONTROL SETTINGS		TP5 (DC VOLTS)	IF ABNORMAL CHECK
MAX	9	-2.465 ±0.080	R12
↓	*	-2.619 ±0.090	R12, R20
	10	-2.773 ±0.090	R11
	*	-3.002 ±0.100	R11, R20
	11	-3.130 ±0.100	R10
	*	-3.283 ±0.110	R10, R20
rotated	12	-3.439 ±0.110	R9
from MAX	*	-3.570 ±0.120	R9, R20
ccw toward	13	-3.700 ±0.120	R8
MIN	*	-3.886 ±0.130	R8, R20
↓	14	-4.072 ±0.130	R7
	*	-4.218 ±0.140	R7, R20
	15	-4.363 ±0.140	R6
	*	-4.532 ±0.150	R6, R20
↓	16	-4.700 ±0.150	R5
MIN	*	-4.858 ±0.160	R5, R20

and U2.

*Controlled by least significant bcd input for rf gain control, available only on processor controls. Bcd for least significant bcd signal at MAX setting is bit wt 0. Bcd signal for most significant bcd signal at one step beyond MIN setting is bit wt 31.

Note

AGC tests, steps d through f, are applicable to the receiver controls only.

d. Set channel A1 AGC BUS switch to ON.	Check logic levels at the associated parallel output pin numbers as shown in chart.	
e. Rotate channel A1 AGC control switch through all its positions.	Check logic levels at the associated parallel output pin numbers as shown in chart.	
f. Repeat steps d and e for channels A2, B1, and B2.	Check logic levels at the associated parallel output pin numbers as shown in chart.	

(Cont)

Table 2. Parallel Output, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>3. (Cont)</td><td>

Note

Logic 1 = NLT +3.0 V dc.
Logic 0 = NMT 0.5 V dc.

<table>
<tr><th rowspan="2">PARALLEL OUTPUT</th><th rowspan="2">PIN NO P1-( )</th><th colspan="4">AGC SWITCH POSITION</th><th rowspan="2">IF ABNORMAL CHECK</th></tr>
<tr><th>OFF</th><th>FAST</th><th>MEDIUM</th><th>SLOW</th></tr>
<tr><td>CH A1 AGC 1</td><td>32</td><td>1</td><td>0</td><td>0</td><td>1</td><td rowspan="8">Check U26,U27, &17, U7, U11, and associated circuits.</td></tr>
<tr><td>CH A1 AGC 2</td><td>97</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>CH A2 AGC 1</td><td>20</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>CH A2 AGC 2</td><td>19</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>CH B1 AGC 1</td><td>33</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>CH B1 AGC 2</td><td>98</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>CH B2 AGC 1</td><td>85</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>CH B2 AGC 2</td><td>84</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
</table>

Note

Bandwidth tests, steps g and h, are applicable to the receiver control only.

g. Set control unit MODE switch to SSB/CW.

h. Set control unit BANDWIDTH switch to each of its positions.

Note

Logic 1 = NLT +3.0 V dc.
Logic 0 = NMT 0.5 V dc.

(Cont)</td><td>The display associated with the BANDWIDTH switch positions lights. Refer to chart for logic levels and associated parallel output pin numbers.</td><td>Measure logic levels as indicated in chart.</td></tr>
</table>

Table 2. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL

3. (Cont)

PARALLEL OUTPUT	PIN NO P1-( )	BANDWIDTH SWITCH POSITION								IF ABNORMAL CHECK
		16	A	B			C	D	E	
										U26, U27, U17, U7, U11, and associated circuits.
FL3	100	0	1	0			0	0	0	
FL4	37	0	0	1			0	0	0	
FL1	99	1	0	0			0	0	0	
FL5	106	0	0	0			1	0	0	
FL6	41	0	0	0			0	1	0	
FL7	3	0	0	0			0	0	1	

Note

Mode tests, step i, are applicable to the receiver control only.

i. Set MODE switch (receiver control only) to each of its positions.

The display associated with the MODE switch position lights. Refer to chart for logic levels and associated parallel output pin numbers.

Measure logic levels as indicated in chart.

PARALLEL OUTPUT	PIN NO P1-( )	MODE SWITCH POSITION				IF ABNORMAL CHECK
		NET DATA	*CW	*AM	ISB	
AM EN	8	0	0	1	0	U25, U17, U7, U11, and associated circuits.
DATA NET EN	73	1	0	0	0	
CW EN	72	0	1	0	0	
ISB EN	9	0	0	0	1	

*In these positions the display and logic levels associated with the BANDWIDTH switch position are also activated.

Note

Mode tests, step j, are applicable to the exciter controls only.

j. Set MODE switch (exciter controls only) to each of its positions.

The display associated with the MODE switch position lights. Refer to chart for logic levels and

(Cont)

Table 2. Parallel Output, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>3. (Cont)</td><td>j. (Cont)

Note

Logic 1 = NLT +3.0 V dc.
Logic 0 = NMT 0.5 V dc.

Note

Channel select tests, steps k through m, are applicable to receiver control only.

k. Place MODE switch in the ISB position.

l. Place CH B2 switch to ON position.

m. Repeat step l for CH B1, CH A1, and CH A2 switches.</td><td>associated parallel output pin numbers.

The display associated with the CH B2 ON position lights. Refer to chart for logic levels and associated parallel output pin numbers.</td><td></td></tr>
<tr><td></td><td>
<table>
<tr><th rowspan="2">PARALLEL OUTPUT</th><th rowspan="2">PIN NO P1-( )</th><th colspan="2">CH SWITCH POSITION</th><th rowspan="2">IF ABNORMAL CHECK</th></tr>
<tr><th>ON</th><th>OFF</th></tr>
<tr><td>A2 ENBL</td><td>17</td><td>1</td><td>0</td><td rowspan="4">Check U25, U17, U7, U11, and associated circuits.</td></tr>
<tr><td>A1 ENBL</td><td>26</td><td>1</td><td>0</td></tr>
<tr><td>B1 ENBL</td><td>6</td><td>1</td><td>0</td></tr>
<tr><td>B2 ENBL</td><td>74</td><td>1</td><td>0</td></tr>
</table>
</td><td></td><td></td></tr>
<tr><td></td><td>Note

Channel select tests, steps n through p, are applicable to exciter control only.

n. Place MODE switch in ISB position.

o. Place channel A1 CHANNEL ENABLE switch in LINE position and then to MIC position.</td><td>The display associated with channel A1 lights. Refer to chart for logic levels and associated parallel output pin numbers.</td><td></td></tr>
<tr><td>(Cont)</td><td>p. Repeat step o for channels A2, B1, and B2.</td><td>Same as step o.</td><td></td></tr>
</table>

Table 2. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL

3. (Cont)

PARALLEL INPUT	PIN NO P1-( )	CHANNEL ENABLE SWITCH POSITION			IF ABNORMAL CHECK
		LINE	OFF	MIC	
A2 ENBL	17	1	0	1	U25, U17, U7, U11, and associated circuits.
A1 ENBL	26	1	0	1	
B1 ENBL	6	1	0	1	
B2 ENBL	74	1	0	1	

Note

Vbfo and AFC enable tests, steps q through t, are applicable to receiver controls only.

q. Set control unit AFC switch to OFF.	Logic level 0 at P1-34. (NMT 0.5 V dc.)	
r. Set control unit AFC switch to ON.	Logic level 1 at P1-34. (NLT +3.0 V dc.)	Check U26, U27, U17, U7, U11, and associated circuits.
s. Set control unit VBFO switch to FXO.	Logic level 0 at P1-35. (NMT 0.5 V dc.)	
t. Set control unit VBFO switch to VAR.	Logic level 1 at P1-35. (NLT 3.0 V dc.)	Same as step s.

Note

Peak clip enable test, step u and v, are applicable to exciter controls only.

(Cont)

Table 2. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	u. Set control unit PEAK CLIP switch to OFF.	Logic level 0 at P1-32. (NMT 0.5 V dc.)	Same as step s.
	v. Set control unit PEAK CLIP switch to ON.	Logic level 1 at P1-32. (NLT 3.0 V dc.)	
4. Data inputs, word 3	a. Set control unit CONT switch to TEST. *Note* Word 3 tests can also be accomplished with control unit CONT switch in NORM and local unit CONT switch in REM. Then measure voltages at local unit parallel output card (the card being tested). Pa tests, steps b through e, are applicable to the exciter and receiver-exciter controls only.		
	b. Set control unit PA PWR switch to OFF.	Check logic levels at the associated parallel output pin numbers as shown in chart.	
	c. Set control unit PA PWR switch to STBY.	Check logic levels at the associated parallel output pin numbers as shown in chart.	
(Cont)	d. Set control unit PA PWR switch to HIGH PWR.	Check logic levels at the associated parallel output pin numbers as shown in chart.	

Table 2. Parallel Output, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>4. (Cont)</td><td>e. Set control unit PA PWR switch to LOW PWR.

Note

Logic 1 = NLT +3.0 V dc.
Logic 0 = NMT 0.5 V dc.</td><td>Check logic levels at the associated parallel output pin numbers as shown in chart.</td><td></td></tr>
<tr><td></td><td>
<table>
<tr><th rowspan="2">PARALLEL OUTPUT</th><th rowspan="2">PIN NO P1-( )</th><th colspan="4">PA PWR SWITCH POSITION</th><th rowspan="2">IF ABNORMAL CHECK</th></tr>
<tr><th>OFF</th><th>STBY</th><th>HIGH PWR</th><th>LOW PWR</th></tr>
<tr><td>PA LV EN</td><td>79</td><td>0</td><td>1</td><td>1</td><td>1</td><td rowspan="3">U19, U5, U7, U11, and associated circuits.</td></tr>
<tr><td>PA HV EN</td><td>14</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>LO PWR EN</td><td>78</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
</table>
</td><td></td><td></td></tr>
<tr><td></td><td>Note

Pilot carrier tests, steps f and g, are applicable to the exciter controls only.

f. Set control unit PILOT CARR switch to OFF.

g. Set control unit PILOT CARR switch to ON.

Note

Dvbfo tests, steps h through k, are applicable only to the receiver with a dvbfo option installed.

h. Set the control unit MODE switch to CW and the VBFO switch to VAR.</td><td>Logic level 0 at P1-82 (NMT 0.5 V dc).

Logic level 1 at P1-82 (NLT +3.0 V dc).</td><td>Check U19, U5, U7, U11, and associated circuits.</td></tr>
<tr><td>(Cont)</td><td></td><td></td><td></td></tr>
</table>

Table 2. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	i. Set digital VBFO controls for +9990 Hz.	VBFO frequency display reads +9990. Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	j. Set digital VBFO controls for -6660 Hz.	VBFO frequency display reads -6660. Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	k. Set digital VBFO controls for +1000 Hz.	VBFO frequency display reads +1000. Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.

Note

Logic 1 = NLT +3.0 V dc.
Logic 0 = NMT 0.5 V dc.

BCD OUTPUT SIGNAL		PARALLEL OUTPUT PIN NO P1-( )	LOGIC LEVELS +9990	LOGIC LEVELS -6660	LOGIC LEVELS +1000	IF ABNORMAL CHECK
DVBFO 1 kHz	(8)	48	1	0	0	U29, U5, U7, U11, and associated circuits.
	(4)	113	0	1	0	
	(2)	47	0	1	0	
	(1)	112	1	0	1	
DVBFO 100 Hz	(8)	46	1	0	0	U21, U5, U7, U11, and associated circuits.
	(4)	111	0	1	0	
	(2)	110	0	1	0	
	(1)	44	1	0	0	
DVBFO 10 Hz	(8)	109	1	0	0	
	(4)	43	0	1	0	
	(2)	108	0	1	0	
	(1)	42	1	0	0	
DVBFO SIGN		107	1	0	1	U29, U5, U7, U11, and associated circuits.

(Cont)

Table 2. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	a. Set control unit CONT switch to NORM.		
	b. Set local unit CONT switch to LCL.		
	Note System key test, steps c and d, is applicable only to exciter controls.		
	c. Set local unit KEY switch to LOCK.	Control unit KEY display lights. Logic level 1 at P1-68 (NLT +3.0 V dc).	Check U15, U17, U7, U11, and associated circuits.
	d. Set local unit KEY switch to NORM.	Control unit KEY display goes out. Logic level 0 at P1-68 (NMT 0.5 V dc).	
	e. Set local unit PWR switch off.	Control unit EXCTR FAULT flashes. Logic level 1 follows light at P1-12 (NLT +3.0 V dc.)	Check U16, U12, U32, U8, U17, U7, U11, and associated circuits.
	f. Set local unit PWR switch to ON. Change any frequency control on local unit front panel.	Control unit EXCTR FAULT goes out. Logic level 0 at P1-12 (NMT 0.5 V dc).	
	Note Receive overload test, steps g and h, is applicable only to receiver controls.		
	g. Connect +5 V dc to local unit J16-27.	Control unit RF OVERLOAD lights. Logic level 1 at P1-68 (NLT-+3.0 V dc)	Check U16, U17, U7, U11, and associated circuits.
	h. Remove +5 V dc from local unit J16-27.	Control unit RF OVERLOAD goes out. Logic level 0 at P1-68 (NMT 0.5 V dc).	Same as step g.
(Cont)	***Note*** Coupler fault test, steps i and j, is applicable only to exciter controls.		

Table 2. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	i. Connect +5 V dc to local unit J15-1.	Control unit COUPLER FAULT lights. Logic level 1 at P1-92 (NLT +3.0 V dc).	
	j. Remove +5 V dc from local unit J15-1.	Control unit COUPLER FAULT lights. Logic level 0 at P1-92 (NMT 0.5 V dc).	
	Note Rf out test, steps k and l, is applicable only to exciter controls.		
	k. Connect ground signal to local unit J15-5.	Control unit RF OUT lights. Logic level 1 at P1-5 (NLT +3.0 V dc).	
	l. Remove ground signal from local unit J15-5.	Control unit RF OUT goes out. Logic level 0 at P1-5 (NMT 0.5 V dc).	Same as step g.
	Note Pa fault test, steps m and n, is applicable only to exciter controls.		
	m. Connect +5 V dc to local unit J15-3.	Control unit PA FAULT lights. Logic level 1 at P1-104 (NLT +3.0 V dc).	
	n. Remove +5 V dc from local unit J15-3.	Control unit PA FAULT goes out. Logic level 0 at P1-104 (NMT 0.5 V dc).	
	Note Pa ready test, steps o and p, is applicable only to exciter controls.		
(Cont)	o. Connect ground signal to local unit J15-21.	Control unit PA READY lights. Logic level 0 at P1-70 (NMT 0.5 V dc).	

Table 2. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	p. Remove ground signal from local unit J15-21.	Control unit PA READY goes out. Logic level 0 at P1-70 (NMT 0.5 V dc).	Same as step g.
	q. Press and hold local unit CONT switch to MON.	Logic level 1 at P1-30 (NLT +3.0 V dc).	Check U24, U17, U7, U11, and associated circuits.
	r. Set local unit CONT switch to REM.	Logic level 0 at P1-30 (NMT 0.5 V dc).	
	s. Set local unit CONT switch to LCL.	Logic level 1 at P1-95 (NLT +3.0 V dc).	
		Control unit BUSY indicator lights. Logic level 1 at P1-7 (NLT +3.0 V dc).	Check U28, U20, U12, U4, U24, U17, U7, U11, and associated circuits.
	t. Set local unit CONT switch to REM.	After short delay logic level 0 at P1-95 (NMT 0.5 V dc).	Same as step s.
		After short delay control unit BUSY indicator goes out. Logic level 0 at P1-7 (NMT 0.5 V dc).	
	u. Set local unit CONT switch to LCL.		
	v. Apply a ground to local unit A13U51A-6.		
	w. Apply a ground to local unit A13U51A-3.		
	x. Remove ground from local unit A13U51A-3.		
	y. Apply ground to local unit A13U16A-1, 2, 8.		
	z. Remove ground from local unit A13U16A-1, 2, 8.	Logic level 1 at P1-29 (NLT +3.0 V dc).	Same as step q.
	aa. Remove ground from local unit A13U51A-6.		
(Cont)	ab. Apply ground to local unit A13U42A-3.	Logic level 0 at P1-29 (NMT 0.5 V dc).	

Table 2. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	ac. Remove ground from local unit A13U42A-3.		Same as step q.
	ad. Apply +5 V dc to local unit J16-8.	Control unit PRE-SEL FAULT lights. Logic level 1 at P1-28 (NLT +3.0 V dc).	
	ae. Remove +5 V dc from local unit J16-8.	Control unit PRE-SEL FAULT goes out. Logic level 0 at P1-28 (NMT 0.5 V dc).	

4. UNIT STRAPPING

The parallel output card must be strapped for proper operation at initial installation and/or following testing and troubleshooting. Strapping is accomplished using jumper clips over the square pins marked E1 through E6.

Place jumper connectors (quantity 4) on each of the square pin pairs labeled E1 through E4.

Pin pair E5 is strapped between the middle and top pins for a flashing fault indicator or strapped between the middle and bottom pins for a nonflashing fault indicator.

Pin pair E6 is strapped between the middle and right pins for character 4, bit 1 fault position (2-channel equipment) or character 2, bit 6 fault position (4-channel equipment).

5. REPAIR

Repair of the parallel output card is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

6.1 Introduction

Caution

This equipment contains electrostatic discharge sensitive (ESDS) devices. Special handling methods and materials must be used to prevent equipment damage. Refer to the maintenance section for the equipment before assembly/disassembly or repair is performed. ESDS items are identified in the description column of the parts list by (ESDS).

All supporting parts list illustrations that contain ESDS items are shown with the following symbol.

This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figure 3). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on the schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator. In addition, the manufacturer's code and part number are listed when applicable.

6.2 Parts List

REF DES Column — Reference designators of each part/subassembly are listed in alphanumeric sequence. These are the reference designators shown on the parts location drawing and schematic diagram.

DESCRIPTION Column — Lists the noun name, modifier, descriptive information, and modifications.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points to the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

COLLINS PART NUMBER Column — Lists the Collins part number for each item in the parts list.

USABLE ON CODE Column — Part variations within a group of equipment are indicated by a letter code (A, B, C, etc). Absence of a code indicates part applies to all models.

MFR CODE Column — Lists the manufacturer's code from which selected parts can be procured.

MFR PART NUMBER Column — Lists the manufacturer's part number for the selected parts.

Listed below are the manufacturer's names and addresses for the manufacturer's codes used in this parts list.

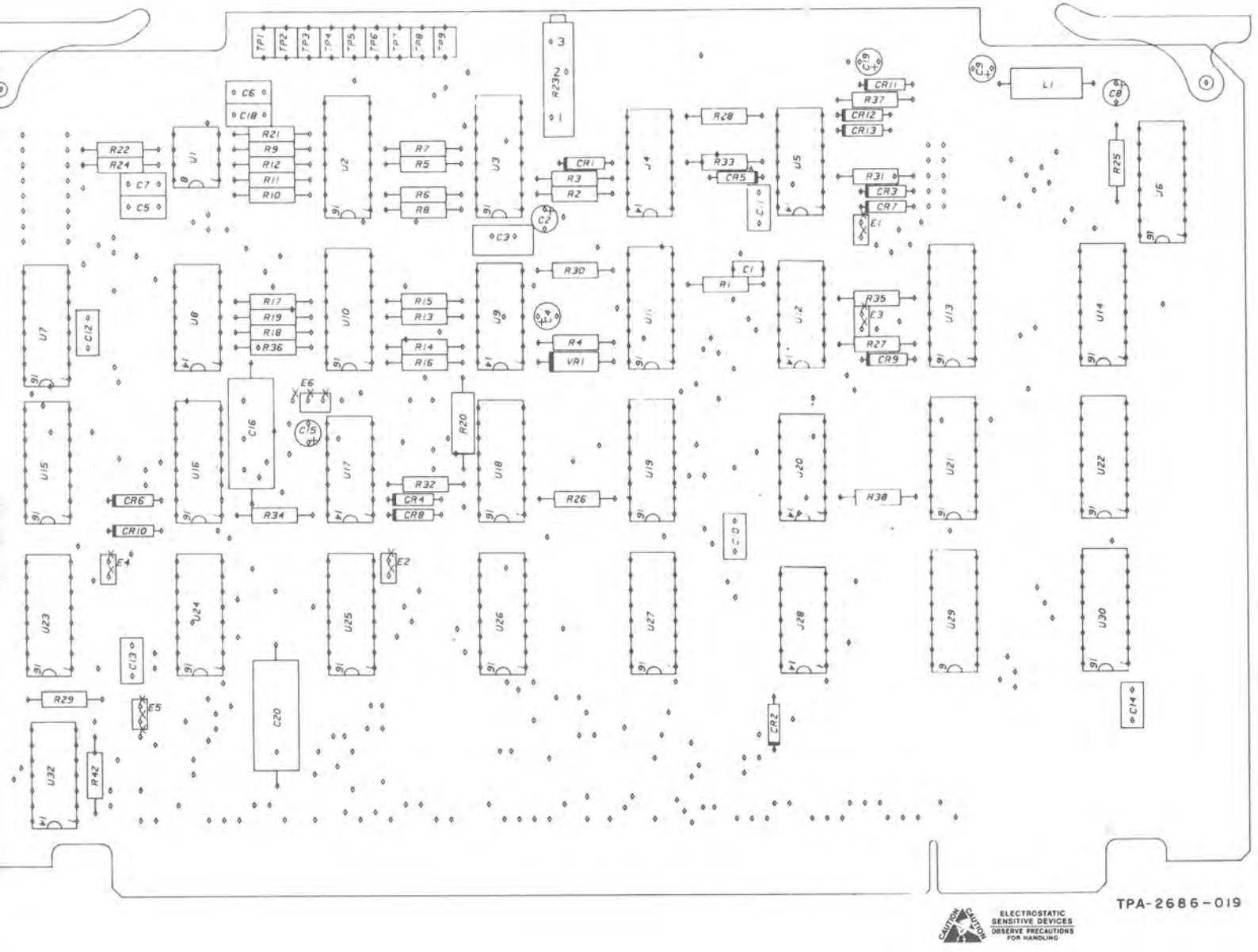
MFR CODE	MANUFACTURER'S NAME AND ADDRESS
02735	RCA CORP SOLID STATE DIVISION ROUTE 202 SOMERVILLE NJ 08876

MFR CODE	MANUFACTURER'S NAME AND ADDRESS
03508	GENERAL ELECTRIC CO SEMI-CONDUCTOR PRODUCTS DEPT W GENESEE ST AUBURN NY 13021
04099	CAPCO INC FORESIGHT INDUSTRIAL PARK P O BOX 2164 GRAND JUNCTION CO 81501
04713	MOTOROLA INC SEMICONDUCTOR PRODUCTS GROUP 5005 E MCDOWELL RD PHOENIX AZ 85008
07263	FAIRCHILD CAMERA AND INSTRUMENT CORP SEMICONDUCTOR DIV 464 ELLIS ST MOUNTAIN VIEW CA 94042
16546	GLOBE-UNION INC USCC/CENTRALAB ELECTRICS DIV 4561 COLORADO LOS ANGELES CA 90039
22526	BERG ELECTRONICS INC YOUK EXPRESSWAY NEW CUMBERLAND PA 17070
56289	SPRAGUE ELECTRIC CO NORTH ADAMS MA 01247
74970	JOHNSON E F CO 299 10TH AVE S W WASECA MN 56093
80294	BOURNS INC INSTRUMENT DIV 6135 MAGNOLIA AVE RIVERSIDE CA 92506
81349	MILITARY SPECIFICATION
96906	MILITARY STANDARD

6.3 Equipment Covered

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Parallel Output	642-3137-001	REV F



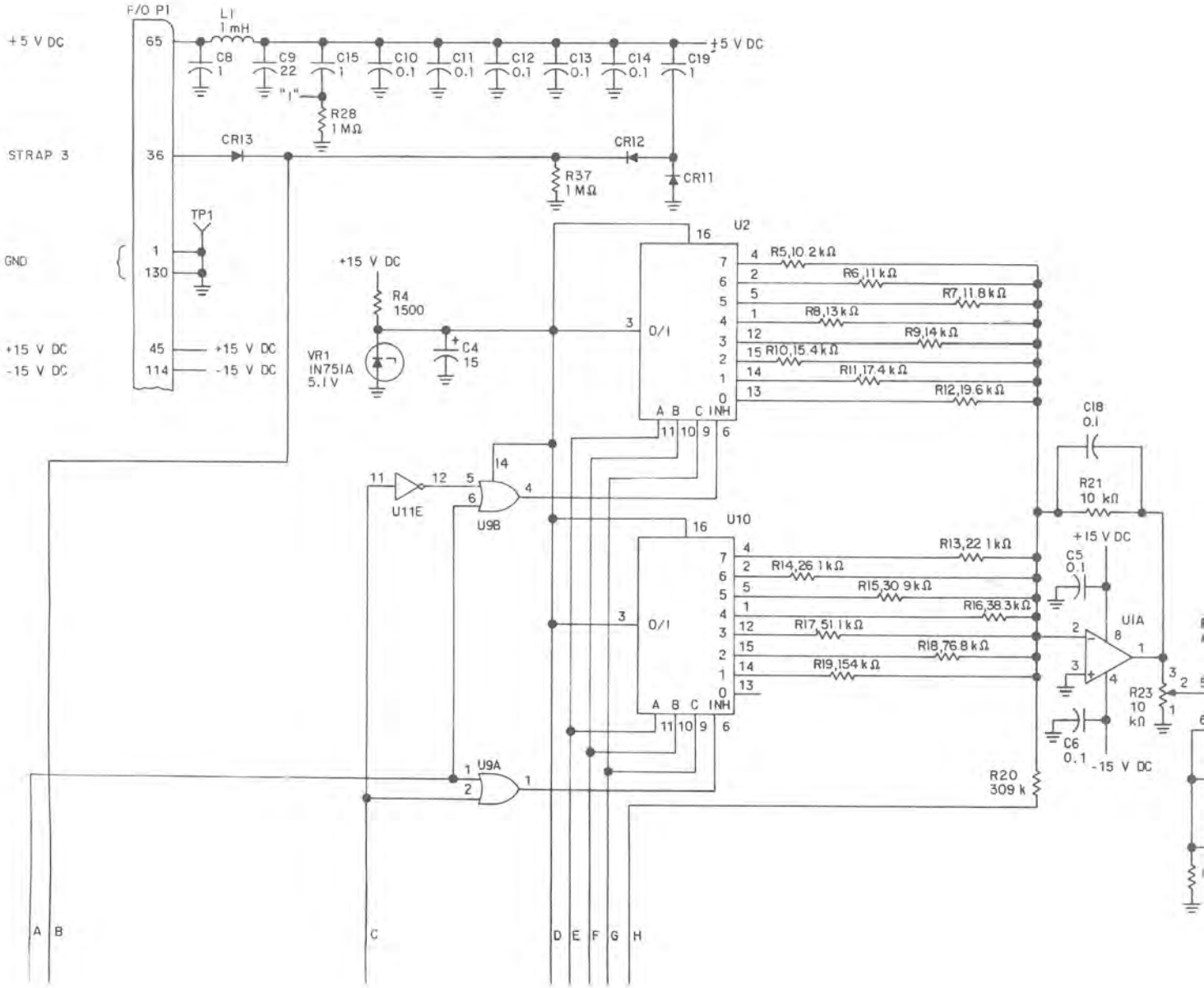
Parallel Output, Schematic Diagram
Figure 3 (Sheet 1 of 6)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE	MFR CODE	MFR PART NUMBER
	PARALLEL OUTPUT (ESDS)	642-3137-001			
CR1-CR13	SEMICOND DEVICE	353-3644-010		03508	1N4454GE
C1	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000		81349	CK05BX102K
C2	CAPACITOR,FXD TNTLM ELCTLT, 0.47UF, 20%, 35V	184-9102-330		56289	199D474X0035AB1
C3	CAPACITOR,FXD MICA DIEL, 100PF, 5%, 500V	912-3879-000		81349	CM04FD101J03
C4	CAPACITOR,FXD TNTLM ELCTLT, 15UF, 20%, 15V	184-9102-130		56289	199D156X0015CB1
C5-C7	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-200		16546	CY30C104M
C8	CAPACITOR,FXD TNTLM ELCTLT, 1UF, 20%, 35V	184-9102-350		56289	199D105X0035BB1
C9	CAPACITOR,FXD TNTLM ELCTLT, 22UF, 20%, 10V	184-9102-080		56289	199D226X0010CB1
C10-C14	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-200		16546	CY30C104M
C15	CAPACITOR,FXD TNTLM ELCTLT, 1UF, 20%, 35V	184-9102-350		56289	199D105X0035BB1
C16	CAPACITOR,FXD PLSTC DIEL, 1UF, 10%, 50V	933-1081-200		04099	CRC1-200
C17	NOT USED				
C18	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-200		16546	CY30C104M
C19	CAPACITOR,FXD TNTLM ELCTLT, 1UF, 20%, 35V	184-9102-350		56289	199D105X0035BB1
C20	CAPACITOR,FXD PLSTC DIEL, 1UF, 10%, 50V	933-1081-200		04099	CRC1-200
E1-E6	CONNECTOR,JMPR SYS	372-0046-010		22526	65474-001
L1	COIL,RF 1000UH	240-2540-000		96906	MS90539-15
R1	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000		81349	RCR07G105KS
R2,R3	RESISTOR,FXD CMPSN, 1.8MEGO, 10%, 1/4W	745-0866-000		81349	RCR07G185KS
R4	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/4W	745-0755-000		81349	RCR07G152KS
R5	RESISTOR,FXD FILM, 10.2K, 1%, 1/8W	705-3605-480		81349	RN55D1022F
R6	RESISTOR,FXD FILM, 11K, 1%, 1/8W	705-1046-000		81349	RN55D1102F
R7	RESISTOR,FXD FILM, 11.8K, 1%, 1/8W	705-3605-510		81349	RN55D1182F
R8	RESISTOR,FXD FILM, 13K, 1%, 1/8W	705-3605-530		81349	RN55D1302F
R9	RESISTOR,FXD FILM, 14K, 1%, 1/8W	705-1051-000		81349	RN55D1402F
R10	RESISTOR,FXD FILM, 15.4K, 1%, 1/8W	705-1053-000		81349	RN55D1542F
R11	RESISTOR,FXD FILM, 17.4K, 1%, 1/8W	705-3605-590		81349	RN55D1742F
R12	RESISTOR,FXD FILM, 19.6K, 1%, 1/8W	705-1058-000		81349	RN55D1962F
R13	RESISTOR,FXD FILM, 22.1K, 1%, 1/8W	705-3605-640		81349	RN55D2212F
R14	RESISTOR,FXD FILM, 26.1K, 1%, 1/8W	705-1064-000		81349	RN55D2612F
R15	RESISTOR,FXD FILM, 30.9K, 1%, 1/8W	705-3605-710		81349	RN55D3092F
R16	RESISTOR,FXD FILM, 38.3K, 1%, 1/8W	705-1072-000		81349	RN55D3832F
R17	RESISTOR,FXD FILM, 51.1K, 1%, 1/8W	705-1078-000		81349	RN55D5112F
R18	RESISTOR,FXD FILM, 76.8K, 1%, 1/8W	705-3605-900		81349	RN55D7682F
R19	RESISTOR,FXD FILM, 154K, 1%, 1/8W	705-1101-000		81349	RN55D1543F
R20	RESISTOR,FXD FILM, 309K, 1%, 1/4W	705-3601-230		81349	RN60D3093F
R21,R22	RESISTOR,FXD FILM, 10K, 1%, 1/8W	705-1044-000		81349	RN55D1002F
R23	RESISTOR,VAR 10K, 10%, 3/4W	382-0012-290		80294	3006P1-103
R24	RESISTOR,FXD FILM, 1K, 1%, 1/8W	705-0996-000		81349	RN55D1001F
R25,R26	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000		81349	RCR07G105KS
R27	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000		81349	RCR07G104KS
R28-R35	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000		81349	RCR07G105KS
R36	RESISTOR,FXD CMPSN, 0.68MEGO, 10%, 1/4W	745-0851-000		81349	RCR07G684KS
R37,R38	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000		81349	RCR07G105KS
R39-R41	NOT USED				
R42	RESISTOR,FXD CMPSN, 2.7MEGO, 10%, 1/4W	745-0872-000		81349	RCR07G275KS
TP1	JACK,TIP BRN	360-0484-070		74970	105-1108-011
TP2	JACK,TIP RED	360-0484-020		74970	105-1102-011
TP3	JACK,TIP ORN	360-0484-050		74970	105-1106-011
TP4	JACK,TIP YEL	360-0484-060		74970	105-1107-011
TP5	JACK,TIP GRN	360-0484-040		74970	105-1104-011
TP6	JACK,TIP BLU	360-0484-080		74970	105-1110-011
TP7	JACK,TIP VIO	360-0484-090		74970	105-1112-011
TP8	JACK,TIP GRA	360-0484-100		74970	105-1113-011
TP9	JACK,TIP WHT	360-0484-010		74970	105-1101-011
U1	INTEGRATED CIRCUIT OPNL AMPLIFIER	351-1071-070		07263	UA1458TC
U2	INTEGRATED CKT (ESDS)	351-8227-010		07263	F4051PC
U3	INTEGRATED CIRCUIT (ESDS)	351-8479-010		04713	MC14538BCP
U4	INTEGRATED CIRCUIT (ESDS)	351-8159-040		04713	MC14011UBCP
U5	INTEGRATED CIRCUIT (ESDS)	351-8159-110		07263	4013BPC
U6	INTEGRATED CIRCUIT REGISTER (ESDS)	351-8346-010		02735	CD4094BE
U7	INTEGRATED CKT (ESDS)	351-8227-010		07263	F4051PC
U8	MICROCIRCUIT (ESDS)	351-8200-020		02735	CD4047BE
U9	INTEGRATED CIRCUIT MOS GATE (ESDS)	351-8287-010		02735	CD4071BE
U10	INTEGRATED CKT (ESDS)	351-8227-010		07263	F4051PC
U11	INTEGRATED CIRCUIT (ESDS)	351-8159-210		07263	F4049BPC
U12	INTEGRATED CIRCUIT (ESDS)	351-8407-010		04713	MC14070BCP
U13-U16	INTEGRATED CIRCUIT REGISTER (ESDS)	351-8346-010		02735	CD4094BE
U17	INTEGRATED CIRCUIT (ESDS)	351-8159-110		07263	4013BPC
U18,U19	INTEGRATED CIRCUIT REGISTER (ESDS)	351-8346-010		02735	CD4094BE
U20	INTEGRATED CIRCUIT (ESDS)	351-8159-110		07263	4013BPC
U21-U27	INTEGRATED CIRCUIT REGISTER (ESDS)	351-8346-010		02735	CD4094BE
U28	INTEGRATED CIRCUIT MOS GATE (ESDS)	351-8287-030		02735	CD4081BE
U29,U30	INTEGRATED CIRCUIT REGISTER (ESDS)	351-8346-010		02735	CD4094BE
U31	NOT USED				
U32	MICROCIRCUIT (ESDS)	351-8200-020		02735	CD4047BE
VR1	SEMICOND DEVICE	353-2710-000		07263	1N751A

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. TYPE DESIGNATION SHOWN MAY BE GENERIC IN FORM AND ARE FOR REFERENCE ONLY. SEE APPLICABLE PARTS LIST FOR REPLACEMENT PARTS.
4. UNLESS OTHERWISE SPECIFIED, DIODES ARE TYPE IN4454.
5. P2 IS A CABLE CONNECTOR FIELD. THIS CABLE CONNECTOR (372-0043-010) IS NOT IN 642-3137-001 CONFIGURATION.
6. THE FOLLOWING PARTS PROVIDE FOR REMOTE CONTROL OF LOCAL/REMOTE IN A RADIO AND ARE NOT IN 642-3137-001 CONFIGURATION: R39, R40, R41, Q1, Q2, AND U31.
7. SIGNAL NAMES ARE NOT SHOWN FOR P1 AND P2 PINS THAT ARE A CONTROL/STATUS BITS. THESE PINS HAVE DIFFERENT SIGNAL N THE EQUIPMENT THIS CARD IS USED IN. REFER TO TABLE FOR NAMES). ALL PIN NUMBERS IN TABLE ARE ON P1, EXCEPT WORD WHICH ARE ON P2.
8. NONSTANDARD ABBREVIATION; FLT = FAULT
9. PIN NUMBERS IN PARENTHESIS IN TABLE ARE STATUS OUTPUTS
10. THIS EQUIPMENT CONTAINS ELECTROSTATIC DISCHARGE SENSIT SPECIAL HANDLING METHODS AND MATERIALS MUST BE USED T DAMAGE.



NS THAT ARE ASSOCIATED WITH
RENT SIGNAL NAMES DEPENDING ON
TO TABLE FOR PIN FUNCTIONS (SIGNAL
, EXCEPT WORD 3, CHARACTER 4

ATUS OUTPUTS IN CONTROL UNITS ONLY.

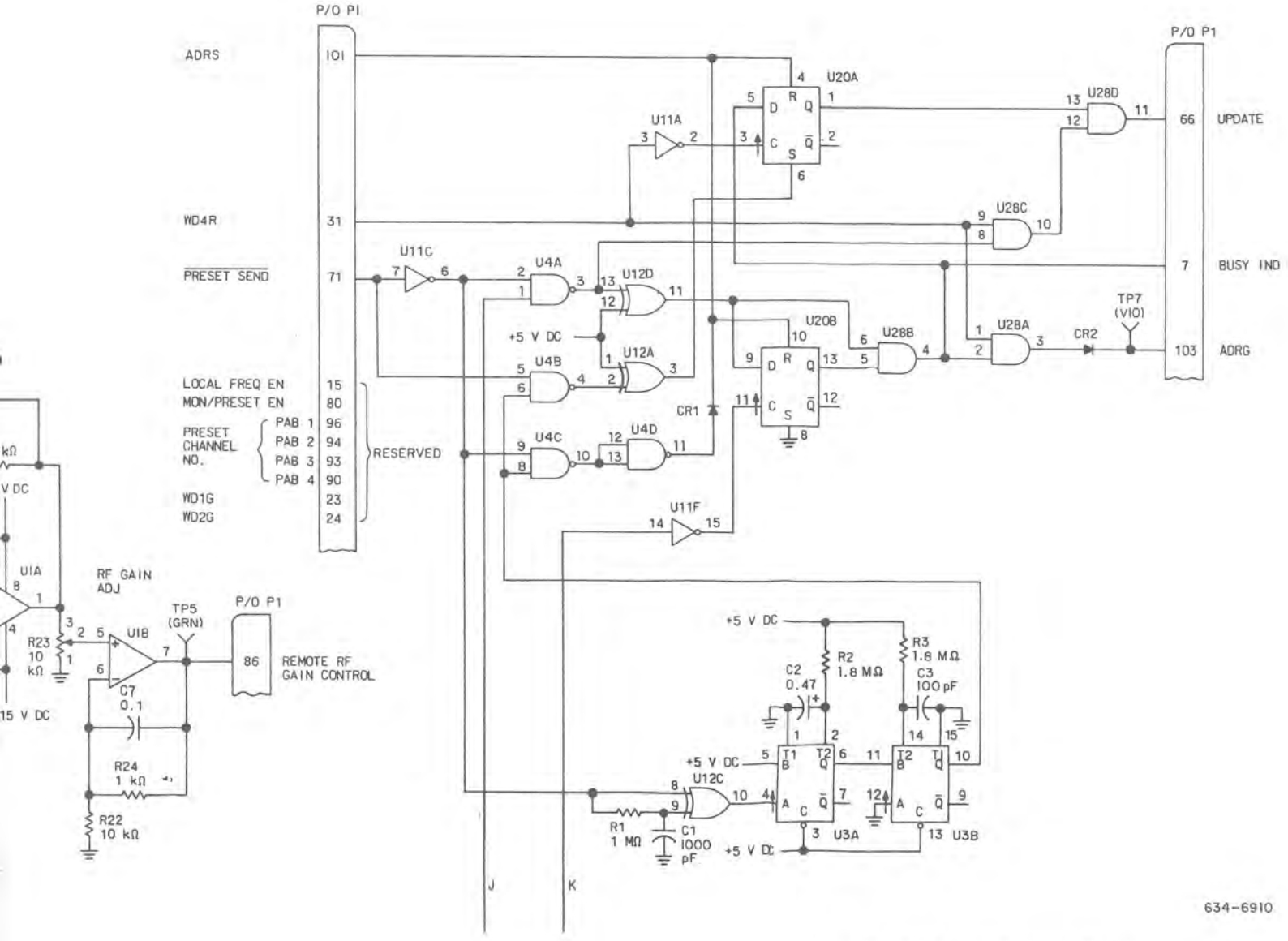
CHARGE SENSITIVE (ESDS) DEVICES.
OST BE USED TO PREVENT EQUIPMENT

MICROCIRCUIT INFORMATION

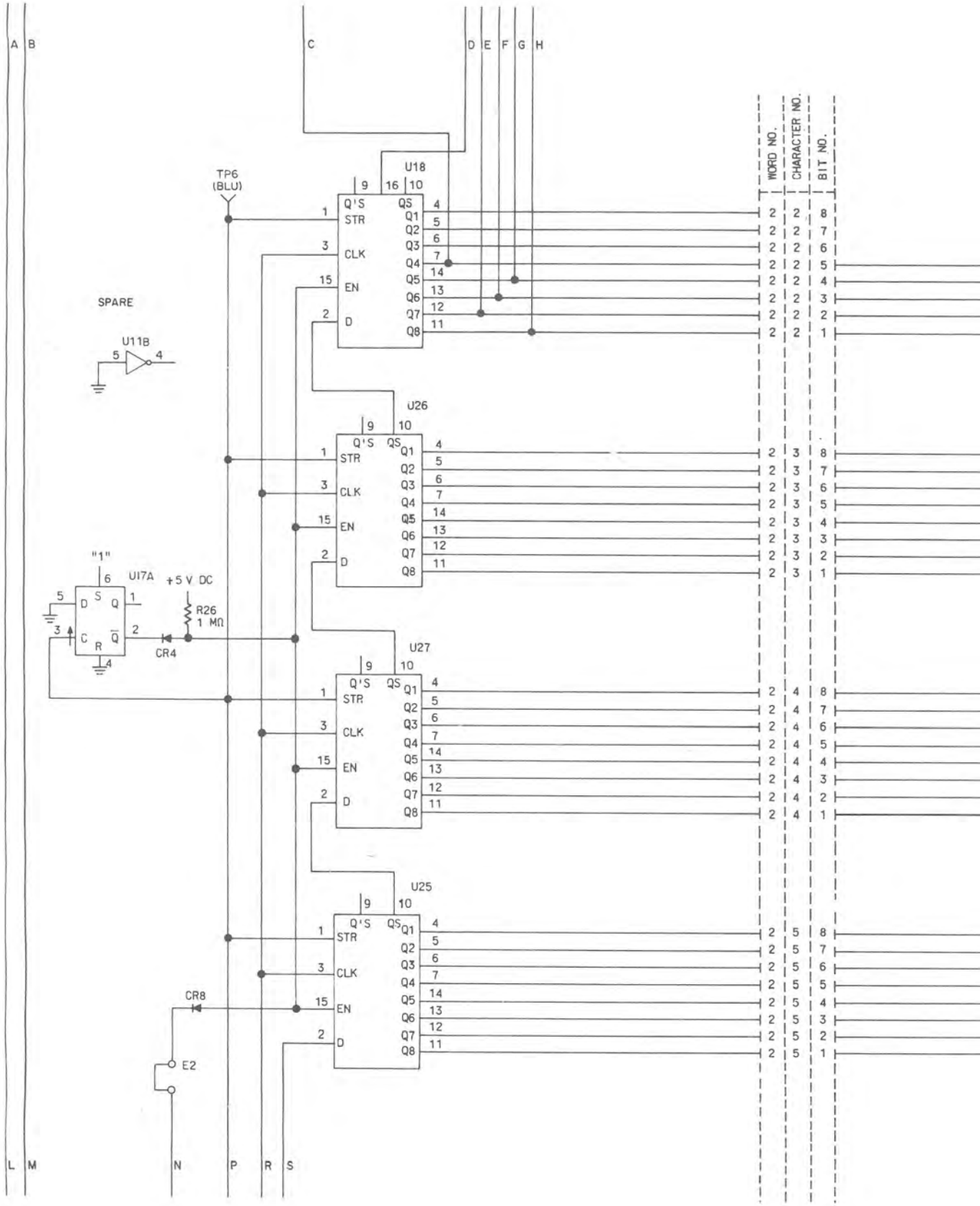
REF DES	COMMON DEVICE OR COLLINS PN	PWR (V DC)	
		+5	GND
U1	MC1458P1		
U2	F4051PC	16	8,7
U3	MC14538BCP	16	8
U4	MC14011CP	14	7
U5	F4013BPC	14	7
U6	CD4094BE	16	8
U7	F4051PC	16	8,7
U8	CD4047AE	14	7
U9	MC14071BCP		7
U10	F4051PC	16	8,7
U11	F4049BPC	1	8
U12	MC14070BCP	14	7
U13	CD4094BE	16	8
U14	CD4094BE	16	8
U15	CD4094BE	16	8
U16	CD4094BE	16	8

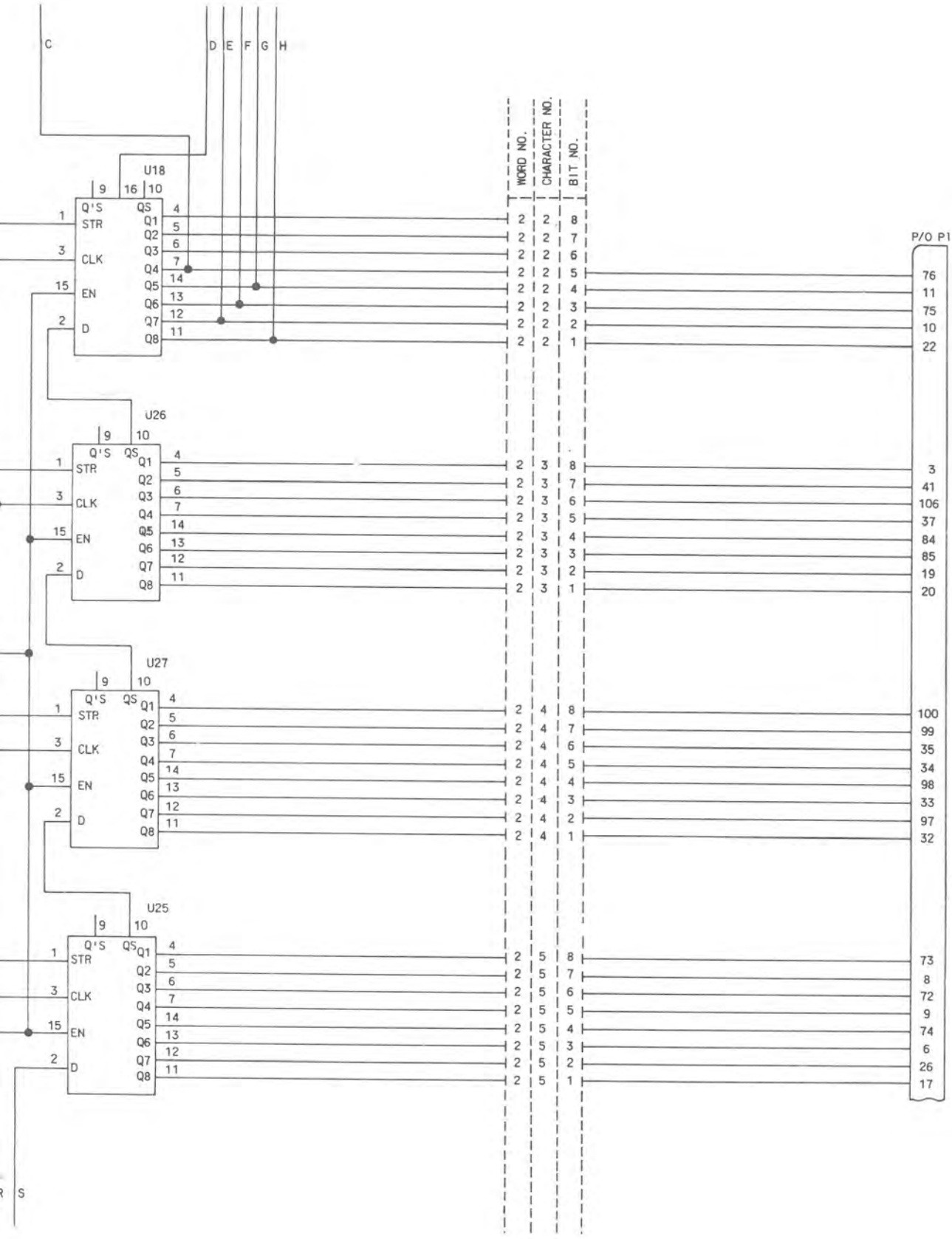
MICROCIRCUIT INFORMATION

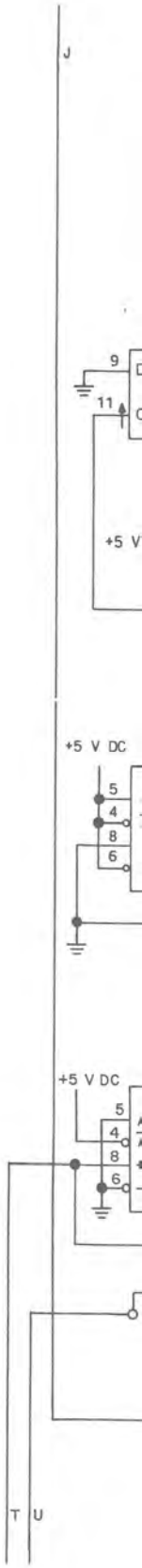
REF DES	COMMON DEVICE OR COLLINS PN	PWR (V DC)	
		+5	GND
U17	F4013BPC	14	7
U18	CD4094BE	16	8
U19	CD4094BE	16	8
U20	F4013BPC	14	7
U21	CD4094BE	16	8
U22	CD4094BE	16	8
U23	CD4094BE	16	8
U24	CD4094BE	16	8
U25	CD4094BE	16	8
U26	CD4094BE	16	8
U27	CD4094BE	16	8
U28	MC14081BCP	14	7
U29	CD4094BE	16	8
U30	CD4094BE	16	8
U31	CD4094BE	16	8
U32	CD4047AE	14	7

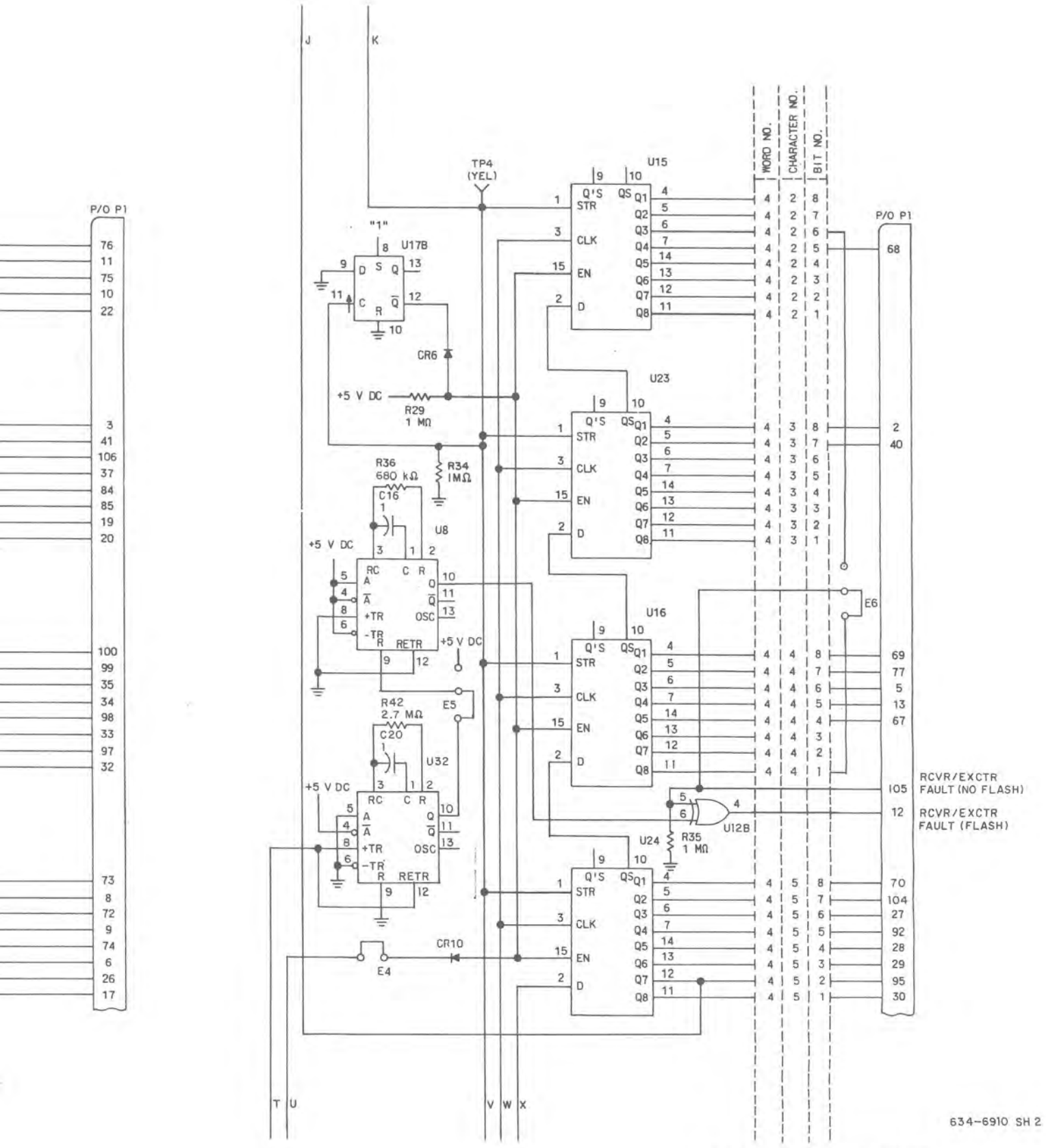


Parallel Output, Schematic Diagram
Figure 3 (Sheet 3)

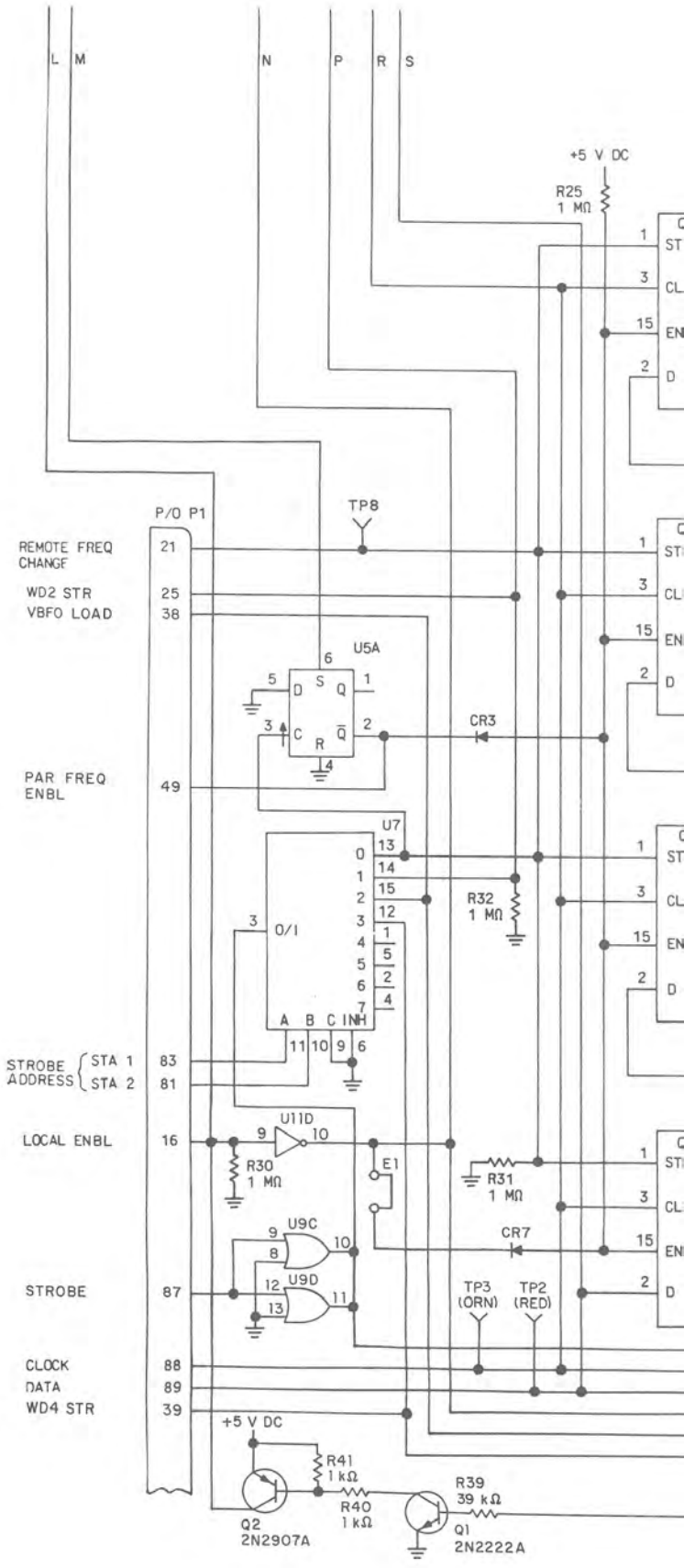

A
B
C
D
E
F
G
H
WORD NO.
CHARACTER NO.
BIT NO.
TP6
(BLU)
U18
U26
U27
U25
SPARE
U11B
"1"
U17A
+5 V DC
R26
1 MΩ
CR4
CR8
E2
STR
CLK
EN
D
Q'S
QS
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
L
M
N
P
R
S

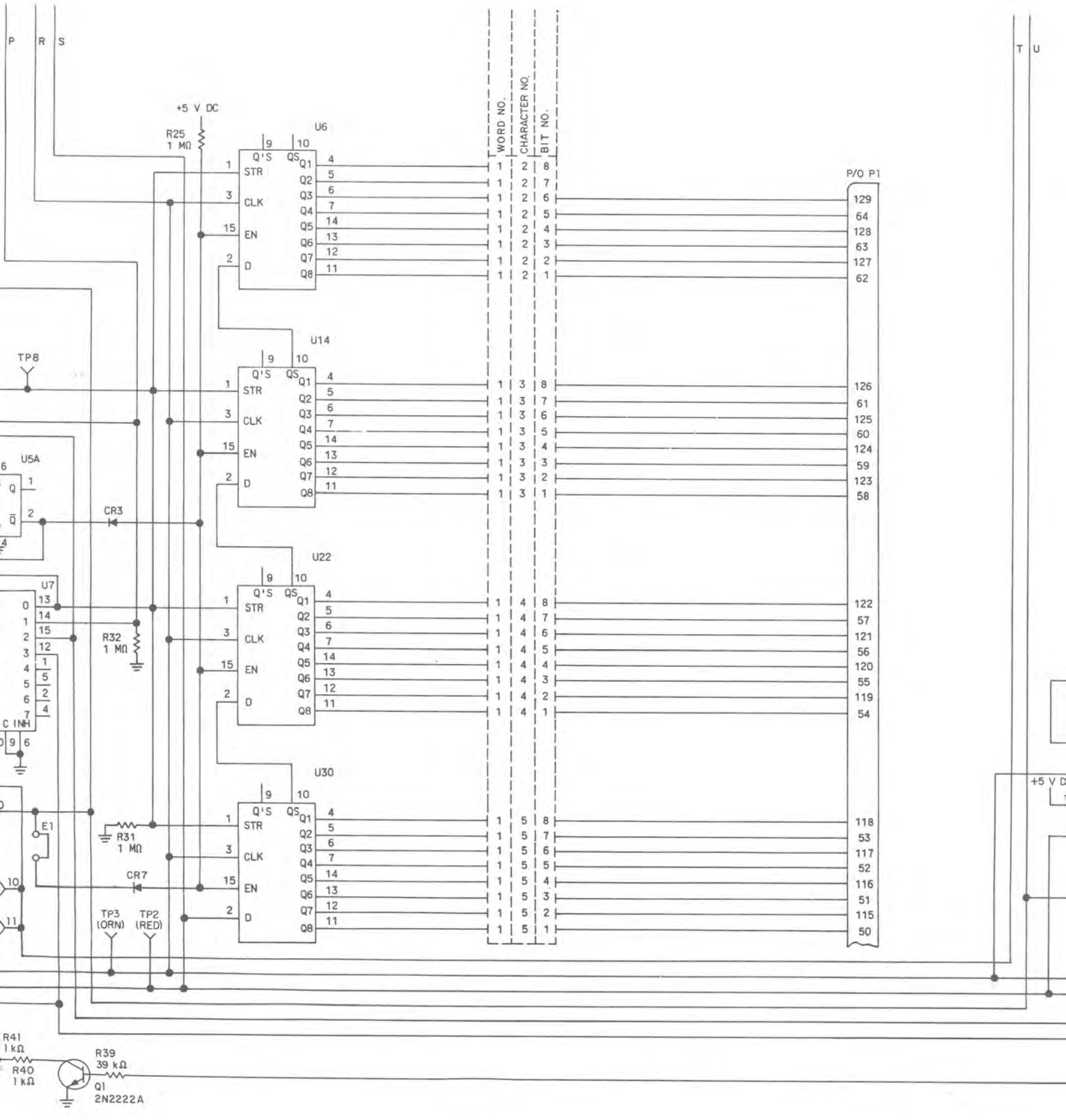

C
D
E
F
G
H
WORD NO.
CHARACTER NO.
BIT NO.
U18
U26
U27
U25
Q'S
QS
STR
CLK
EN
D
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
P/O P1
76
11
75
10
22
3
41
106
37
84
85
19
20
100
99
35
34
98
33
97
32
73
8
72
9
74
6
26
17
R
S

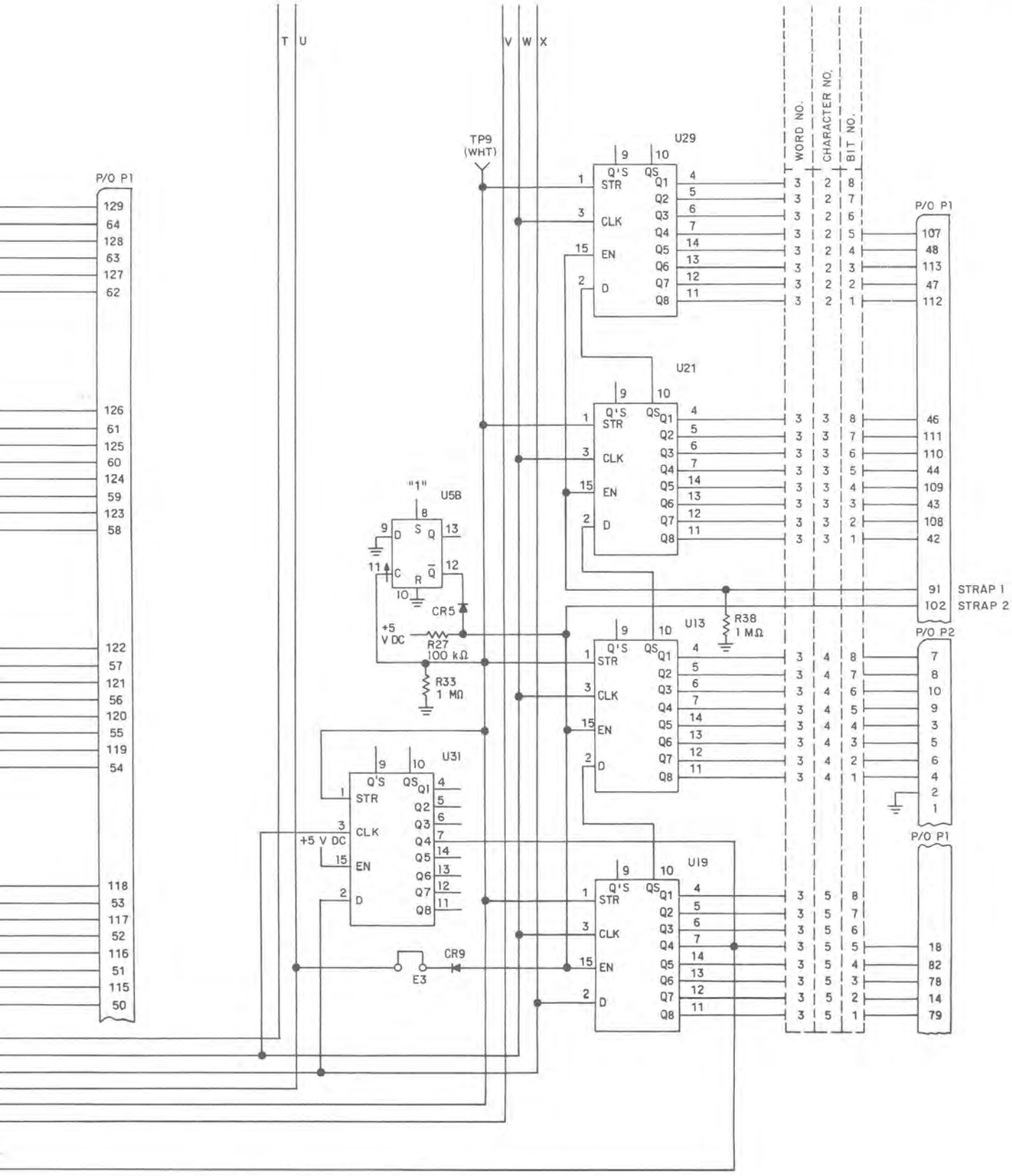

J
+5 V DC
+5 V DC
T
U



Parallel Output, Schematic Diagram
Figure 3 (Sheet 4)


L
M
N
P
R
S
+5 V DC
R25
1 MΩ
P/O P1
TP8
REMOTE FREQ CHANGE
21
WD2 STR
25
VBFO LOAD
38
U5A
CR3
PAR FREQ ENBL
49
U7
R32
1 MΩ
O/I
A B C INH
STROBE ADDRESS
STA 1
83
STA 2
81
LOCAL ENBL
16
U11D
R30
1 MΩ
E1
R31
1 MΩ
U9C
CR7
STROBE
87
U9D
TP3 (ORN)
TP2 (RED)
CLOCK
88
DATA
89
WD4 STR
39
+5 V DC
R41
1 kΩ
R40
1 kΩ
R39
39 kΩ
Q2
2N2907A
Q1
2N2222A


P
R
S
T
U
+5 V DC
R25
1 MΩ
U6
U14
U22
U30
Q'S
QS
STR
CLK
EN
D
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
WORD NO.
CHARACTER NO.
BIT NO.
P/O P1
TP8
U5A
CR3
U7
R32
1 MΩ
C INH
E1
R31
1 MΩ
CR7
TP3
(ORN)
TP2
(RED)
+5 V D
R41
1 kΩ
R40
1 kΩ
R39
39 kΩ
Q1
2N2222A



634-6910 SH 3

Parallel Output, Schematic Diagram
Figure 3 (Sheet 5)

CONTROL / STATUS BIT WORD FORMAT							EQUIPMENT TYPE																							
HF-80 8-BIT				ASCII 7-BIT			HF-80XX 2-CHANNEL RADIOS AND HF-80XX 2-CHANNEL CONTROLS			85IS-1/2, HF-8095			4-CHANNEL EXCITER, AND 4-CHANNEL EXCITER CONTROL			4-CHAN 4-CHAN		
WORD NO.	CHARACTER NO.	BIT NO.		WORD NO	CHARACTER NO.	BIT WT.	PARALLEL OUTPUT PIN NO.	PARALLEL INPUT PIN NO.	FUNCTION	PARALLEL OUTPUT PIN NO.	PARALLEL INPUT PIN NO.	FUNCTION	PARALLEL OUTPUT PIN NO.	PARALLEL INPUT PIN NO.	FUNCTION	PARALLEL OUTPUT PIN NO.	PARALLEL INPUT PIN NO.	
1	2	8		1	6	8		103	COMMAND (C)		103	COMMAND (C)			NOT USED			
1	2	7		1	6	4		38	STATUS REQUEST (S)		38	STATUS REQUEST (S)			NOT USED			
1	2	6		1	6	2	129	129	FREQ 10 MHz (2)	129	129	FREQ 10 MHz (2)	129	129	FREQ 10 MHz (2)	129	12
1	2	5		1	6	1	64	64	FREQ 10 MHz (1)	64	64	FREQ 10 MHz (1)	64	64	FREQ 10 MHz (1)	64	6
1	2	4		1	7	8	128	128	FREQ 1 MHz (8)	128	128	FREQ 1 MHz (8)	128	128	FREQ 1 MHz (8)	128	12
1	2	3		1	7	4	63	63	(4)	63	63	(4)	63	63	(4)	63	6
1	2	2		1	7	2	127	127	(2)	127	127	(2)	127	127	(2)	127	12
1	2	1		1	7	1	62	62	(1)	62	62	(1)	62	62	(1)	62	6
1	3	8		1	8	8	126	126	FREQ 100 kHz (8)	126	126	FREQ 100 kHz (8)	126	126	FREQ 100 kHz (8)	126	12
1	3	7		1	8	4	61	61	(4)	61	61	(4)	61	61	(4)	61	6
1	3	6		1	8	2	125	125	(2)	125	125	(2)	125	125	(2)	125	12
1	3	5		1	8	1	60	60	(1)	60	60	(1)	60	60	(1)	60	6
1	3	4		1	9	8	124	124	FREQ 10 kHz (8)	124	124	FREQ 10 kHz (8)	124	124	FREQ 10 kHz (8)	124	12
1	3	3		1	9	4	59	59	(4)	59	59	(4)	59	59	(4)	59	5
1	3	2		1	9	2	123	123	(2)	123	123	(2)	123	123	(2)	123	12
1	3	1		1	9	1	58	58	(1)	58	58	(1)	58	58	(1)	58	5
1	4	8		1	10	8	122	122	FREQ 1 kHz (8)	122	122	FREQ 1 kHz (8)	122	122	FREQ 1 kHz (8)	122	12
1	4	7		1	10	4	57	57	(4)	57	57	(4)	57	57	(4)	57	5
1	4	6		1	10	2	121	121	(2)	121	121	(2)	121	121	(2)	121	12
1	4	5		1	10	1	56	56	(1)	56	56	(1)	56	56	(1)	56	5
1	4	4		1	11	8	120	120	FREQ 100 Hz (8)	120	120	FREQ 100 Hz (8)	120	120	FREQ 100 Hz (8)	120	12
1	4	3		1	11	4	55	55	(4)	55	55	(4)	55	55	(4)	55	5
1	4	2		1	11	2	119	119	(2)	119	119	(2)	119	119	(2)	119	11
1	4	1		1	11	1	54	54	(1)	54	54	(1)	54	54	(1)	54	5
1	5	8		1	12	8	118	118	FREQ 10 Hz (8)	118	118	FREQ 10 Hz (8)	118	118	FREQ 10 Hz (8)	118	11
1	5	7		1	12	4	53	53	(4)	53	53	(4)	53	53	(4)	53	5
1	5	6		1	12	2	117	117	(2)	117	117	(2)	117	117	(2)	117	11
1	5	5		1	12	1	52	52	(1)	52	52	(1)	52	52	(1)	52	5
1	5	4		1	13	8	116	116	FREQ 1 Hz (8)	116	116	FREQ 1 Hz (8)	116	116	FREQ 1 Hz (8)	116	11
1	5	3		1	13	4	51	51	(4)	51	51	(4)	51	51	(4)	51	5
1	5	2		1	13	2	115	115	(2)	115	115	(2)	115	115	(2)	115	11
1	5	1		1	13	1	50	50	(1)	50	50	(1)	50	50	(1)	50	5
2	2	8		2	6	8		103	COMMAND (C)		103	COMMAND (C)			NOT USED			
2	2	7		2	6	4		38	STATUS REQUEST (S)		38	STATUS REQUEST (S)						
2	2	6		2	6	2			NOT USED			NOT USED						
2	2	5		2	6	1	76	76	RF GAIN (16)	76	76	RF GAIN (16)	76	76		76	7
2	2	4		2	7	8	11	11	(8)	11	11	(8)	11	11		11	1
2	2	3		2	7	4	75	75	(4)	75	75	(4)	75	75		75	7
2	2	2		2	7	2	10	10	(2)	10	10	(2)	10	10		10	1
2	2	1		2	7	1	22	87	(1)	22	87	(1)	22	87		22	8
2	3	8		2	8	8	3		NOT USED	3		NOT USED	3	12	NOT USED	3	12
2	3	7		2	8	4	41	41	VBFO ENBL	41	41	VBFO ENBL	41	41		41	41
2	3	6		2	8	2	106	106	AFC ENBL	106	106	RESERVED	106	106		106	106
2	3	5		2	8	1	37	37	AGC CROWBAR ENBL	37	37	AGC CROWBAR ENBL	37	37		37	37
2	3	4		2	9	8	84	84	USB AGC OFF	84	84	USB AGC OFF	84	84		84	84
2	3	3		2	9	4	85	85	USB AGC FAST	85	85	USB AGC FAST	85	85		85	85
2	3	2		2	9	2	19	19	LSB AGC OFF	19	19	LSB AGC OFF	19	19		19	19
2	3	1		2	9	1	20	20	LSB AGC FAST	20	20	LSB AGC FAST	20	20		20	20
2	4	8		2	10	8	100	100	FL8 ENBL	100	100	FL8 ENBL	100	100	NOT USED	100	100
2	4	7		2	10	4	99	99	FL7 ENBL	99	99	FL7 ENBL	99	99		99	99
2	4	6		2	10	2	35	35	FL6 ENBL	35	35	FL6 ENBL	35	35		35	35
2	4	5		2	10	1	34	34	FL5 ENBL	34	34	FL5 ENBL	34	34		34	34
2	4	4		2	11	8	98	98	FL4 ENBL	98	98	FL4 ENBL	98	98		98	98
2	4	3		2	11	4	33	33	FL3 ENBL	33	33	FL3 ENBL	33	33		33	33
2	4	2		2	11	2	97	97	FL2 ENBL	97	97	FL2 ENBL	97	97		97	97
2	4	1		2	11	1	32	32	FL1 ENBL	32	32	FL1 ENBL	32	32	PEAK CLIPPER ENBL	32	32
2	5	8		2	12	8	73	73	FM ENBL	73	73	FM ENBL	73	73	NOT USED	73	73
2	5	7		2	12	4	8	8	AM ENBL	8	8	AM ENBL	8	8	AM ENBL	8	8
2	5	6		2	12	2	72	72	SSB ENBL	72	72	SSB ENBL	72	72	CW ENBL	72	72
2	5	5		2	12	1	9	9	CW ENBL	9	9	CW ENBL	9	9	ISB ENBL	9	9
2	5	4		2	13	8	74	74	ISB ENBL	74	74	ISB ENBL	74	74	B2 ENBL	74	74
2	5	3		2	13	4	6	92	RESERVED	6	92	RESERVED	6	92	B1 ENBL	6	92
2	5	2		2	13	2	26	91	RESERVED	26	91	RESERVED	26	91	A1 ENBL	26	91
2	5	1		2	13	1	17	21	RESERVED	17	21	RESERVED	17	21	A2 ENBL	17	21

PIN FUNCTION (SIGNAL NAME) TABLE

FUNCTION
USED
USED
10 MHz (2)
10 MHz (1)
1 MHz (8)
(4)
(2)
(1)
100 kHz (8)
(4)
(2)
(1)
10 kHz (8)
(4)
(2)
(1)
1 kHz (8)
(4)
(2)
(1)
100 Hz (8)
(4)
(2)
(1)
10 Hz (8)
(4)
(2)
(1)
1 Hz (8)
(4)
(2)
(1)
SED
SED
SED
LIPPER ENBL
SED
BL
BL
NBL
BL
BL
BL

4-CHANNEL RECEIVER, AND 4-CHANNEL RECEIVER CONTROL

PARALLEL OUTPUT PIN NO.	PARALLEL INPUT PIN NO.	FUNCTION
		NOT USED
		NOT USED
129	129	FREQ 10 MHz (2)
64	64	FREQ 10 MHz (1)
128	128	FREQ 1 MHz (8)
63	63	(4)
127	127	(2)
62	62	(1)
126	126	FREQ 100 kHz (8)
61	61	(4)
125	125	(2)
60	60	(1)
124	124	FREQ 10 kHz (8)
59	59	(4)
123	123	(2)
58	58	(1)
122	122	FREQ 1 kHz (8)
57	57	(4)
121	121	(2)
56	56	(1)
120	120	FREQ 100 Hz (8)
55	55	(4)
119	119	(2)
54	54	(1)
118	118	FREQ 10 Hz (8)
53	53	(4)
117	117	(2)
52	52	(1)
116	116	FREQ 1 Hz (8)
51	51	(4)
115	115	(2)
50	50	(1)
		NOT USED
		NOT USED
		NOT USED
76	76	RF GAIN (16)
11	11	(8)
75	75	(4)
10	10	(2)
22	87	(1)
3	12	FL7 (E) ENBL
41	41	FL6 (D) ENBL
106	106	FL5 (C) ENBL
37	37	FL4 (B) ENBL
84	84	B2 AGC (2)
85	85	B2 AGC (1)
19	19	A2 AGC (2)
20	20	A2 AGC (1)
100	100	FL3 (A) ENBL
99	99	FL1 (16 kHz) ENBL
35	35	VBFO ENBL
34	34	AFC ENBL
98	98	B1 AGC (2)
33	33	B1 AGC (1)
97	97	A1 AGC (2)
32	32	A1 AGC (1)
73	73	DATA NET ENBL
8	8	AM ENBL
72	72	CW ENBL
9	9	ISB ENBL
74	74	B2 ENBL
6	92	B1 ENBL
26	91	A1 ENBL
17	21	A2 ENBL

CONTROL / STATUS BIT WORD FORMAT

HF-80 8-BIT WORD NO.	HF-80 8-BIT CHARACTER NO.	HF-80 8-BIT BIT NO.	ASCII 7-BIT WORD NO.	ASCII 7-BIT CHARACTER NO.	ASCII 7-BIT BIT WT.
3	2	8	3	6	8
3	2	7	3	6	4
3	2	6	3	6	2
3	2	5	3	6	1
3	2	4	3	7	8
3	2	3	3	7	4
3	2	2	3	7	2
3	2	1	3	7	1
3	3	8	3	8	8
3	3	7	3	8	4
3	3	6	3	8	2
3	3	5	3	8	1
3	3	4	3	9	8
3	3	3	3	9	4
3	3	2	3	9	2
3	3	1	3	9	1
3	4	8	3	10	8
3	4	7	3	10	4
3	4	6	3	10	2
3	4	5	3	10	1
3	4	4	3	11	8
3	4	3	3	11	4
3	4	2	3	11	2
3	4	1	3	11	1
3	5	8	3	12	8
3	5	7	3	12	4
3	5	6	3	12	2
3	5	5	3	12	1
3	5	4	3	13	8
3	5	3	3	13	4
3	5	2	3	13	2
3	5	1	3	13	1
4	2	8	4	6	8
4	2	7	4	6	4
4	2	6	4	6	2
4	2	5	4	6	1
4	2	4	4	7	8
4	2	3	4	7	4
4	2	2	4	7	2
4	2	1	4	7	1
4	3	8	4	8	8
4	3	7	4	8	4
4	3	6	4	8	2
4	3	5	4	8	1
4	3	4	4	9	8
4	3	3	4	9	4
4	3	2	4	9	2
4	3	1	4	9	1
4	4	8	4	10	8
4	4	7	4	10	4
4	4	6	4	10	2
4	4	5	4	10	1
4	4	4	4	11	8
4	4	3	4	11	4
4	4	2	4	11	2
4	4	1	4	11	1
4	5	8	4	12	8
4	5	7	4	12	4
4	5	6	4	12	2
4	5	5	4	12	1
4	5	4	4	13	8
4	5	3	4	13	4
4	5	2	4	13	2
4	5	1	4	13	1

HF-80XX 2-CHANNEL RADIOS AND HF-80XX 2-CHANNEL CONTROLS

PARALLEL OUTPUT PIN NO.	PARALLEL INPUT PIN NO.	FUNCTION
	103	COMMAND (C)
	38	STATUS REQUEST (S)
		NOT USED
107	107	VBFO SIGN
48	48	VBFO FREQ 1 kHz (8)
113	113	(4)
47	47	(2)
112	112	(1)
46	46	VBFO FREQ 100 Hz (8)
111	111	(4)
110	110	(2)
44	44	(1)
109	109	VBFO FREQ 10 Hz (8)
43	43	(4)
108	108	(2)
42	42	(1)
7	7	NOT USED
8	8	
10	10	
9	9	
3	3	
5	5	
6	6	
4	4	
		NOT USED
18	81	
82	82	PILOT CARRIER ENBL
78	78	PA L PWR ENBL
14	14	PA HV ENBL
79	79	PA LV ENBL
	103	COMMAND (C)
	38	STATUS REQUEST (S)
		NOT USED
92 (68)	68	REMOTE KEY (MON)
		NOT USED
(2)	2	AFC LOCK
(40)	40	EXCTR RF MON
	105	CHAN A XMT AF MON
	36	CHAN A RCV AF MON
	83	CHAN A AGC MON
	39	CHAN B XMT MON
	101	CHAN B RCV MON
	18	CHAN B AGC MON
(69)	69	PA RDY
(77)	4	PA FLT
(5)	5	PA RF MON
(13)	70	CPLR FLT
(67)	67	RF OVLD FLT
	49	SYNTH FLT
	86	PS FLT
(12)	3	RCVR/EXCTR FLT
(70)		NOT USED
(104)		NOT USED
(27)	7	VBFO SYNTH FLT
(92)		NOT USED
(28)	71	PRESEL FLT
(29)	95	DATA ERROR
(95)	16	LOCAL CONTROL
(30	80	MONITOR

EQUIPMENT TYP

85IS-1/2, HF-8095

PARALLEL OUTPUT PIN NO.	PARALLEL INPUT PIN NO.	FUNCTION
	103	COMMAND (C)
	38	STATUS REQUEST (S)
		NOT USED
107	107	VBFO SIGN
48	48	VBFO FREQ 1 kHz (8)
113	113	(4)
47	47	(2)
112	112	(1)
46	46	VBFO FREQ 100 Hz (8)
111	111	(4)
110	110	(2)
44	44	(1)
109	109	VBFO FREQ 10 Hz (8)
43	43	(4)
108	108	(2)
42	42	(1)
7	7	NOT USED
8	8	
10	10	
9	9	
3	3	
5	5	
6	6	
4	4	
		NOT USED
18	81	
82	82	VBFO TUNE
78	78	VBFO PARALLEL ENBL
14	14	FINE TUNE
79	79	RESERVED
	103	COMMAND (C)
	38	STATUS REQUEST (S)
27	105	UP/DOWN
92	68	TUNE RATE (16)
28	4	(8)
29	39	(4)
95	5	(2)
30	70	(1)
(2)	2	NOT USED
(40)	40	NOT USED
	105	NOT USED
	36	CHAN A AF MON
	83	CHAN A AGC MON
	39	NOT USED
	101	CHAN B AF MON
	18	CHAN B AGC MON
(69)	69	NOT USED
(77)	4	
(5)	5	
(13)	70	
(67)	67	RF OVLD FLT
	49	SYNTH
	86	PS FLT
(12)	3	RCVR FLT
(70)		NOT USED
(104)		NOT USED
(27)	7	VBFO SYNTH FLT
(92)		NOT USED
(28)	71	PRESEL FLT
(29)	95	DATA ERROR
(95)	16	LOCAL CONTROL
(30)	80	MONITOR

EQUIPMENT TYPE

85IS-1/2, HF-8095			4-CHANNEL EXCITER, AND 4-CHANNEL EXCITER, CONTROL			4-CHANNEL RECEIVER, AND 4-CHANNEL RECEIVER CONTROL		
PARALLEL OUTPUT PIN NO.	PARALLEL INPUT PIN NO.	FUNCTION	PARALLEL OUTPUT PIN NO.	PARALLEL INPUT PIN NO.	FUNCTION	PARALLEL OUTPUT PIN NO.	PARALLEL INPUT PIN NO.	FUNCTION
	103	COMMAND (C)			NOT USED			NOT USED
	38	STATUS REQUEST (S)						NOT USED
		NOT USED						NOT USED
107	107	VBFO SIGN	107	107		107	107	VBFO SIGN
48	48	VBFO FREQ 1 kHz (8)	48	48		48	48	VBFO FREQ 1 kHz (8)
113	113	(4)	113	113		113	113	(4)
47	47	(2)	47	47		47	47	(2)
112	112	(1)	112	112		112	112	(1)
46	46	VBFO FREQ 100 Hz (8)			NOT USED	46	46	VBFO FREQ 100 Hz (8)
111	111	(4)				111	111	(4)
110	110	(2)				110	110	(2)
44	44	(1)				44	44	(1)
109	109	VBFO FREQ 10 Hz (8)				109	109	VBFO FREQ 10 Hz (8)
43	43	(4)				43	43	(4)
108	108	(2)				108	108	(2)
42	42	(1)				42	42	(1)
7	7	NOT USED	7	7	NOT USED	7	7	NOT USED
8	8		8	8		8	8	
10	10		10	10		10	10	
9	9		9	9		9	9	
3	3		3	3		3	3	
5	5		5	5		5	5	
6	6		6	6		6	6	
4	4		4	4		4	4	
		NOT USED			NOT USED			NOT USED
18	81		18	81		18	81	
82	82	VBFO TUNE	82	82	PILOT CARRIER ENBL	82	82	B2 AGC BUS
78	78	VBFO PARALLEL ENBL	78	78	PA LO PWR ENBL	78	78	B1 AGC BUS
14	14	FINE TUNE	14	14	PA HV ENBL	14	14	A1 AGC BUS
79	79	RESERVED	79	79	PA LV ENBL	79	79	A2 AGC BUS
	103	COMMAND (C)			NOT USED			NOT USED
	38	STATUS REQUEST (S)			NOT USED			NOT USED
27	105	UP/DOWN	(12)	13	EXCTR FLT	(12)	13	RCVR FLT
92	68	TUNE RATE (16)	92 (68)	68	REMOTE KEY (MON)	92 (68)	68	RF OVLD FLT
28	4	(8)		88	B2 AF MON		88	B2 AF MON
29	39	(4)		23	B1 AF MON		23	B1 AF MON
95	5	(2)		22	A1 AF MON		22	A1 AF MON
30	70	(1)		24	A2 AF MON		24	A2 AF MON
(2)	2	NOT USED	(2)	2	NOT USED	(2)	2	NOT USED
(40)	40	NOT USED	(40)	40	10 Hz LOCK IND	(40)	40	10 Hz LOCK IND
	105	NOT USED		105	100 Hz LOCK IND		105	100 Hz LOCK IND
	36	CHAN A AF MON		36	1 kHz LOCK IND		36	1 kHz LOCK IND
	83	CHAN A AGC MON		83	10 kHz LOCK IND		83	10 kHz LOCK IND
	39	NOT USED		39	100 kHz LOCK IND		39	100 kHz LOCK IND
	101	CHAN B AF MON		101	SYNTH OUT LOCK IND		101	SYNTH OUT LOCK IND
	18	CHAN B AGC MON		18	FREQ REF FLT		18	FREQ REF FLT
(69)	69	NOT USED	(69)	69	NOT USED	(69)	69	NOT USED
(77)	4		(77)	4	SUBCARRIER LOCK FLT	(77)	4	SUBCARRIER LOCK FLT
(5)	5		(5)	5	EXCTR RF MON	(5)	5	VBFO SYNTH FLT
(13)	70		(13)	70	EXCTR PS FLT	(13)	70	RCVR PS FLT
(67)	67	RF OVLD FLT	(67)	67	NOT USED	(67)	67	B2 AGC MON
	49	SYNTH		49	EXT STANDARD		49	B1 AGC MON
	86	PS FLT		86	A1 IF MON		86	A1 AGC MON
(12)	3	RCVR FLT	(105)	3	NOT USED	(105)	3	A2 AGC MON
(70)		NOT USED	(70)	77	PA READY	(70)	77	NOT USED
(104)		NOT USED	(104)	102	PA FLT	(104)	102	EXT STANDARD
(27)	7	VBFO SYNTH FLT	(27)	7	PA RF MON	(27)	7	AFC LOCK MON
(92)		NOT USED	(92)	89	CPLR FLT	(92)	89	RF XLTR MON
(28)	71	PRESEL FLT	(28)	71	PRESEL FLT	(28)	71	PRESEL FLT
(29)	95	DATA ERROR	(29)	95	DATA ERROR	(29)	95	DATA ERROR
(95)	16	LOCAL CONTROL	(95)	16	LOCAL CONTROL	(95)	16	LOCAL CONTROL
(30)	80	MONITOR	(30)	80	MONITOR	(30)	80	MONITOR

634-6910

Parallel Output, Schematic Diagram
Figure 3 (Sheet 6)