Parallel Input (642-3135-001)

Rockwell International

instructions

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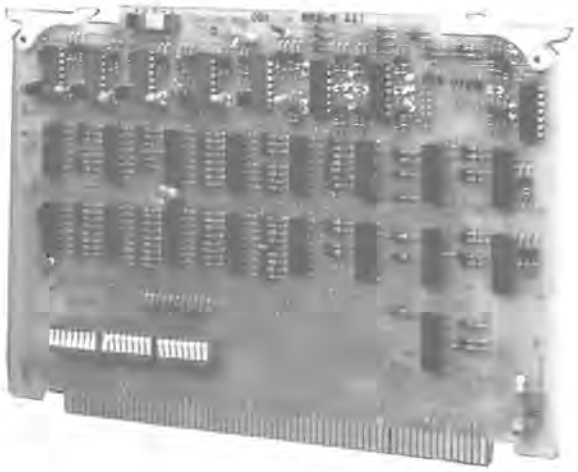
1. DESCRIPTION

Parallel Input 642-3135-001, shown in figure 1, is a 2-layer planar card with a 130-pin (2 layers, 65 pins each) edge-on connector. All test points are mounted at the top edge of the card for easy access with the card installed in the unit.

The parallel input card consists of sixteen 8-channel data selectors (multiplexers), ten multivibrators (gate generators), and three 8-section dip switches.



TPA-2840-017

Parallel Input
Figure 1

2. PRINCIPLES OF OPERATION

2.1 General (Refer to figure 2.)

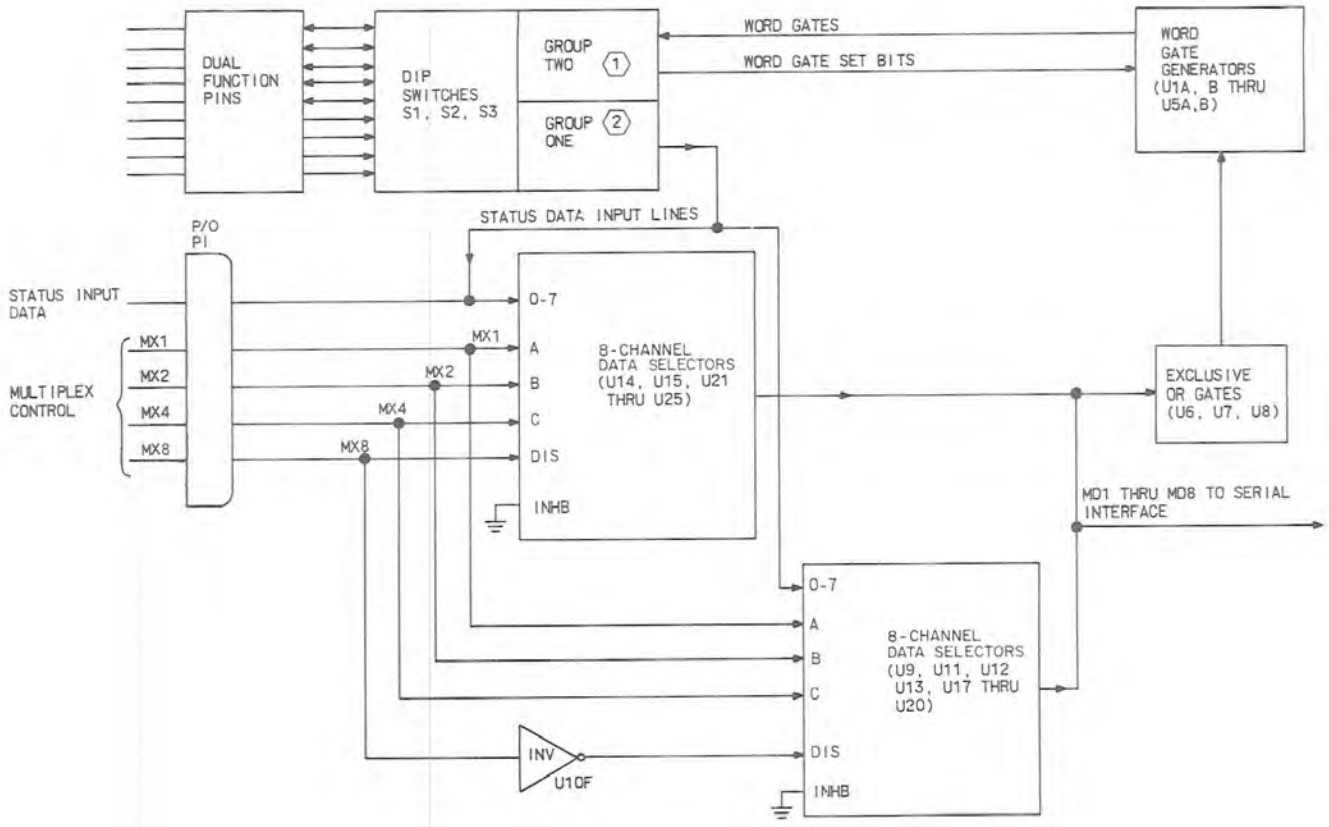
The parallel input card is designed for use in HF-80 four-channel and two-channel equipment. Dip switches S1, S2, and S3 are placed on the card to permit selection of the desired configuration.

The parallel input card consists of two primary circuits: the 8-channel data selectors and the gate generators. Each data selector receives up to eight inputs developed by the unit front-panel controls and monitor circuits. Address bits, from the serial interface card, select individual inputs for transfer to the single output from the data selectors. These address bits are developed from word gate signals produced by the multivibrator circuits when the card is configured for two-channel equipment. When the card is configured for four-channel equipment, the address bits are generated on the serial interface card.

2.2 Multiplexers (Refer to figure 2 and figure 3, the schematic diagram.)

The multiplexers are integrated circuits functioning as 8-channel data selectors. (Refer to table 1 for a truth table of the data selector.) The circuit arrangement is two sections of eight multiplexers each. The MX8 input selects the active section. When at a logic 1 level, the disable input to a multiplexer keeps its output at a high impedance. A logic 0 disable input permits an output to be transferred from one of the eight input lines. MUX 8 is connected to the disable inputs of the first section and inverted by U10F and applied to the disable inputs of the second section to ensure one section is always disabled while the other is enabled.

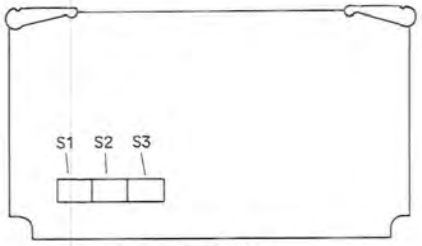
The MX1, MX2, and MX4 inputs, applied simultaneously to all multiplexers, control which of



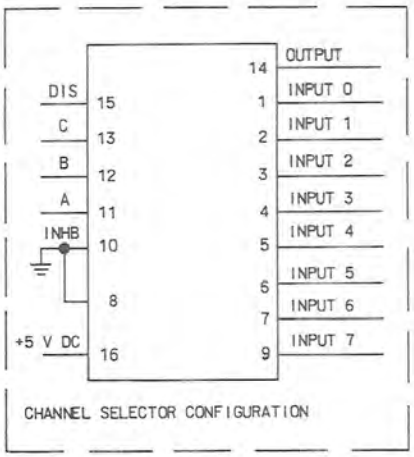
NOTES:

(1) GROUP TWO (S2, SWITCHES 2 THRU 8 AND S3, SWITCHES 1 THRU 8) CLOSED FOR 2-CHANNEL EQUIPMENT. GROUP ONE OPEN.

(2) GROUP ONE (S1, SWITCHES 1 THRU 8, AND S2, SWITCH 1) CLOSED FOR 4-CHANNEL EQUIPMENT. GROUP TWO OPEN.



DIPSWITCH LOCATION



CHANNEL SELECTOR CONFIGURATION

TPA-2623-014

Parallel Input, Block Diagram
Figure 2

the eight input signals (0-7) to each multiplexer is transferred to the output line. (Refer to the truth table of table 1.) The resulting output signals from the eight multiplexers are the eight data bits (MD1 through MD8) of the control word for the unit under control. These data bits are coupled to the serial interface card for parallel-to-serial conversion, word formation, ASCII or 8-bit formatting, and application to the control bus.

2.3 Gate Generators (Refer to figure 2 and figure 3, the schematic diagram.)

When the parallel input card is configured for two-channel equipment and a front-panel control is switched to a different position, a gate signal is developed by one of five gate generators. Each of these generator circuits is two multivibrators connected in series, that develop a single output pulse. The output is a word or address gate signal, determined by the inputs to the exclusive OR gates, and applied to the serial interface card.

An input pulse to the first multivibrator causes an output pulse from that multivibrator of about 0.1-second width which is the input to the second multivibrator. The second circuit does not trigger until the end (1-to-0 transition) of the first output pulse. This delay gives time for switch settling into the final position selected.

The output from the second multivibrator is a 0.1-millisecond pulse for the word gates and a 10-microsecond pulse for the address gate.

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the parallel input card are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in tables 2 and 3 check the total performance of the parallel input card. The procedures in table 2 are for the following equipments:

HF-8010/8010A Exciter
HF-8050/8050A Receiver
HF-8070/8070A Receiver-Exciter
851S Receiver
HF-8090, HF-8091, HF-8092, and HF-8095 Controls.

The procedures in table 3 are for the following equipments:

HF-8014/8014A Exciter
HF-8054/8054A Receiver
HF-8093 and HF-8094 Controls.

These procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic diagram to trace the source of the fault.

Table 1. 8-Channel Data Selector Truth Table.

C	B	A	INHIBIT	DISABLE	OUTPUT
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
M	M	M	1	0	0
M	M	M	M	1	HIGH IMPED-ANCE

X = transfer to output

M = don't care

Table 2. Parallel Input, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	***Note***		
	The testing and troubleshooting procedures herein are for 1- or 2-channel configurations of the HF-8010/8010A, HF-8050/8050A, HF-8070/ 8070A, 851S, HF-8090, HF-8091, HF-8092, and HF-8095.		
	These testing and troubleshooting procedures are based on using a control unit and an associated local unit. The most effective method of testing and troubleshooting is obtained by installing the questionable parallel input in the control unit.		
	During these tests when a control unit is referred to it is a receiver-exciter control, an exciter control, or a receiver control. When a local unit is referred to it is a receiver-exciter, an exciter, or a receiver.		
	a. Remove top cover of unit containing parallel input to be tested.		
	b. Remove parallel input.		
	c. Set the dip switches for two-channel operation. (Group 1 open, group 2 closed). Refer to figure 2 for dip switch location.		
	d. Place the parallel input card on the card extender and place it in the unit.		
(Cont)	e. Set control unit and local unit LINE SELECTOR switches to 115 V.		

Table 2. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. (Cont)	f. Connect control unit and local unit to 115-V ac power source and set power on.		
	g. Measure dc voltages, on the card under test, between the following pins and ground (TP1, brown):		
	P1-45 P1-65 P1-114	+15 ±1.0 V dc. +5 ±0.5 V dc. -15 ±1.0 V dc.	
	h. Strap local unit for address 0.		
	i. Connect local unit to control unit.		
2. Word and address gates	a. Connect oscilloscope to TP2 (red).		
	b. Set control unit KEY switch to LOCK and note oscilloscope.	A logic level 1, 100-μs (nominal) pulse.	Check U2A, U2B, U8D, and associated circuit.
	c. Set control unit KEY switch to NORM and note oscilloscope.	Same as step b.	Same as step b.
	d. Connect oscilloscope to TP3 (orange).		
	e. Set control unit PA PWR switch to STBY and note oscilloscope.	A logic level 1, 100-μs (nominal) pulse.	Check U3A, U3B, U10A, S3, and associated circuit.
	f. Set control unit PA PWR switch to OFF and note oscilloscope.	Same as step e.	Same as step e.
	g. Connect oscilloscope to TP 4 (yellow).		
	h. Rotate each control unit FREQUENCY KHZ thumb wheel and note oscilloscope when changing positions.	A logic level 1, 100-μs (nominal) pulse.	Check U1A, U1B, S2 and associated circuit.
	i. Connect oscilloscope to TP5 (green).		
(Cont)	j. Set control unit MODE switch to each mode position and note oscilloscope when changing positions.	A logic level 1, 100-μs (nominal) pulse.	Check U5A, U5B, U6, U7, U10C, S3, and associated circuit.

Table 2. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	k. Connect oscilloscope to P1-88.		
	l. Rotate control unit ADDRESS switch and note oscilloscope when changing positions.	A logic level 1, 100-μs (nominal) pulse.	Check U4A, U4B, S3 and associated circuit.
	m. Connect +5-V dc input to P1-66.		
	n. Check voltage levels at:		
	TP2	NLT +4.0 V dc.	Check CR1.
	TP3	NLT +4.0 V dc.	Check CR2.
	TP4	NLT +4.0 V dc.	Check CR4.
	TP5	NLT +4.0 V dc.	Check CR3.
	o. Remove +5 V dc from P1-66.		

Note

Tests 3 through 18 are output tests. During all of these tests serial interface card A13 is removed from unit under test and mux inputs are strapped according to word and character being tested. To strap a logic 1 input, connect a 4700-Ω resistor in series between the mux input pin and +5 V dc. To strap a logic 0 input, connect directly from the mux input pin to ground. See following chart and figure for mux input/output strapping and setup requirements. Where front-panel controls are shown, these controls may be used to apply the appropriate inputs. If they are not used their associated front-panel connector must be disconnected.

MUX CONTROL LINES INPUT STRAPPING				*OUTPUTS PRESENTED BY PARALLEL INPUT CARD									
				WORD NO	CHARACTER NO	OUTPUT BIT NO							
MX8	MX4	MX2	MX1			1	2	3	4	5	6	7	8
P1-93	P1-90	P1-25	P1-27			P1-26	P1-28	P1-29	P1-94	P1-30	P1-31	P1-96	P1-104
0	0	0	0	1	2	P1-62	P1-127	P1-63	P1-128	P1-64	P1-129	P1-38	P1-103
0	0	0	1	1	3	P1-58	P1-123	P1-59	P1-124	P1-60	P1-125	P1-61	P1-126
0	0	1	0	1	4	P1-54	P1-119	P1-55	P1-120	P1-56	P1-121	P1-57	P1-122
0	0	1	1	1	5	P1-50	P1-115	P1-51	P1-116	P1-52	P1-117	P1-53	P1-118
0	1	0	0	2	2	P1-87	P1-10	P1-75	P1-11	P1-76	NA	NA	NA
0	1	0	1	2	3	P1-20	P1-19	P1-85	P1-84	P1-37	P1-106	P1-41	NA

*Outputs presented at the bit no pins are the inputs at the bit no pins associated with the word no/character no.

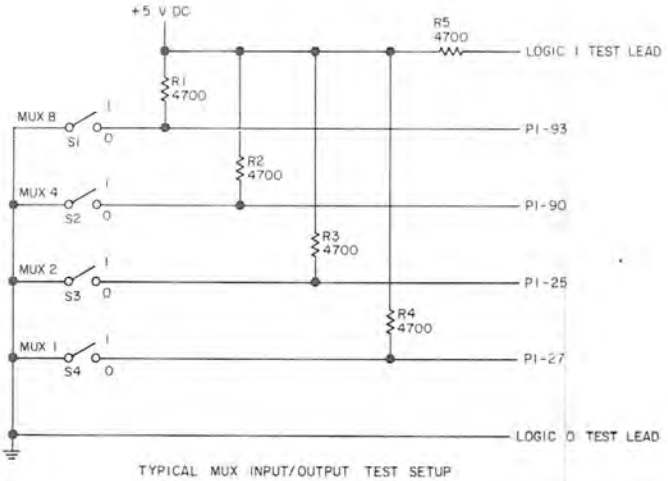
(Cont)

Table 2. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)			

MUX CONTROL LINES INPUT STRAPPING				*OUTPUTS PRESENTED BY PARALLEL INPUT CARD									
				WORD NO	CHARACTER NO	OUTPUT BIT NO							
MX8	MX4	MX2	MX1			1	2	3	4	5	6	7	8
P1-93	P1-90	P1-25	P1-27			P1-26	P1-28	P1-29	P1-94	P1-30	P1-31	P1-96	P1-104
0	1	1	0	2	4	P1-32	P1-97	P1-33	P1-98	P1-34	P1-35	P1-99	P1-100
0	1	1	1	2	5	P1-21	P1-91	P1-92	P1-74	P1-9	P1-72	P1-8	P1-73
1	0	0	0	3	2	P1-112	P1-47	P1-113	P1-48	P1-107	NA	NA	NA
1	0	0	1	3	3	P1-42	P1-108	P1-43	P1-109	P1-44	P1-110	P1-111	P1-46
1	0	1	0	3	4	NA	NA	NA	NA	NA	NA	NA	NA
1	0	1	1	3	5	P1-79	P1-14	P1-78	P1-82	P1-81	NA	NA	NA
1	1	0	0	4	2	NA	NA	NA	NA	P1-68	NA	NA	NA
1	1	0	1	4	3	P1-18	P1-101	P1-39	P1-83	P1-36	P1-105	P1-40	P1-2
1	1	1	0	4	4	P1-3	P1-86	P1-49	P1-67	P1-70	P1-5	P1-4	P1-69
1	1	1	1	4	5	P1-80	P1-16	P1-95	P1-71	NA	NA	NA	NA

*Outputs presented at the bit no pins are the inputs at the bit no pins associated with the word no/character no.



TYPICAL MUX INPUT/OUTPUT TEST SETUP

TP5-4247-013

Table 2. Parallel Input, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>3. Word 1, character 2 outputs</td><td>a. Strap mux control lines for word 1, character 2.

b. Apply logic 1 inputs at inputs associated with word 1, character 2 (see chart).

Note

FREQUENCY KHZ switches apply logic 1 inputs in the positions indicated in the chart. In the 0 position these switches apply logic 0 inputs.

c. Apply logic 0 inputs at inputs associated with word 1, character 2 (see chart).</td><td>

Verify that associated outputs are at logic 1.

Verify that associated outputs are at logic 0.</td><td></td></tr>
<tr><td colspan="4">
<table>
<tr><th>FRONT-PANEL CONTROL</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>1 MHz 1</td><td>1</td><td>62</td><td>26</td><td>U25, U18</td></tr>
<tr><td>1 MHz 2</td><td>2</td><td>127</td><td>28</td><td>U15, U19</td></tr>
<tr><td>1 MHz 4</td><td>3</td><td>63</td><td>29</td><td>U23, U20</td></tr>
<tr><td>1 MHz 8</td><td>4</td><td>128</td><td>94</td><td>U21, U17</td></tr>
<tr><td>10 MHz 1</td><td>5</td><td>64</td><td>30</td><td>U24, U11</td></tr>
<tr><td>10 MHz 2</td><td>6</td><td>129</td><td>31</td><td>U16, U13</td></tr>
<tr><td>NA</td><td>7</td><td>38</td><td>96</td><td>U22, U12</td></tr>
<tr><td>NA</td><td>8</td><td>103</td><td>104</td><td>U14, R42, U9</td></tr>
</table>
</td></tr>
<tr><td>4. Word 1, character 3 outputs

(Cont)</td><td>a. Strap mux control lines for word 1, character 3.

b. Apply logic 1 inputs at inputs associated with word 1, character 3 (see chart).

Note

FREQUENCY KHZ switches apply logic 1 inputs in the positions indicated in the chart. In the 0 position, these switches apply logic 0 inputs.

c. Apply logic 0 inputs at inputs associated with word 1, character 3 (see chart).</td><td>

Verify that associated outputs are at logic 1.

Verify that associated outputs are at logic 0.</td><td></td></tr>
</table>

Table 2. Parallel Input, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>4. (Cont)</td><td colspan="3">
<table>
<tr><th>FRONT-PANEL CONTROL</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>10 kHz 1</td><td>1</td><td>58</td><td>26</td><td>U25, U18</td></tr>
<tr><td>10 kHz 2</td><td>2</td><td>123</td><td>28</td><td>U15, U19</td></tr>
<tr><td>10 kHz 4</td><td>3</td><td>59</td><td>29</td><td>U23, U20</td></tr>
<tr><td>10 kHz 8</td><td>4</td><td>124</td><td>94</td><td>U21, U17</td></tr>
<tr><td>100 kHz 1</td><td>5</td><td>60</td><td>30</td><td>U24, U11</td></tr>
<tr><td>100 kHz 2</td><td>6</td><td>125</td><td>31</td><td>U16, U13</td></tr>
<tr><td>100 kHz 4</td><td>7</td><td>61</td><td>96</td><td>U22, U12</td></tr>
<tr><td>100 kHz 8</td><td>8</td><td>126</td><td>104</td><td>U14, U9</td></tr>
</table>
</td></tr>
<tr><td>5. Word 1, character 4 outputs</td><td colspan="3">
a. Strap mux control lines for word 1, character 4.

b. Apply logic 1 inputs at inputs associated with word 1, character 4 (see chart). — Verify that associated outputs are at logic 1.

Note

FREQUENCY KHZ switches apply logic 1 inputs in the positions indicated in the chart. In the 0 position, these switches apply logic 0 inputs.

c. Apply logic 0 inputs at inputs associated with word 1, character 4 (see chart). — Verify that associated outputs are at logic 0.

<table>
<tr><th>FRONT-PANEL CONTROL</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>100 Hz 1</td><td>1</td><td>54</td><td>26</td><td>U25, U18</td></tr>
<tr><td>100 Hz 2</td><td>2</td><td>119</td><td>28</td><td>U15, U19</td></tr>
<tr><td>100 Hz 4</td><td>3</td><td>55</td><td>29</td><td>U23, U20</td></tr>
<tr><td>100 Hz 8</td><td>4</td><td>120</td><td>94</td><td>U21, U17</td></tr>
<tr><td>1 kHz 1</td><td>5</td><td>56</td><td>30</td><td>U24, U11</td></tr>
<tr><td>1 kHz 2</td><td>6</td><td>121</td><td>31</td><td>U16, U13</td></tr>
<tr><td>1 kHz 4</td><td>7</td><td>57</td><td>96</td><td>U22, U12</td></tr>
<tr><td>1 kHz 8</td><td>8</td><td>122</td><td>104</td><td>U14, U9</td></tr>
</table>
</td></tr>
</table>

Table 2. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
6. Word 1, character 5 outputs	a. Strap mux control lines for word 1, character 5.		
	b. Apply logic 1 inputs at inputs associated with word 1, character 5 (see chart). **Note** FREQUENCY KHZ switches apply logic 1 inputs in the positions indicated in the chart. In the 0 position, these switches apply logic 0 inputs.	Verify that associated outputs are at logic 1.	
	c. Apply logic 0 inputs at inputs associated with word 1, character 5 (see chart).	Verify that associated outputs are at logic 0.	

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	50	26	U25, R68, U18
NA	2	115	28	U15, R64, U19
NA	3	51	29	U23, R60, U20
NA	4	116	94	U21, R56, U17
*10 Hz 1	5	52	30	U24, R52, U11
*10 Hz 2	6	117	31	U16, R49, U13
*10 Hz 4	7	53	96	U22, R46, U12
*10 Hz 8	8	118	104	U14, R43, U9

*Applicable only with 10-Hz front-panel tuning.

7. Word 2, character 2 outputs (Cont)	a. Strap mux control lines for word 2, character 2.	**Note** Grounded input as noted in chart will always be logic 0 output.	
	b. Apply logic 1 inputs at inputs associated with word 2, character 2 (see chart).	Verify that associated outputs are at logic 1.	

Table 2. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
7. (Cont)	***Note*** RF GAIN switch applies logic 1 input in the position indicated in the chart (positions read as MAX minus X number of positions). In the MAX position, this switch applies logic 0 inputs. c. Apply logic 0 inputs at inputs associated with word 2, character 2 (see chart).	Verify that associated outputs are at logic 0.	

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	87	26	U25, R69, U18
RF GAIN MAX-1	2	10	28	U15, R65, U19
RF GAIN MAX-2	3	75	29	U23, R61, U20
RF GAIN MAX-4	4	11	94	U21, R57, U17
RF GAIN MAX-8	5	76	30	U24, R53, U11
NA	6	*	31	U16, U13
NA	7	38	96	U22, U12
NA	8	103	104	U14, R42, U9

*Grounded input.

8. Word 2, character 3 outputs	a. Strap mux control lines for word 2, character 3.	***Note*** Grounded input as noted in chart will always be logic 0 output.	
	b. Apply logic 1 inputs at inputs associated with word 2, character 3 (see chart). ***Note*** AGC switch applies logic 1 input in the position indicated in the chart. In the AGC-SLOW position, this switch applies logic 0 inputs.	Verify that associated ouputs are at logic 1.	
(Cont)	c. Apply logic 0 inputs at inputs associated with word 2, character 3 (see chart).	Verify that associated outputs are at logic 0.	

Table 2. Parallel Input, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>8. (Cont)</td><td colspan="3">
<table>
<tr><th>FRONT-PANEL CONTROL</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>AGC-FAST (B)</td><td>1</td><td>20</td><td>26</td><td>U25, U18</td></tr>
<tr><td>AGC-OFF (B)</td><td>2</td><td>19</td><td>28</td><td>U15, U19</td></tr>
<tr><td>AGC-FAST (A)</td><td>3</td><td>85</td><td>29</td><td>U23, U20</td></tr>
<tr><td>AGC-OFF (A)</td><td>4</td><td>84</td><td>94</td><td>U21, U17</td></tr>
<tr><td>NA</td><td>5</td><td>37</td><td>30</td><td>U24, U11</td></tr>
<tr><td>NA</td><td>6</td><td>106</td><td>31</td><td>U16, U13</td></tr>
<tr><td>NA</td><td>7</td><td>41</td><td>96</td><td>U22, U12</td></tr>
<tr><td>NA</td><td>8</td><td>*</td><td>104</td><td>U14, U9</td></tr>
<tr><td colspan="5">*Grounded input.</td></tr>
</table>
</td></tr>
<tr><td>9. Word 2, character 4 outputs</td><td colspan="3">
a. Strap mux control lines for word 2, character 4.

b. Apply logic 1 inputs at inputs associated with word 2, character 4 (see chart).

Note

MODE switch and/or BANDWIDTH switch applies logic 1 input in the position indicated in the chart. In the LSB position, the MODE switch applies logic 0 inputs.

c. Apply logic 0 inputs at inputs associated with word 2, character 4 (see chart).

<table>
<tr><th>FRONT-PANEL CONTROL (MODE)</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>SSB/CW-USB or USB</td><td>1</td><td>32</td><td>26</td><td>U25, R70, U18</td></tr>
<tr><td>SSB/CW-LSB or LSB</td><td>2</td><td>97</td><td>28</td><td>U15, R66, U19</td></tr>
<tr><td>*SSB/CW-A</td><td>3</td><td>33</td><td>29</td><td>U23, R62, U20</td></tr>
<tr><td>*SSB/CW-B</td><td>4</td><td>98</td><td>94</td><td>U21, R58, U17</td></tr>
<tr><td>*SSB/CW-C</td><td>5</td><td>34</td><td>30</td><td>U24, R54, U11</td></tr>
<tr><td>*SSB/CW-D</td><td>6</td><td>35</td><td>31</td><td>U16, R50, U13</td></tr>
<tr><td>*SSB/CW-E</td><td>7</td><td>99</td><td>96</td><td>U22, R47, U12</td></tr>
<tr><td>*SSB/CW-16</td><td>8</td><td>100</td><td>104</td><td>U14, R44, U9</td></tr>
<tr><td colspan="5">*SSB/CW applicable only on receiver control.</td></tr>
</table>
</td><td>Verify that associated outputs are at logic 1.

Verify that associated outputs are at logic 0.</td><td></td></tr>
</table>

Table 2. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
10. Word 2, character 5 outputs	a. Strap mux control lines for word 2, character 5.		
	b. Apply logic 1 inputs at inputs associated with word 2, character 5 (see chart). *Note* MODE switch applies logic 1 input in the position indicated in the chart. In any other position, the MODE switch applies logic 0 input.	Verify that associated outputs are at logic 1.	
	c. Apply logic 0 inputs at inputs associated with word 2, character 5 (see chart).	Verify that associated outputs are at logic 0.	

FRONT-PANEL CONTROL (MODE)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	21	26	U25, R71, U18
NA	2	91	28	U15, R67, U19
NA	3	92	29	U23, R63, U20
ISB	4	74	94	U21, R59, U17
*CW	5	9	30	U24, R55, U11
CW, LSB, USB, ISB, or SSB/CW	6	72	31	U16, R51, U13
AM	7	8	96	U22, R48, U12
NA	8	73	104	U14, R45, U9

*CW applicable only on exciter control and receiver-exciter control.

11. Word 3, character 2 outputs (Cont)	a. Strap mux control lines for word 3, character 2.	*Note* Grounded input as noted in chart will always be logic 0 output.	
	b. Apply logic 1 inputs at inputs associated with word 3, character 2 (see chart).	Verify that associated outputs are at logic 1.	
	c. Apply logic 0 inputs at inputs associated with word 3, character 2 (see chart).	Verify that associated outputs are at logic 0.	

Table 2. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL

11. (Cont)

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	112	26	U18, R103, U25
NA	2	47	28	U19, R97, R15
NA	3	113	29	U20, R91, U23
NA	4	48	94	U17, R86, U21
NA	5	107	30	U11, R81, U24
NA	6	*	31	U13, U16
NA	7	38	96	U12, U22
NA	8	103	104	U9, R42, U14

*Grounded input.

12. Word 3, character 3 outputs

a. Strap mux control lines for word 3, character 3.

b. Apply logic 1 inputs at inputs associated with word 3, character 3 (see chart). — Verify that associated outputs are at logic 1.

c. Apply logic 0 inputs at inputs associated with word 3, character 3 (see chart). — Verify that associated outputs are at logic 0.

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	42	26	U18, R104, U25
NA	2	108	28	U19, R98, U15
NA	3	43	29	U20, R92, U23
NA	4	109	94	U17, R87, U21
NA	5	44	30	U11, R82, U24
NA	6	110	31	U13, R78, U16
NA	7	111	96	U12, R75, U22
NA	8	46	104	U9, R72, U14

Table 2. Parallel Input, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>13. Word 3, character 4 outputs</td><td>a. Strap mux control lines for word 3, character 4.</td><td>Note
Grounded input as noted in chart will always be logic 0 output.

Verify that all associated outputs are at logic 0.</td><td></td></tr>
<tr><td colspan="4">
<table>
<tr><th>FRONT-PANEL CONTROL</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>NA</td><td>1</td><td>*</td><td>26</td><td>U18, U25</td></tr>
<tr><td>NA</td><td>2</td><td>*</td><td>28</td><td>U19, U15</td></tr>
<tr><td>NA</td><td>3</td><td>*</td><td>29</td><td>U20, U23</td></tr>
<tr><td>NA</td><td>4</td><td>*</td><td>94</td><td>U17, U21</td></tr>
<tr><td>NA</td><td>5</td><td>*</td><td>30</td><td>U11, U24</td></tr>
<tr><td>NA</td><td>6</td><td>*</td><td>31</td><td>U13, U16</td></tr>
<tr><td>NA</td><td>7</td><td>*</td><td>96</td><td>U12, U22</td></tr>
<tr><td>NA</td><td>8</td><td>*</td><td>104</td><td>U9, U14</td></tr>
<tr><td colspan="5">*Grounded input.</td></tr>
</table>
</td></tr>
<tr><td>14. Word 3, character 5 outputs

(Cont)</td><td>a. Strap mux control lines for word 3, character 5.

b. Apply logic 1 inputs at inputs associated with word 3, character 5 (see chart).

Note
PA PWR and P CAR switches apply logic 1 inputs in the positions indicated in the chart. In the OFF positions these switches apply logic 0 inputs.

c. Apply logic 0 inputs at inputs associated with word 3, character 5 (see chart).</td><td>Note
Grounded input as noted in chart will always be logic 0 output.

Verify that associated outputs are at logic 1.

Verify that associated outputs are at logic 0.</td><td></td></tr>
</table>

Table 2. Parallel Input, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>14. (Cont)</td><td colspan="3">
<table>
<tr><th>FRONT-PANEL CONTROL</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>PA PWR-STBY</td><td>1</td><td>79</td><td>26</td><td>U18, R105, U25</td></tr>
<tr><td>PA PWR-HIGH PWR</td><td>2</td><td>14</td><td>28</td><td>U19, R99, U15</td></tr>
<tr><td>PA PWR-LOW PWR</td><td>3</td><td>78</td><td>29</td><td>U20, R93, U23</td></tr>
<tr><td>P CAR-ON</td><td>4</td><td>82</td><td>94</td><td>U17, R8, U21</td></tr>
<tr><td>NA</td><td>5</td><td>81</td><td>30</td><td>U11, R83, U24</td></tr>
<tr><td>NA</td><td>6</td><td>*</td><td>31</td><td>U13, U16</td></tr>
<tr><td>NA</td><td>7</td><td>*</td><td>96</td><td>U12, U22</td></tr>
<tr><td>NA</td><td>8</td><td>*</td><td>104</td><td>U9, U14</td></tr>
<tr><td colspan="5">*Grounded input.</td></tr>
</table>
</td></tr>
<tr><td>15. Word 4, character 2 outputs

(Cont)</td><td>a. Strap mux control lines for word 4, character 2.

b. Apply logic 1 inputs at inputs associated with word 4, character 2 (see chart).

Note
KEY switch in the LOCK position applies a logic 1 input and in the NORM position applies a logic 0 input.

c. Apply logic 0 inputs at inputs associated with word 4, character 2 (see chart).</td><td>Note
Grounded input as noted in chart will always be logic 0 output.

Verify that associated outputs are at logic 1.

Verify that associated outputs are at logic 0.</td><td></td></tr>
</table>

Table 2. Parallel Input, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>15. (Cont)</td><td>
<table>
<tr><th>FRONT-PANEL CONTROL</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>NA</td><td>1</td><td>*</td><td>26</td><td>U18, U25</td></tr>
<tr><td>NA</td><td>2</td><td>*</td><td>28</td><td>U19, U15</td></tr>
<tr><td>NA</td><td>3</td><td>*</td><td>29</td><td>U20, U23</td></tr>
<tr><td>NA</td><td>4</td><td>*</td><td>94</td><td>U17, U21</td></tr>
<tr><td>KEY-LOCK</td><td>5</td><td>68</td><td>30</td><td>U11, R12, U24</td></tr>
<tr><td>NA</td><td>6</td><td>*</td><td>31</td><td>U13, U16</td></tr>
<tr><td>NA</td><td>7</td><td>38</td><td>96</td><td>U12, U22</td></tr>
<tr><td>NA</td><td>8</td><td>103</td><td>104</td><td>U9, R42, U14</td></tr>
<tr><td colspan="5">*Grounded input.</td></tr>
</table>
</td><td></td><td></td></tr>
<tr><td>16. Word 4, character 3 outputs</td><td>a. Strap mux control lines for word 4, character 3.

b. Apply logic 1 inputs at inputs associated with word 4, character 3 (see chart).

c. Apply logic 0 inputs at inputs associated with word 4, character 3 (see chart).

<table>
<tr><th>FRONT-PANEL CONTROL</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>NA</td><td>1</td><td>18</td><td>26</td><td>U18, R106, U25</td></tr>
<tr><td>NA</td><td>2</td><td>101</td><td>28</td><td>U19, R100, U15</td></tr>
<tr><td>NA</td><td>3</td><td>39</td><td>29</td><td>U20, R94, U23</td></tr>
<tr><td>NA</td><td>4</td><td>83</td><td>94</td><td>U17, R88, U21</td></tr>
<tr><td>NA</td><td>5</td><td>36</td><td>30</td><td>U11, R84, U24</td></tr>
<tr><td>NA</td><td>6</td><td>105</td><td>31</td><td>U13, R79, U16</td></tr>
<tr><td>NA</td><td>7</td><td>40</td><td>96</td><td>U12, R76, U22</td></tr>
<tr><td>NA</td><td>8</td><td>2</td><td>104</td><td>U9, R73, U14</td></tr>
</table>
</td><td>Verify that associated outputs are at logic 1.

Verify that associated outputs are at logic 0.</td><td></td></tr>
</table>

Table 2. Parallel Input, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>17. Word 4, character 4 outputs</td><td>a. Strap mux control lines for word 4, character 4.
b. Apply logic 1 inputs at inputs associated with word 4, character 4 (see chart).
c. Apply logic 0 inputs at inputs associated with word 4, character 4 (see chart).</td><td>
Verify that associated outputs are at logic 1.
Verify that associated outputs are at logic 0.</td><td></td></tr>
<tr><td colspan="4"><table>
<tr><th>FRONT-PANEL CONTROL</th><th>BIT NO</th><th>INPUTS P1-( )</th><th>OUTPUTS P1-( )</th><th>IF ABNORMAL CHECK</th></tr>
<tr><td>NA</td><td>1</td><td>3</td><td>26</td><td>U18, R107, U25</td></tr>
<tr><td>NA</td><td>2</td><td>86</td><td>28</td><td>U19, R101, U15</td></tr>
<tr><td>NA</td><td>3</td><td>49</td><td>29</td><td>U20, R95, U23</td></tr>
<tr><td>NA</td><td>4</td><td>67</td><td>94</td><td>U17, R89, U21</td></tr>
<tr><td>NA</td><td>5</td><td>70</td><td>30</td><td>U11, R85, U24</td></tr>
<tr><td>NA</td><td>6</td><td>5</td><td>31</td><td>U13, R80, U16</td></tr>
<tr><td>NA</td><td>7</td><td>4</td><td>96</td><td>U12, R77, U22</td></tr>
<tr><td>NA</td><td>8</td><td>69</td><td>104</td><td>U9, R74, U14</td></tr>
</table></td></tr>
<tr><td>18. Word 4, character 5 outputs

(Cont)</td><td>a. Strap mux control lines for word 4, character 5.
b. Apply logic 1 inputs at inputs associated with word 4, character 5 (see chart).
c. Apply logic 0 inputs at inputs associated with word 4, character 5 (see chart).</td><td>Note
Grounded input as noted in chart will always be logic 0 output.
Verify that associated outputs are at logic 1.
Verify that associated outputs are at logic 0.</td><td></td></tr>
</table>

Table 2. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
18. (Cont)			

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	80	26	U18, R108, U25
NA	2	16	28	U19, R102, CR24, C28, U15
NA	3	95	29	U20, R96, U23
NA	4	71	94	U17, R90, U21
NA	5	*	30	U11, U24
NA	6	*	31	U13, U16
NA	7	*	96	U12, U22
NA	8	*	104	U9, U14

*Grounded input.

Table 3. Parallel Input, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	***Note*** The testing and troubleshooting procedures herein are for 1-, 2-, 3-, or 4-channel configurations of the HF-8014/8014A, HF-8054/8054A, HF-8093, and HF-8094. These testing and troubleshooting procedures are based on using a control unit and an associated local unit. The most effective method of testing and troubleshooting is obtained by installing the questionable parallel input in the control unit. During these tests when a control unit is referred to it is an exciter control, or a receiver control. When a local unit is referred to it is a receiver-exciter, an exciter, or a receiver. a. Remove top cover of unit containing parallel input to be tested. b. Remove parallel input. c. Set the dip switches for four-channel operation. (Group 1 closed, group 2 open.) Refer to figure 2 for dip switch location. d. Place the parallel input card on the card extender and place it in the unit. e. Set control unit and local unit LINE SELECTOR switches to 115 V. f. Connect control unit and local unit to 115-V ac power source and set power on.		
(Cont)			

Table 3. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. (Cont)	g. Measure dc voltages, on the card under test, between the following pins and ground (TP1, brown):		
	P1-45 P1-65 P1-114	+15 ± 1.0 V dc. +5 ±0.5 V dc. -15 ±1.0 V dc.	
	h. Strap local unit for address 0.		
	i. Connect local unit to control unit.		

Note

Tests 2 through 17 are output tests. During all of these tests serial interface card A13 is removed from unit uder test and mux inputs are strapped according to word and character being tested. To strap a logic 1 input, connect a 4700-Ω resistor in series between the mux input pin and +5 V dc. To strap a logic 0 input, connect directly from the mux input pin to ground. See following chart and figure for mux input/output strapping and setup requirements. Where front-panel controls are shown, these controls may be used to apply the appropriate inputs. If they are not used their associated front-panel connector must be disconnected. Signal names are given in parentheses ( ) where there is not a front-panel control.

MUX CONTROL LINES INPUT STRAPPING				*OUTPUTS PRESENTED BY PARALLEL INPUT CARD								
				WORD NO	CHARACTER NO	OUTPUT BIT NO						
MX8	MX4	MX2	MX1			1	2	3	4	5	6	7	8
P1-93	P1-90	P1-25	P1-27			P1-26	P1-28	P1-29	P1-94	P1-30	P1-31	P1-96	P1-104
0	0	0	0	1	2	P1-62	P1-127	P1-63	P1-128	P1-64	P1-129	P1-38	P1-103
0	0	0	1	1	3	P1-58	P1-123	P1-59	P1-124	P1-60	P1-125	P1-61	P1-126
0	0	1	0	1	4	P1-54	P1-119	P1-55	P1-120	P1-56	P1-121	P1-57	P1-122
0	0	1	1	1	5	P1-50	P1-115	P1-51	P1-116	P1-52	P1-117	P1-53	P1-118
0	1	0	0	2	2	P1-87	P1-10	P1-75	P1-11	P1-76	NA	NA	NA
0	1	0	1	2	3	P1-20	P1-19	P1-85	P1-84	P1-37	P1-106	P1-41	P1-12

*Outputs presented at the bit no pins are the inputs at the bit no pins associated with the word no/character no.

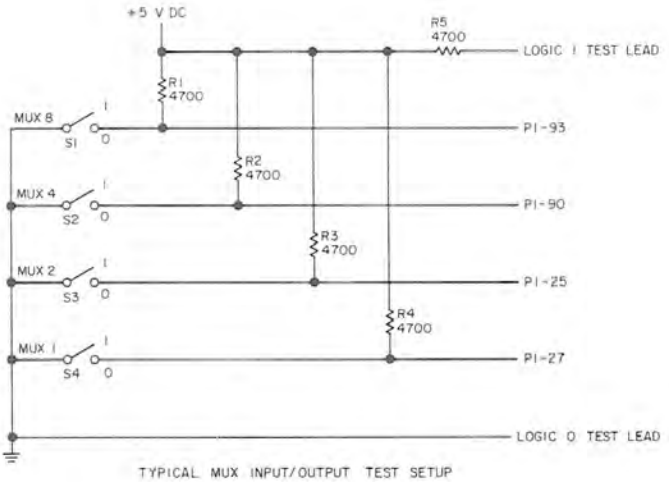
(Cont)			

Table 3. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. (Cont)			

MUX CONTROL LINES INPUT STRAPPING				*OUTPUTS PRESENTED BY PARALLEL INPUT CARD									
				WORD NO	CHARACTER NO	OUTPUT BIT NO							
MX8	MX4	MX2	MX1			1	2	3	4	5	6	7	8
P1-93	P1-90	P1-25	P1-27			P1-26	P1-28	P1-29	P1-94	P1-30	P1-31	P1-96	P1-104
0	1	1	0	2	4	P1-32	P1-97	P1-33	P1-98	P1-34	P1-35	P1-99	P1-100
0	1	1	1	2	5	P1-21	P1-91	P1-92	P1-74	P1-9	P1-72	P1-8	P1-73
1	0	0	0	3	2	P1-112	P1-47	P1-113	P1-48	P1-107	NA	NA	NA
1	0	0	1	3	3	P1-42	P1-108	P1-43	P1-109	P1-44	P1-110	P1-111	P1-46
1	0	1	0	3	4	P2-4	P2-6	P2-5	P2-3	P2-9	P2-10	P2-8	P2-7
1	0	1	1	3	5	P1-79	P1-14	P1-78	P1-82	P1-81	NA	NA	NA
1	1	0	0	4	2	P1-24	P1-22	P1-23	P1-88	P1-68	P1-13	NA	NA
1	1	0	1	4	3	P1-18	P1-101	P1-39	P1-83	P1-36	P1-105	P1-40	P1-2
1	1	1	0	4	4	P1-3	P1-86	P1-49	P1-67	P1-70	P1-5	P1-4	P1-69
1	1	1	1	4	5	P1-80	P1-16	P1-95	P1-71	P1-89	P1-7	P1-102	P1-77

*Outputs presented at the bit no pins are the inputs at the bit no pins associated with the word no/character no.



TYPICAL MUX INPUT/OUTPUT TEST SETUP

TP5-4247-013

Table 3. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. Word 1, character 2 outputs	a. Strap mux control lines for word 1, character 2.		
	b. Apply logic 1 inputs at inputs associated with word 1, character 2 (see chart). **Note** FREQUENCY KHZ switches apply logic 1 inputs in the positions indicated in the chart. In the 0 position these switches apply logic 0 inputs.	Verify that associated outputs are at logic 1.	
	c. Apply logic 0 inputs at inputs associated with word 1, character 2 (see chart).	Verify that associated outputs are at logic 0.	

EXCITER FRONT-PANEL CONTROL (SIGNAL)	RECEIVER FRONT-PANEL CONTROL (SIGNAL)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
1 MHz 1	1 MHz 1	1	62	26	U25, U18
1 MHz 2	1 MHz 2	2	127	28	U15, U19
1 MHz 4	1 MHz 4	3	63	29	U23, U20
1 MHz 8	1 MHz 8	4	128	94	U21, U17
10 MHz 1	10 MHz 1	5	64	30	U24, U11
10 MHz 2	10 MHz 2	6	129	31	U16, U13
NA	NA	7	38	96	U22, U12
NA	NA	8	103	104	U14, R42, U9

3. Word 1, character 3 outputs	a. Strap mux control lines for word 1, character 3.		
	b. Apply logic 1 inputs at inputs associated with word 1, character 3 (see chart). **Note** FREQUENCY KHZ switches apply logic 1 inputs in the positions indicated in the chart. In the 0 position, these switches apply logic 0 inputs.	Verify that associated outputs are at logic 1.	
(Cont)	c. Apply logic 0 inputs at inputs associated with word 1, character 3 (see chart).	Verify that associated outputs are at logic 0.	

Table 3. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL

3. (Cont)

EXCITER FRONT-PANEL CONTROL (SIGNAL)	RECEIVER FRONT-PANEL CONTROL (SIGNAL)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
10 kHz 1	10 kHz 1	1	58	26	U25, U18
10 kHz 2	10 kHz 2	2	123	28	U15, U19
10 kHz 4	10 kHz 4	3	59	29	U23, U20
10 kHz 8	10 kHz 8	4	124	94	U21, U17
100 kHz 1	100 kHz 1	5	60	30	U24, U11
100 kHz 2	100 kHz 2	6	125	31	U16, U13
100 kHz 4	100 kHz 4	7	61	96	U22, U12
100 kHz 8	100 kHz 8	8	126	104	U14, U9

4. Word 1, character 4 outputs

a. Strap mux control lines for word 1, character 4.

b. Apply logic 1 inputs at inputs associated with word 1, character 4 (see chart). — Verify that associated outputs are at logic 1.

Note

FREQUENCY KHZ switches apply logic 1 inputs in the positions indicated in the chart. In the 0 position, these switches apply logic 0 inputs.

c. Apply logic 0 inputs at inputs associated with word 1, character 4 (see chart). — Verify that associated outputs are at logic 0.

EXCITER FRONT-PANEL CONTROL (SIGNAL)	RECEIVER FRONT-PANEL CONTROL (SIGNAL)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
100 Hz 1	100 Hz 1	1	54	26	U25, U18
100 Hz 2	100 Hz 2	2	119	28	U15, U19
100 Hz 4	100 Hz 4	3	55	29	U23, U20
100 Hz 8	100 Hz 8	4	120	94	U21, U17
1 kHz 1	1 kHz 1	5	56	30	U24, U11
1 kHz 2	1 kHz 2	6	121	31	U16, U13
1 kHz 4	1 kHz 4	7	57	96	U22, U12
1 kHz 8	1 kHz 8	8	122	104	U14, U9

Table 3. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. Word 1, character 5 outputs	a. Strap mux control lines for word 1, character 5.		
	b. Apply logic 1 inputs at inputs associated with word 1, character 5 (see chart). **Note** FREQUENCY KHZ switches apply logic 1 inputs in the positions indicated in the chart. In the 0 position, these switches apply logic 0 inputs.	Verify that associated outputs are at logic 1.	
	c. Apply logic 0 inputs at inputs associated with word 1, character 5 (see chart).	Verify that associated outputs are at logic 0.	

EXCITER FRONT-PANEL CONTROL (SIGNAL)	RECEIVER FRONT-PANEL CONTROL (SIGNAL)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	NA	1	50	26	U25, R68, U18
NA	NA	2	115	28	U15, R64, U19
NA	NA	3	51	29	U23, R60, U20
NA	NA	4	116	94	U21, R56, U17
*10 Hz 1	*10 Hz 1	5	52	30	U24, R52, U11
*10 Hz 2	*10 Hz 2	6	117	31	U16, R49, U13
*10 Hz 4	*10 Hz 4	7	53	96	U22, R46, U12
*10 Hz 8	*10 Hz 8	8	118	104	U14, R43, U9

*Applicable only with 10-Hz front-panel tuning.

6. Word 2, character 2 outputs (Cont)	a. Strap mux control lines for word 2, character 2.	**Note** Grounded input as noted in chart will always be logic 0 output.	
	b. Apply logic 1 inputs at inputs associated with word 2, character 2 (see chart).	Verify that associated outputs are at logic 1.	

Table 3. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
6. (Cont)	**Note** RF GAIN switch applies logic 1 input in the position indicated in the chart (positions read as MAX minus X number of positions). In the MAX position, this switch applies logic 0 inputs. c. Apply logic 0 inputs at inputs associated with word 2, character 2 (see chart).	Verify that associated outputs are at logic 0.	

EXCITER FRONT-PANEL CONTROL (SIGNAL)	RECEIVER FRONT-PANEL CONTROL (SIGNAL)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	RF GAIN (1)	1	87	26	U25, R69, U18
NA	RF GAIN (2)	2	10	28	U15, R65, U19
NA	RF GAIN (4)	3	75	29	U23, R61, U20
NA	RF GAIN (8)	4	11	94	U21, R57, U17
NA	RF GAIN (16)	5	76	30	U24, R53, U11
NA	NA	6	*	31	U16, U13
NA	NA	7	38	96	U22, U12
NA	NA	8	103	104	U14, R42, U9

*Grounded input.

7. Word 2, character 3 outputs	a. Strap mux control lines for word 2, character 3.	**Note** Grounded input as noted in chart will always be logic 0 output.	
	b. Apply logic 1 inputs at inputs associated with word 2, character 3 (see chart).	Verify that associated ouputs are at logic 1.	
(Cont)	c. Apply logic 0 inputs at inputs associated with word 2, character 3 (see chart).	Verify that associated outputs are at logic 0.	

Table 3. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
7. (Cont)			

EXCITER FRONT-PANEL CONTROL (SIGNAL)	RECEIVER FRONT-PANEL CONTROL (SIGNAL)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	AGC-A2 (1)	1	20	26	U25, U18
NA	AGC-A2 (2)	2	19	28	U15, U19
NA	AGC-B2 (1)	3	85	29	U23, U20
NA	AGC-B2 (2)	4	84	94	U21, U17
NA	FL4 (B) ENBL	5	37	30	U24, U11
NA	FL5 (C) ENBL	6	106	31	U16, U13
NA	FL6 (D) ENBL	7	41	96	U22, U12
NA	FL7 (E) ENBL	8	12	104	U14, U9

8. Word 2, character 4 outputs	a. Strap mux control lines for word 2, character 4.		
	b. Apply logic 1 inputs at inputs associated with word 2, character 4 (see chart).	Verify that associated outputs are at logic 1.	
	c. Apply logic 0 inputs at inputs associated with word 2, character 4 (see chart).	Verify that associated outputs are at logic 0.	

EXCITER FRONT-PANEL CONTROL (SIGNAL)	RECEIVER FRONT-PANEL CONTROL (SIGNAL)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
PEAK CLIP ENABLE	AGC-A1 (1)	1	32	26	U25, R70, U18
NA	AGC-A1 (2)	2	97	28	U15, R66, U19
NA	AGC-B1 (1)	3	33	29	U23, R62, U20
NA	AGC-B1 (2)	4	98	94	U21, R58, U17
NA	AFC ENBL	5	34	30	U24, R54, U11
NA	VBFO ENBL	6	35	31	U16, R50, U13
NA	FL1 ENBL	7	99	96	U22, R47, U12
NA	FL3 (A) ENBL	8	100	104	U14, R44, U9

Table 3. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
9. Word 2, character 5 outputs	a. Strap mux control lines for word 2, character 5.		
	b. Apply logic 1 inputs at inputs associated with word 2, character 5 (see chart).	Verify that associated outputs are at logic 1.	
	c. Apply logic 0 inputs at inputs associated with word 2, character 5 (see chart).	Verify that associated outputs are at logic 0.	

EXCITER FRONT-PANEL CONTROL (MODE) (SIGNAL)	RECEIVER FRONT-PANEL CONTROL (MODE) (SIGNAL)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
12 ENBL	A2 ENBL	1	21	26	U25, R71, U18
A1 ENBL	A1 ENBL	2	91	28	U15, R67, U19
B1 ENBL	B1 ENBL	3	92	29	U23, R63, U20
B2 ENBL	B2 ENBL	4	74	94	U21, R59, U17
ISB ENBL	ISB ENBL	5	9	30	U24, R55, U11
CW ENBL	CW ENBL	6	72	31	U16, R51, U13
AM ENBL	AM ENBL	7	8	96	U22, R48, U12
NA	DATA NET ENBL	8	73	104	U14, R45, U9

10. Word 3, character 2 outputs	a. Strap mux control lines for word 3, character 2.	***Note*** Grounded input as noted in chart will always be logic 0 output.	
	b. Apply logic 1 inputs at inputs associated with word 3, character 2 (see chart).	Verify that associated outputs are at logic 1.	
(Cont)	c. Apply logic 0 inputs at inputs associated with word 3, character 2 (see chart).	Verify that associated outputs are at logic 0.	

Table 3. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
10. (Cont)			

EXCITER FRONT-PANEL CONTROL (SIGNAL)	RECEIVER FRONT-PANEL CONTROL (SIGNAL)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	VBFO 1 kHz 1	1	112	26	U18, U103, U25
NA	VBFO 1 kHz 2	2	47	28	U19, R97, R15
NA	VBFO 1 kHz 4	3	113	29	U20, R91, U23
NA	VBFO 1 kHz 8	4	48	94	U17, R86, U21
NA	(VBFO SIGN)	5	107	30	U11, R81, U24
NA	NA	6	*	31	U13, U16
NA	NA	7	38	96	U12, U22
NA	NA	8	103	104	U9, R42, U14

*Grounded input.

11. Word 3, character 3 outputs	a. Strap mux control lines for word 3, character 3.		
	b. Apply logic 1 inputs at inputs associated with word 3, character 3 (see chart).	Verify that associated outputs are at logic 1.	
	c. Apply logic 0 inputs at inputs associated with word 3, character 3 (see chart).	Verify that associated outputs are at logic 0.	

EXCITER FRONT-PANEL CONTROL (SIGNAL)	RECEIVER FRONT-PANEL CONTROL (SIGNAL)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	VBFO 10 Hz 1	1	42	26	U18, R104, U25
NA	VBFO 10 Hz 2	2	108	28	U19, R98, U15
NA	VBFO 10 Hz 4	3	43	29	U20, R92, U23
NA	VBFO 10 Hz 8	4	109	94	U17, R87, U21
NA	VBFO 100 Hz 1	5	44	30	U11, R82, U24
NA	VBFO 100 Hz 2	6	110	31	U13, R78, U16
NA	VBFO 100 Hz 4	7	111	96	U12, R75, U22
NA	VBFO 100 Hz 8	8	46	104	U9, R72, U14

Table 3. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
12. Word 3, character 4 outputs	a. Strap mux control lines for word 3, character 4.	***Note*** Grounded input as noted in chart will always be logic 0 output. Verify that all associated outputs are at logic 0.	

EXCITER FRONT-PANEL CONTROL (SIGNAL)	RECEIVER FRONT-PANEL CONTROL (SIGNAL)	BIT NO	INPUTS P2-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	NA	1	4	26	U18, U25
NA	NA	2	6	28	U19, U15
NA	NA	3	5	29	U20, U23
NA	NA	4	3	94	U17, U21
NA	NA	5	9	30	U11, U24
NA	NA	6	10	31	U13, U16
NA	NA	7	8	96	U12, U22
NA	NA	8	7	104	U9, U14

13. Word 3, character 5 outputs (Cont)	a. Strap mux control lines for word 3, character 5.	***Note*** Grounded input as noted in chart will always be logic 0 output.	
	b. Apply logic 1 inputs at inputs associated with word 3, character 5 (see chart). ***Note*** PA PWR and PILOT CARR switches apply logic 1 inputs in the positions indicated in the chart. In the OFF positions these switches apply logic 0 inputs.	Verify that associated outputs are at logic 1.	
	c. Apply logic 0 inputs at inputs associated with word 3, character 5 (see chart).	Verify that associated outputs are at logic 0.	

Table 3. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
13. (Cont)			

EXCITER FRONT-PANEL CONTROL (SIGNAL)	RECEIVER FRONT-PANEL CONTROL (SIGNAL)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
PA PWR-STBY	A2 AGC BUS	1	79	26	U18, R105, U25
PA PWR-HIGH PWR	A1 AGC BUS	2	14	28	U19, R99, U15
PA PWR-LOW PWR	B1 AGC BUS	3	78	29	U20, R93, U23
PILOT CARR-ON	B2 AGC BUS	4	82	94	U17, R8, U21
NA	NA	5	81	30	U11, R83, U24
NA	NA	6	*	31	U13, U16
NA	NA	7	*	96	U12, U22
NA	NA	8	*	104	U9, U14

*Grounded input.

14. Word 4, character 2 outputs	a. Strap mux control lines for word 4, character 2.	***Note*** Grounded input as noted in chart will always be logic 0 output.	
	b. Apply logic 1 inputs at inputs associated with word 4, character 2 (see chart).	Verify that associated outputs are at logic 1.	
(Cont)	c. Apply logic 0 inputs at inputs associated with word 4, character 2 (see chart).	Verify that associated outputs are at logic 0.	

Table 3. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL

14. (Cont)

EXCITER FRONT-PANEL CONTROL (SIGNAL)	RECEIVER FRONT-PANEL CONTROL (SIGNAL)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
(A2 AF MON)	(A2 AF MON)	1	24	26	U18, U25
(A1 AF MON)	(A1 AF MON)	2	22	28	U19, U15
(B1 AF MON)	(B1 AF MON)	3	23	29	U20, U23
(B2 AF MON)	(B2 AF MON)	4	88	94	U17, U21
(REMOTE KEY (MON))	(RF OVLD MON)	5	68	30	U11, R12, U24
(EXCITER FLT)	(RECEIVER FLT)	6	13	31	U13, U16
NA	NA	7	38	96	U12, U22
NA	NA	8	103	104	U9, R42, U14

*Grounded input.

15. Word 4, character 3 outputs	a. Strap mux control lines for word 4, character 3.		
	b. Apply logic 1 inputs at inputs associated with word 4, character 3 (see chart).	Verify that associated outputs are at logic 1.	
	c. Apply logic 0 inputs at inputs associated with word 4, character 3 (see chart).	Verify that associated outputs are at logic 0.	

EXCITER FRONT-PANEL CONTROL (SIGNAL)	RECEIVER FRONT-PANEL CONTROL (SIGNAL)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
(FREQ REF FLT)	(FREQ REF FLT)	1	18	26	U18, R106, U25
(SYNTH OUT LOCK FLT)	(SYNTH OUT LOCK FLT)	2	101	28	U19, R100, U15
(100 kHz LOCK FLT)	(100 kHz LOCK FLT)	3	39	29	U20, R94, U23
(10 kHz LOCK FLT)	(10 kHz LOCK FLT)	4	83	94	U17, R88, U21
(1 kHz LOCK FLT)	(1 kHz LOCK FLT)	5	36	30	U11, R85, U24
(100 Hz LOCK FLT)	(100 Hz LOCK FLT)	6	105	31	U13, R79, U16
(10 Hz LOCK FLT)	(10 Hz LOCK FLT)	7	40	96	U12, R76, U22
NA	NA	8	2	104	U9, R73, U14

Table 3. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
16. Word 4, character 4 outputs	a. Strap mux control lines for word 4, character 4.		
	b. Apply logic 1 inputs at inputs associated with word 4, character 4 (see chart).	Verify that associated outputs are at logic 1.	
	c. Apply logic 0 inputs at inputs associated with word 4, character 4 (see chart).	Verify that associated outputs are at logic 0.	

EXCITER FRONT-PANEL CONTROL (SIGNAL)	RECEIVER FRONT-PANEL CONTROL (SIGNAL)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	(A2 AGC MON)	1	3	26	U18, R107, U25
(A1 IF MON)	(A1 AGC MON)	2	86	28	U19, R101, U15
(EXT STANDARD)	(B1 AGC MON)	3	49	29	U20, R95, U23
NA	(B2 AGC MON)	4	67	94	U17, R89, U21
(EXCTR PS FLT)	(RCVR PS FLT)	5	70	30	U11, R85, U24
(EXCTR RF MON)	(VBFO SYNTH FLT)	6	5	31	U13, R80, U16
(SUBCARR LOCK FLT)	(SUBCARR LOCK FLT)	7	4	96	U12, R77, U22
NA	NA	8	69	104	U9, R74, U14

17. Word 4, character 5 outputs (Cont)	a. Strap mux control lines for word 4, character 5.	*Note* Grounded input as noted in chart will always be logic 0 output.	
	b. Apply logic 1 inputs at inputs associated with word 4, character 5 (see chart).	Verify that associated outputs are at logic 1.	
	c. Apply logic 0 inputs at inputs associated with word 4, character 5 (see chart).	Verify that associated outputs are at logic 0.	

Table 3. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE		NORMAL INDICATION		IF INDICATION IS ABNORMAL
17. (Cont)					
EXCITER FRONT-PANEL CONTROL (SIGNAL)	RECEIVER FRONT-PANEL CONTROL (SIGNAL)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
(MONITOR)	(MONITOR)	1	80	26	U18, R108, U25
(LCL CONT)	(LCL CONT)	2	16	28	U19, R102, CR24, C28, U15
(DATA ERROR)	(DATA ERROR)	3	95	29	U20, R96, U23
(PRESEL FLT)	(PRESEL FLT)	4	71	94	U17, R90, U21
(CPLR FLT)	(RF XLATOR MON)	5	*	30	U11, U24
(PA RF MON)	(AFC LOCK MON)	6	*	31	U13, U16
(PA FLT)	(EXT STANDARD)	7	*	96	U12, U22
(PA READY)	NA	8	*	104	U9, U14
*Grounded input.					

4. REPAIR

Repair of the parallel input card is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

5. PARTS LIST/DIAGRAMS

5.1 Introduction

Caution

This equipment contains electrostatic discharge sensitive (ESDS) devices. Special handling methods and materials must be used to prevent equipment damage. Refer to the maintenance section for the equipment before assembly/disassembly or repair is performed. ESDS items are identified in the description column of the parts list by (ESDS).

All supporting parts list illustrations that contain ESDS items are shown with the following symbol.

This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figure 3). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on the schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator. In addition, the manufacturer's code and part number are listed when applicable.

5.2 Parts List

REF DES Column — Reference designators of each part/subassembly are listed in alphanumeric sequence. These are the reference designators shown on the parts location drawing and schematic diagram.

DESCRIPTION Column — Lists the noun name, modifier, descriptive information, and modifications.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points to the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

COLLINS PART NUMBER Column — Lists the Collins part number for each item in the parts list.

USABLE ON CODE Column — Part variations within a group of equipment are indicated by a letter code (A, B, C, etc). Absence of a code indicates part applies to all models.

MFR CODE Column — Lists the manufacturer's code from which selected parts can be procured.

MFR PART NUMBER Column — Lists the manufacturer's part number for the selected parts.

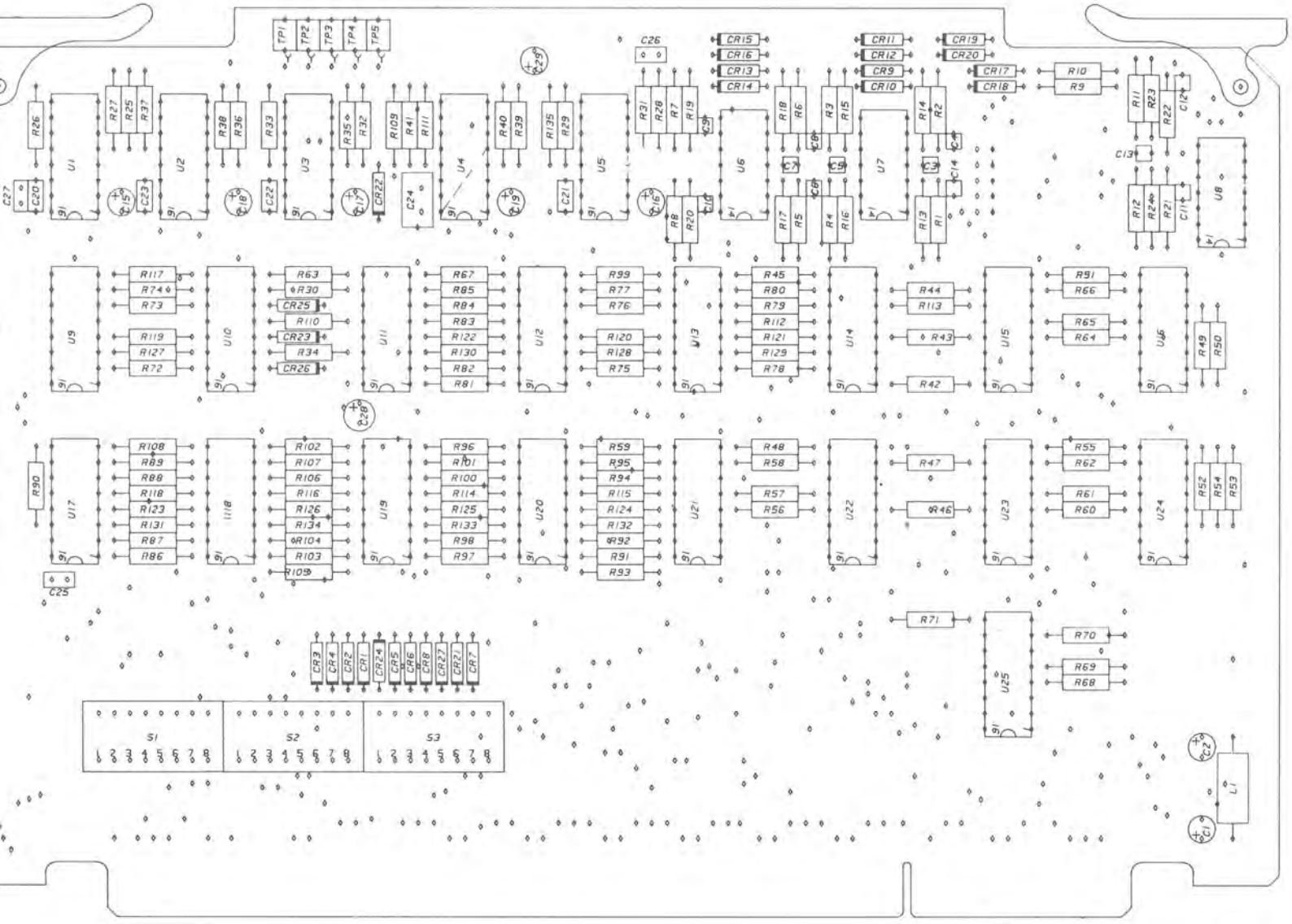
Listed below are the manufacturer's names and addresses for the manufacturer's codes used in this parts list.

MFR CODE	MANUFACTURER'S NAME AND ADDRESS
03508	GENERAL ELECTRIC CO SEMI-CONDUCTOR PRODUCTS DEPT W GENESEE ST AUBURN NY 13021
04713	MOTOROLA INC SEMICONDUCTOR PRODUCTS GROUP 5005 E MCDOWELL RD PHOENIX AZ 85008
07263	FAIRCHILD CAMERA AND INSTRUMENT CORP SEMICONDUCTOR DIV 464 ELLIS ST MOUNTAIN VIEW CA 94042
16546	GLOBE-UNION INC USCC/CENTRALAB ELECTRICS DIV 4561 COLORADO LOS ANGELES CA 90039
27264	MOLEX INC CORPORATE HQ 2222 WELLINGTON COURT LISLE IL 60532
56289	SPRAGUE ELECTRIC CO NORTH ADAMS MA 01247
74970	JOHNSON E F CO 299 10TH AVE S W WASECA MN 56093
81349	MILITARY SPECIFICATION
96906	MILITARY STANDARD

5.3 Equipment Covered

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

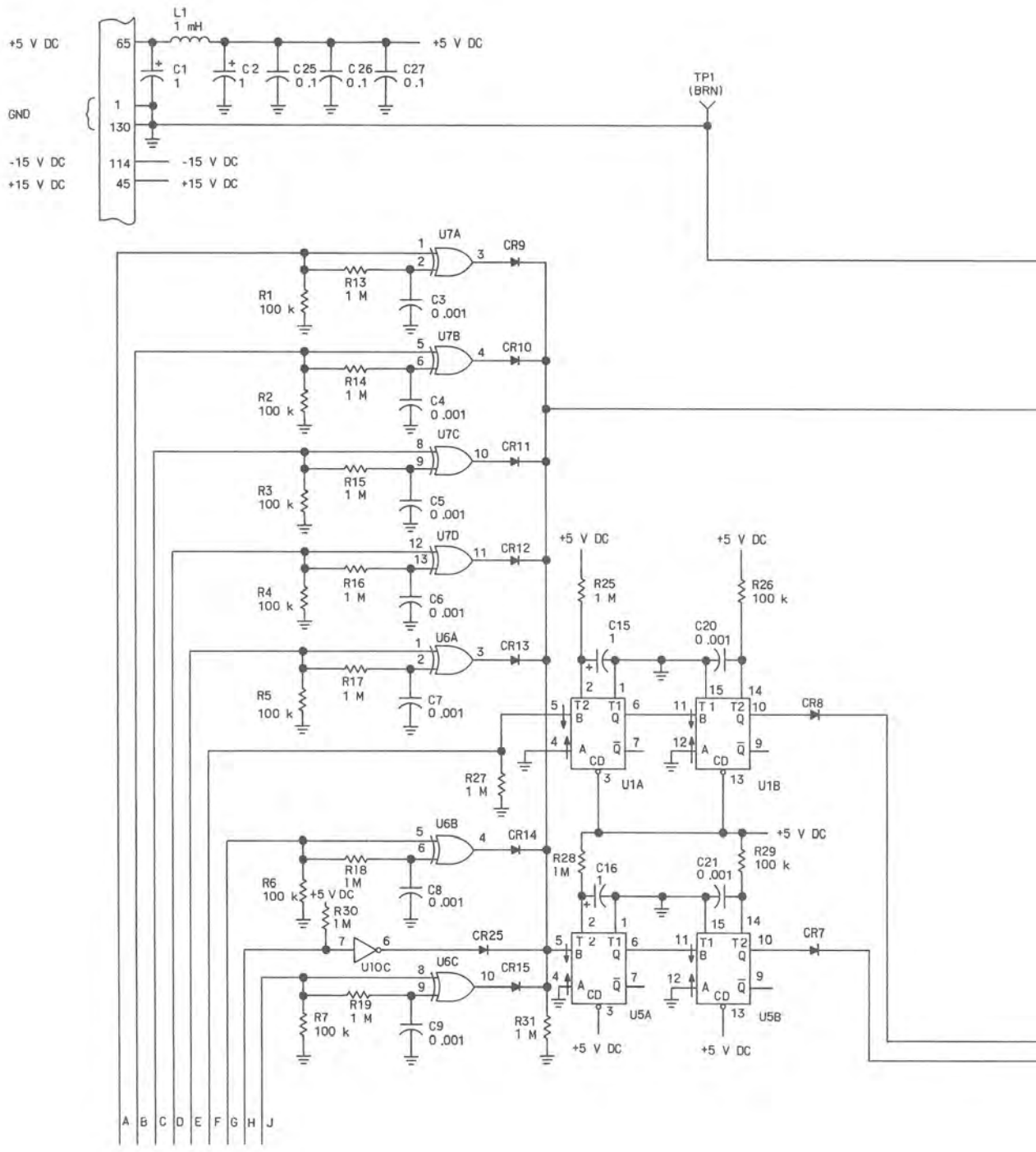
CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Parallel Input	642-3135-001	REV D

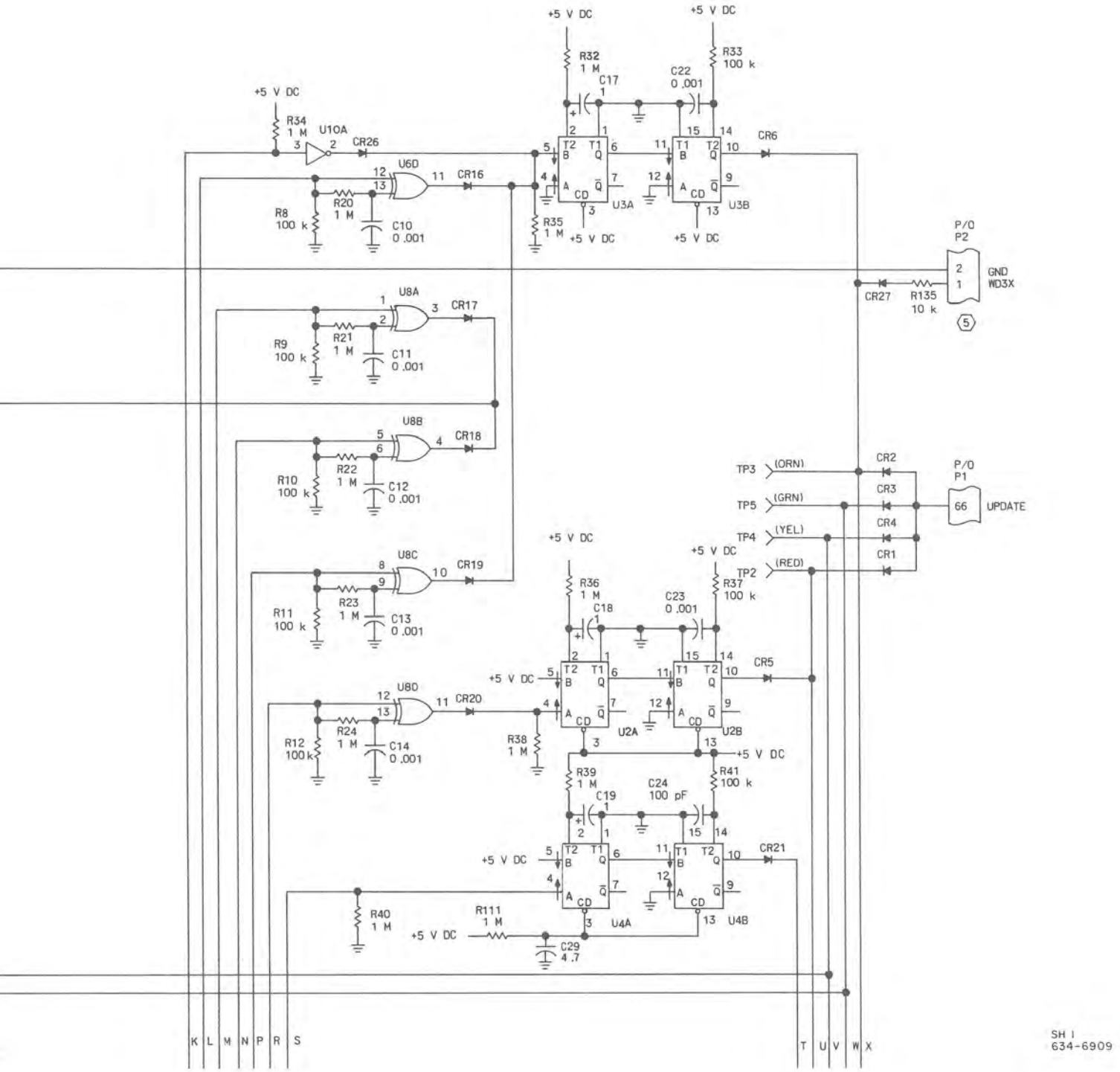


Parallel Input, Schematic Diagram
Figure 3 (Sheet 1 of 6)

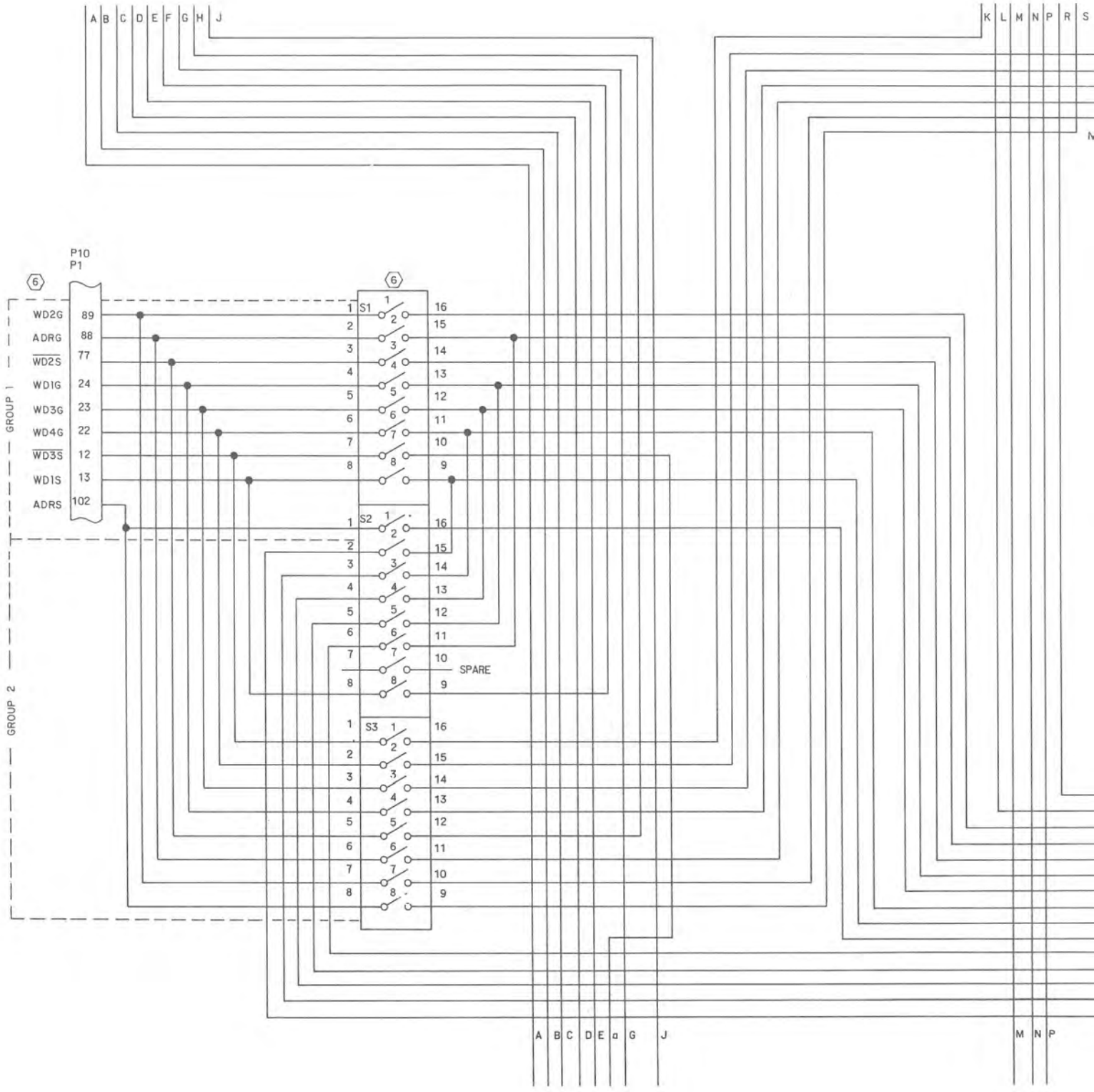
PARTS LIST

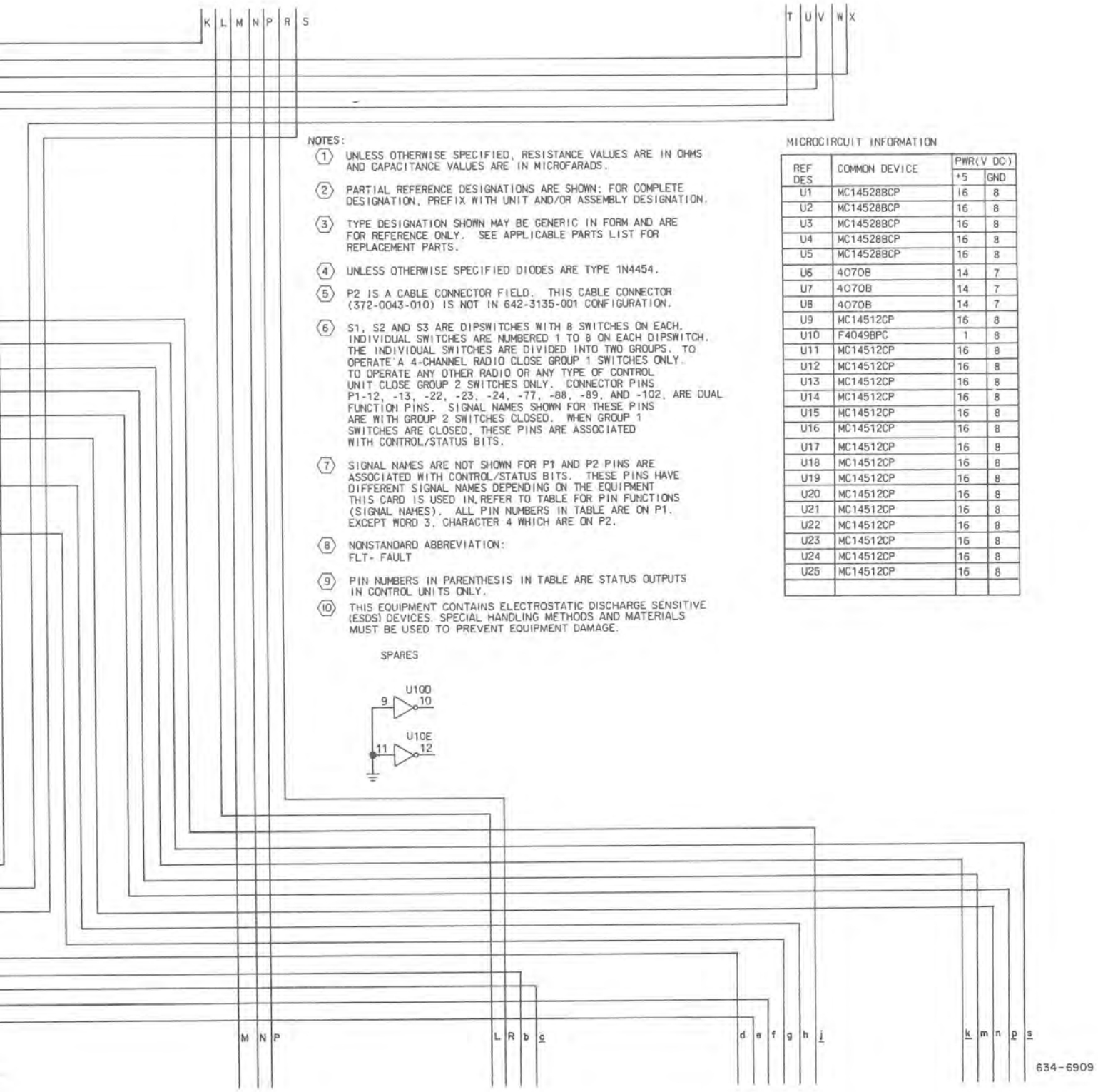
REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE	MFR CODE	MFR PART NUMBER
	PARALLEL INPUT (ESDS)	642-3135-001			
CR1-CR27	SEMICOND DEVICE	353-3644-010		03508	1N4454GE
C1,C2	CAPACITOR,FXD TNTLM ELCTLT, 1UF, 20%, 35V	184-9102-350		56289	199D105X0035BB1
C3-C14	CAPACITOR,FXD CER DIEL, 1000PF, 20%, 50V	913-3279-030		16546	CY10C102M
C15-C19	CAPACITOR,FXD TNTLM ELCTLT, 1UF, 20%, 35V	184-9102-350		56289	199D105X0035BB1
C20-C23	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000		81349	CK05BX102K
C24	CAPACITOR,FXD MICA DIEL, 100PF, 5%, 500V	912-3879-000		81349	CM04FD101J03
C25-C27	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-680		16546	CY20C104M
C28,C29	CAPACITOR,FXD TNTLM ELCTLT, 4.7UF, 20%, 35V	184-9102-390		56289	199D475X0035DB1
L1	COIL,RF 1000UH	240-2540-000		96906	MS90539-15
R1-R12	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000		81349	RCR07G104KS
R13-R25	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000		81349	RCR07G105KS
R26	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000		81349	RCR07G104KS
R27,R28	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000		81349	RCR07G105KS
R29	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000		81349	RCR07G104KS
R30-R32	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000		81349	RCR07G105KS
R33	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000		81349	RCR07G104KS
R34-R36	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000		81349	RCR07G105KS
R37	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000		81349	RCR07G104KS
R38-R40	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000		81349	RCR07G105KS
R41	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000		81349	RCR07G104KS
R42-R108	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000		81349	RCR07G105KS
R109	RESISTOR,FXD CMPSN, 4.7K, 10%, 1/4W	745-0773-000		81349	RCR07G472KS
R110	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000		81349	RCR07G104KS
R111-R118	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000		81349	RCR07G105KS
R119-R126	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000		81349	RCR07G103KS
R127-R134	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000		81349	RCR07G105KS
R135	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000		81349	RCR07G103KS
S1-S3	SWITCH,DUAL PKG	266-0243-050		27264	A10040-108
TP1	JACK,TIP BRN	360-0484-070		74970	105-1108-011
TP2	JACK,TIP RED	360-0484-020		74970	105-1102-011
TP3	JACK,TIP ORN	360-0484-050		74970	105-1106-011
TP4	JACK,TIP YEL	360-0484-060		74970	105-1107-011
TP5	JACK,TIP GRN	360-0484-040		74970	105-1104-011
U1-U5	INTEGRATED CIRCUIT (ESDS)	351-8421-020		07263	4528BPC
U6-U8	INTEGRATED CIRCUIT (ESDS)	351-8407-010		04713	MC14070BCP
U9	INTEGRATED CIRCUIT DATA SELECTOR	351-8420-020		04713	MC14512BCP
U10	INTEGRATED CIRCUIT (ESDS)	351-8159-210		07263	F4049BPC
U11-U25	INTEGRATED CIRCUIT DATA SELECTOR	351-8420-020		04713	MC14512BCP


L1
1 mH
+5 V DC
65
+5 V DC
C1
1
C2
1
C25
0.1
C26
0.1
C27
0.1
GND
1
130
TP1
(BRN)
-15 V DC
114
-15 V DC
+15 V DC
45
+15 V DC
U7A
CR9
R13
1 M
R1
100 k
C3
0.001
U7B
CR10
R14
1 M
R2
100 k
C4
0.001
U7C
CR11
R15
1 M
R3
100 k
C5
0.001
U7D
CR12
R16
1 M
R4
100 k
C6
0.001
U6A
CR13
R17
1 M
R5
100 k
C7
0.001
+5 V DC
R25
1 M
C15
1
C20
0.001
+5 V DC
R26
100 k
CR8
R27
1 M
U1A
U1B
U6B
CR14
R18
1M
R6
100 k
+5 V DC
C8
0.001
R30
1 M
U10C
CR25
U6C
CR15
R19
1 M
R7
100 k
C9
0.001
R31
1 M
+5 V DC
R28
1M
C16
1
C21
0.001
+5 V DC
R29
100 k
CR7
U5A
U5B
+5 V DC
+5 V DC
A
B
C
D
E
F
G
H
J



Parallel Input, Schematic Diagram
Figure 3 (Sheet 3)


A B C D E F G H J
K L M N P R S
P10
P1
6
WD2G 89
ADRG 88
WD2S 77
WD1G 24
WD3G 23
WD4G 22
WD3S 12
WD1S 13
ADRS 102
GROUP 1
GROUP 2
S1
S2
S3
SPARE
A B C D E a G J
M N P



NOTES:

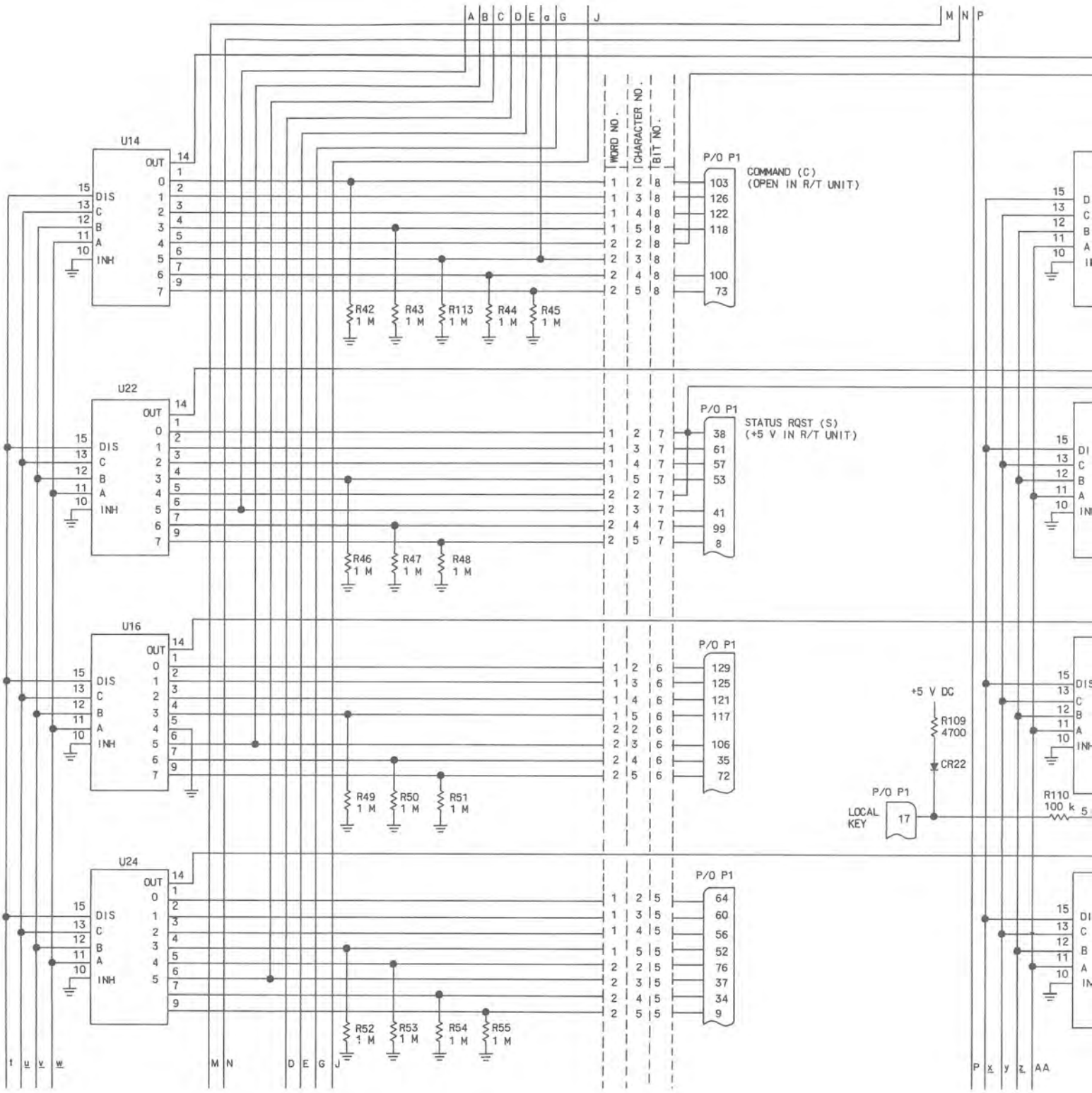
1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. TYPE DESIGNATION SHOWN MAY BE GENERIC IN FORM AND ARE FOR REFERENCE ONLY. SEE APPLICABLE PARTS LIST FOR REPLACEMENT PARTS.
4. UNLESS OTHERWISE SPECIFIED DIODES ARE TYPE 1N4454.
5. P2 IS A CABLE CONNECTOR FIELD. THIS CABLE CONNECTOR (372-0043-010) IS NOT IN 642-3135-001 CONFIGURATION.
6. S1, S2 AND S3 ARE DIPSWITCHES WITH 8 SWITCHES ON EACH. INDIVIDUAL SWITCHES ARE NUMBERED 1 TO 8 ON EACH DIPSWITCH. THE INDIVIDUAL SWITCHES ARE DIVIDED INTO TWO GROUPS. TO OPERATE A 4-CHANNEL RADIO CLOSE GROUP 1 SWITCHES ONLY. TO OPERATE ANY OTHER RADIO OR ANY TYPE OF CONTROL UNIT CLOSE GROUP 2 SWITCHES ONLY. CONNECTOR PINS P1-12, -13, -22, -23, -24, -77, -88, -89, AND -102, ARE DUAL FUNCTION PINS. SIGNAL NAMES SHOWN FOR THESE PINS ARE WITH GROUP 2 SWITCHES CLOSED. WHEN GROUP 1 SWITCHES ARE CLOSED, THESE PINS ARE ASSOCIATED WITH CONTROL/STATUS BITS.
7. SIGNAL NAMES ARE NOT SHOWN FOR P1 AND P2 PINS ARE ASSOCIATED WITH CONTROL/STATUS BITS. THESE PINS HAVE DIFFERENT SIGNAL NAMES DEPENDING ON THE EQUIPMENT THIS CARD IS USED IN. REFER TO TABLE FOR PIN FUNCTIONS (SIGNAL NAMES). ALL PIN NUMBERS IN TABLE ARE ON P1, EXCEPT WORD 3, CHARACTER 4 WHICH ARE ON P2.
8. NONSTANDARD ABBREVIATION:
   FLT- FAULT
9. PIN NUMBERS IN PARENTHESIS IN TABLE ARE STATUS OUTPUTS IN CONTROL UNITS ONLY.
10. THIS EQUIPMENT CONTAINS ELECTROSTATIC DISCHARGE SENSITIVE (ESDS) DEVICES. SPECIAL HANDLING METHODS AND MATERIALS MUST BE USED TO PREVENT EQUIPMENT DAMAGE.

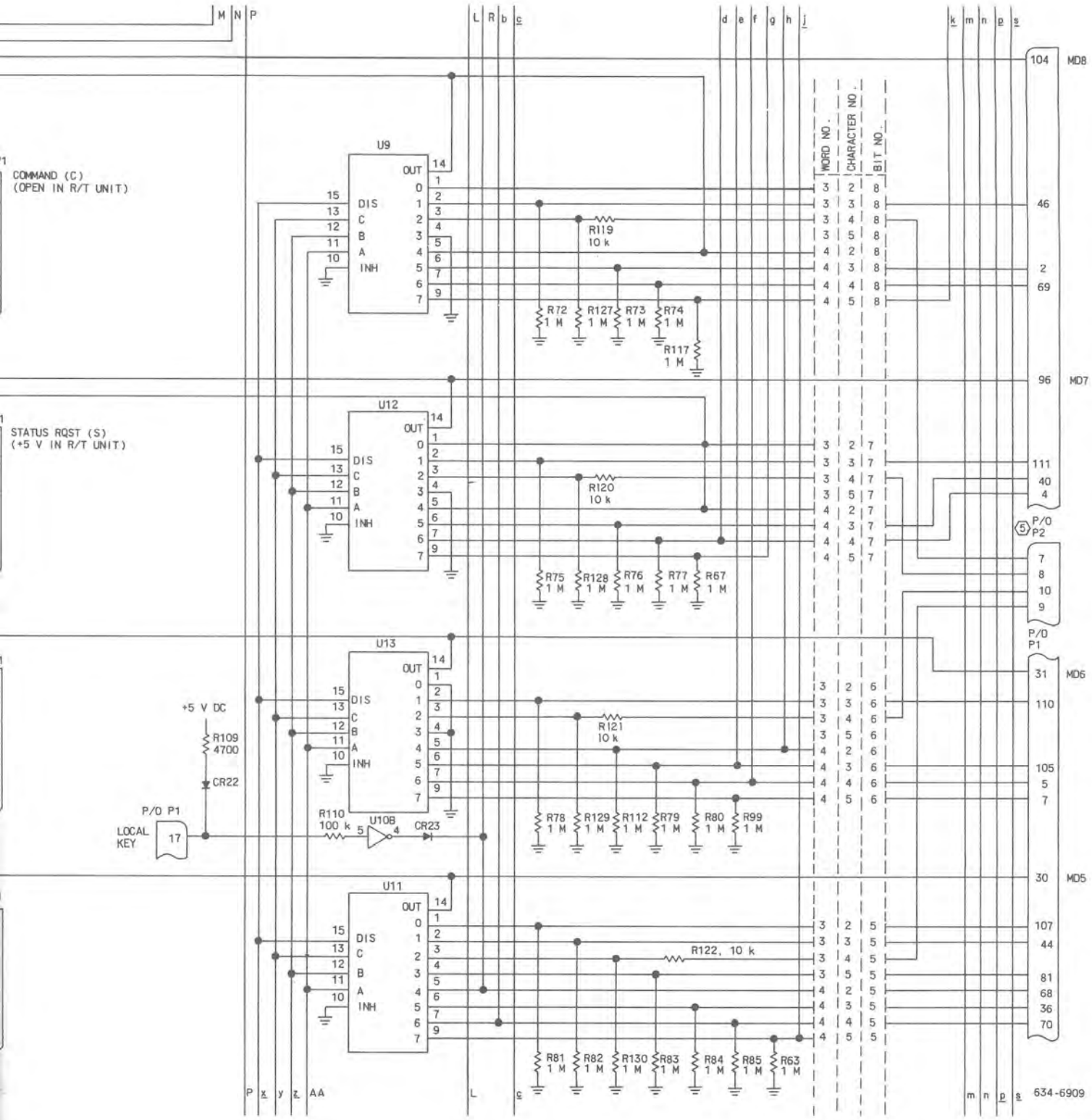
MICROCIRCUIT INFORMATION

REF DES	COMMON DEVICE	PWR(V DC) +5	GND
U1	MC14528BCP	16	8
U2	MC14528BCP	16	8
U3	MC14528BCP	16	8
U4	MC14528BCP	16	8
U5	MC14528BCP	16	8
U6	4070B	14	7
U7	4070B	14	7
U8	4070B	14	7
U9	MC14512CP	16	8
U10	F4049BPC	1	8
U11	MC14512CP	16	8
U12	MC14512CP	16	8
U13	MC14512CP	16	8
U14	MC14512CP	16	8
U15	MC14512CP	16	8
U16	MC14512CP	16	8
U17	MC14512CP	16	8
U18	MC14512CP	16	8
U19	MC14512CP	16	8
U20	MC14512CP	16	8
U21	MC14512CP	16	8
U22	MC14512CP	16	8
U23	MC14512CP	16	8
U24	MC14512CP	16	8
U25	MC14512CP	16	8

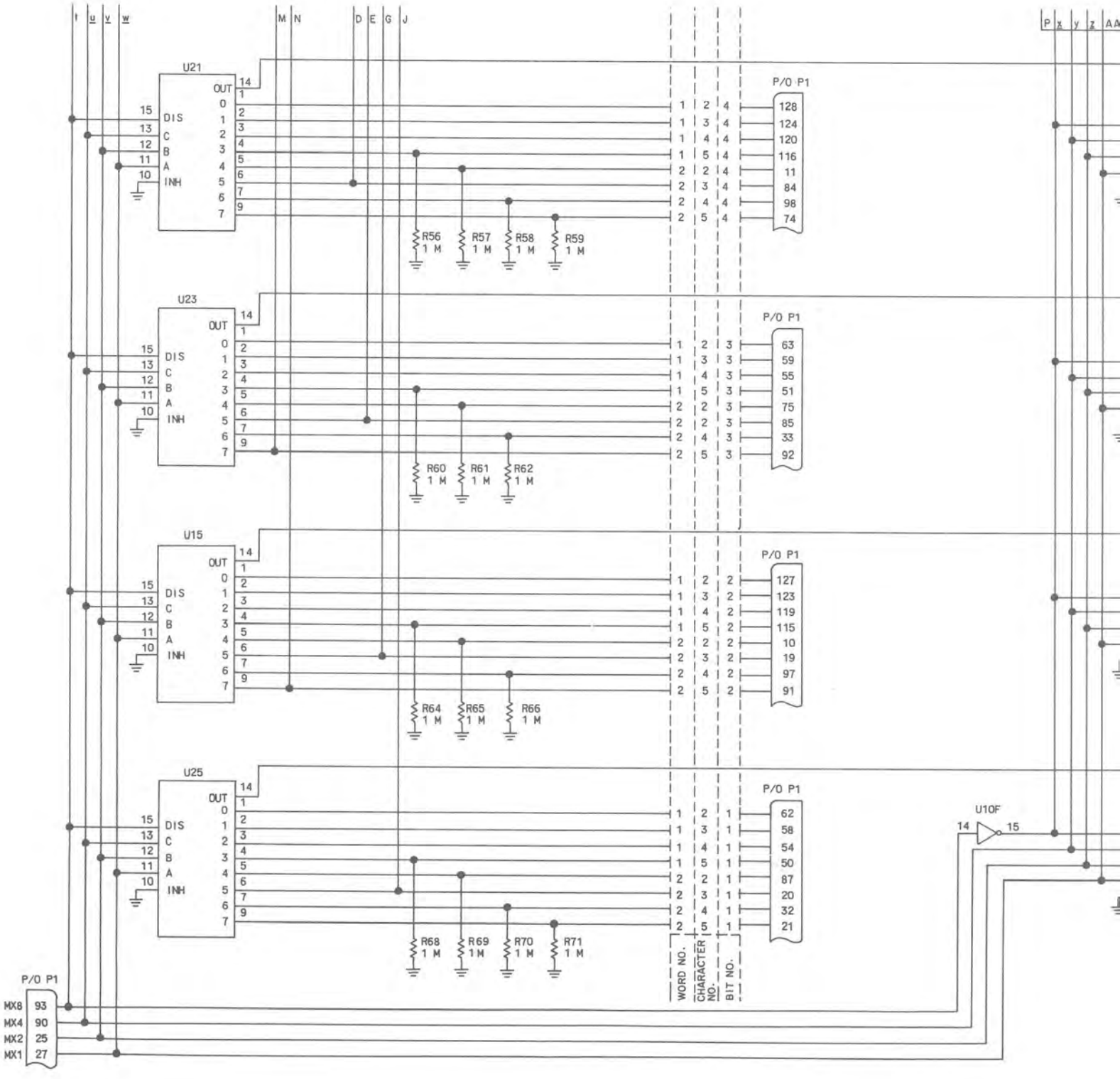
SPARES

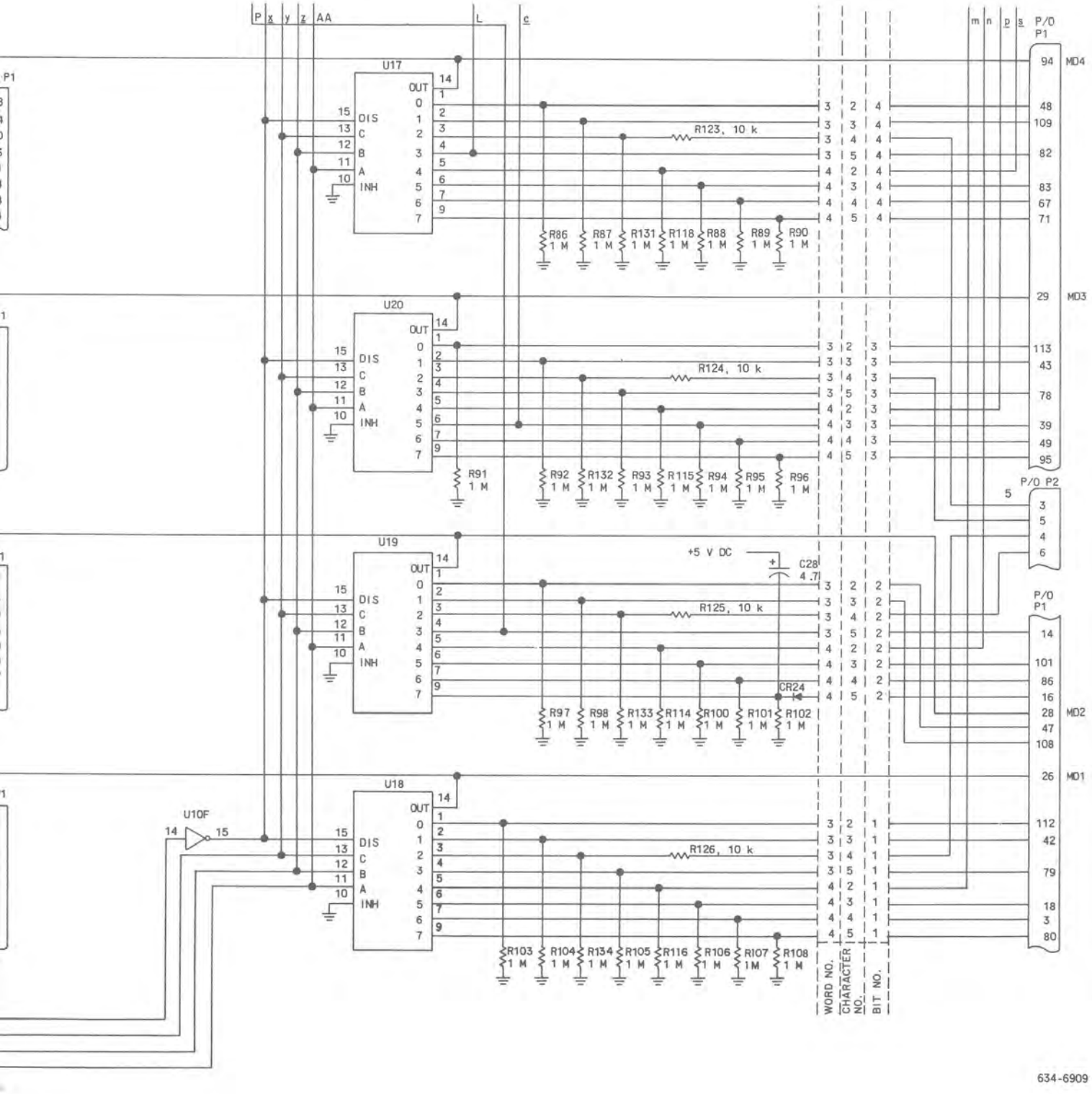
Parallel Input, Schematic Diagram
Figure 3 (Sheet 4)


A B C D E G J
M N P
WORD NO.
CHARACTER NO.
BIT NO.
U14
OUT
DIS
C
B
A
INH
R42 1 M
R43 1 M
R113 1 M
R44 1 M
R45 1 M
P/O P1
COMMAND (C)
(OPEN IN R/T UNIT)
103
126
122
118
100
73
U22
R46 1 M
R47 1 M
R48 1 M
STATUS RQST (S)
(+5 V IN R/T UNIT)
38
61
57
53
41
99
8
U16
R49 1 M
R50 1 M
R51 1 M
129
125
121
117
106
35
72
+5 V DC
R109 4700
CR22
LOCAL KEY
17
R110 100 k
U24
R52 1 M
R53 1 M
R54 1 M
R55 1 M
64
60
56
52
76
37
34
9
t u v w
M N
D E G J
P x y z AA



Parallel Input, Schematic Diagram
Figure 3 (Sheet 5)


t u v w
M N
D E G J
P x y z AA
U21
U23
U15
U25
OUT
DIS
C
B
A
INH
R56 1 M
R57 1 M
R58 1 M
R59 1 M
R60 1 M
R61 1 M
R62 1 M
R64 1 M
R65 1 M
R66 1 M
R68 1 M
R69 1 M
R70 1 M
R71 1 M
P/O P1
128
124
120
116
11
84
98
74
63
59
55
51
75
85
33
92
127
123
119
115
10
19
97
91
62
58
54
50
87
20
32
21
U10F
MX8 93
MX4 90
MX2 25
MX1 27
WORD NO.
CHARACTER NO.
BIT NO.



Parallel Input, Schematic Diagram
Figure 3 (Sheet 6)