523-0769210-00121A

Rockwell International

Collins instruction book

Part 2

851S-1 Receiver

Part 2 of this instruction book includes:

Power Supply	*523-0767948*
LED Status Display	*523-0767946*
Count/Store Assembly	*523-0769218*
Frequency Display	*523-0767975*
VBFO	*523-0769219*
Receive Audio	*523-0767956*
Channel B IF	*523-0767965*
Channel A IF	*523-0767962*
Filter	*523-0767967*
RF Translator	*523-0767959*
RF Translator (1/2-Octave RF Filters)	*523-0769220*
Control	*523-0769221*
Parallel Input	*523-0767949*
Parallel Output	*523-0767950*
Serial Interface	*523-0767951*
Synthesizer Voltage Regulator	*523-0767974*
Synthesizer Reference	*523-0767970*
Synthesizer End Decade	*523-0767973*
Synthesizer Decade	*523-0767972*
Synthesizer Output	*523-0767971*
TS-8010 Card Extender Kit	*523-0767968*
Options	
AC-8012 Oven Standard Kit	*523-0768671*
AC-8013 External Standard Kit	*523-0768672*
AC-8090 Remote Control Kit	*523-0768675*
AC-85100 ISB Kit	*523-0769222*
AC-85101 DVBFO Kit	*523-0769223*
AC-85102 Decade Expansion Kit	*523-0769224*
AC-85105 Optional Filters Kit	*523-0769226*
AC-85106 RF Translator Kit	*523-0769227*
AC-85108 Channel A IF Kit	*523-0769225*

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Power Supply (635-9649-001)

Rockwell International

instructions

Collins Telecommunications Products Division

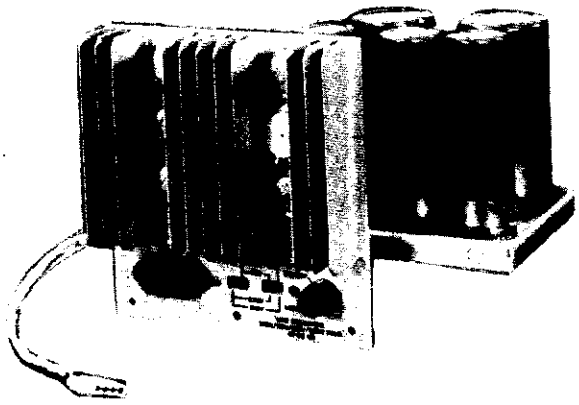
Printed in USA

523-0767948-002211
2nd Edition, 1 June 1978

1. DESCRIPTION

Power Supply 635-9649-001, shown in figure 1, is a module that contains a power transformer, a 2-section input power strapping switch, six power regulators, and a planar circuit card with full-wave rectifiers and an output fault circuit.

The power supply module consists of four primary functional areas: input power switching, power transformer and rectifiers, regulators, and the output fault summary circuit. Refer to figure 2 for a block diagram of the power supply module.



Power Supply
Figure 1

2. PRINCIPLES OF OPERATION

2.1 General

This power supply is fuse protected (2 A for 100/115 V ac; 1 A for 215/230 V ac) and supplies a loss-of-output fault indication. The input power is switchable between 100-, 115-, 215-, and 230-V ac single phase. Output voltages supplied are +24, +18, +15, +8, +5, and -15 V dc.

2.2 Input Power Switching (Refer to figure 3.)

The input power circuit consists of a fuse protector, power on-off switch S2, power control switch S1, and power transformer T1.

Note that power control switch S1 is a dual switch having two 2-position switches. S1A (low pin numbers) selects between series connection (215, 230 V ac) and parallel connection (110, 115 V ac) of transformer T1. S1B (high pin numbers) selects between less-turns ratio (115, 230 V ac) and more-turns ratio (110, 215 V ac) of transformer T1.

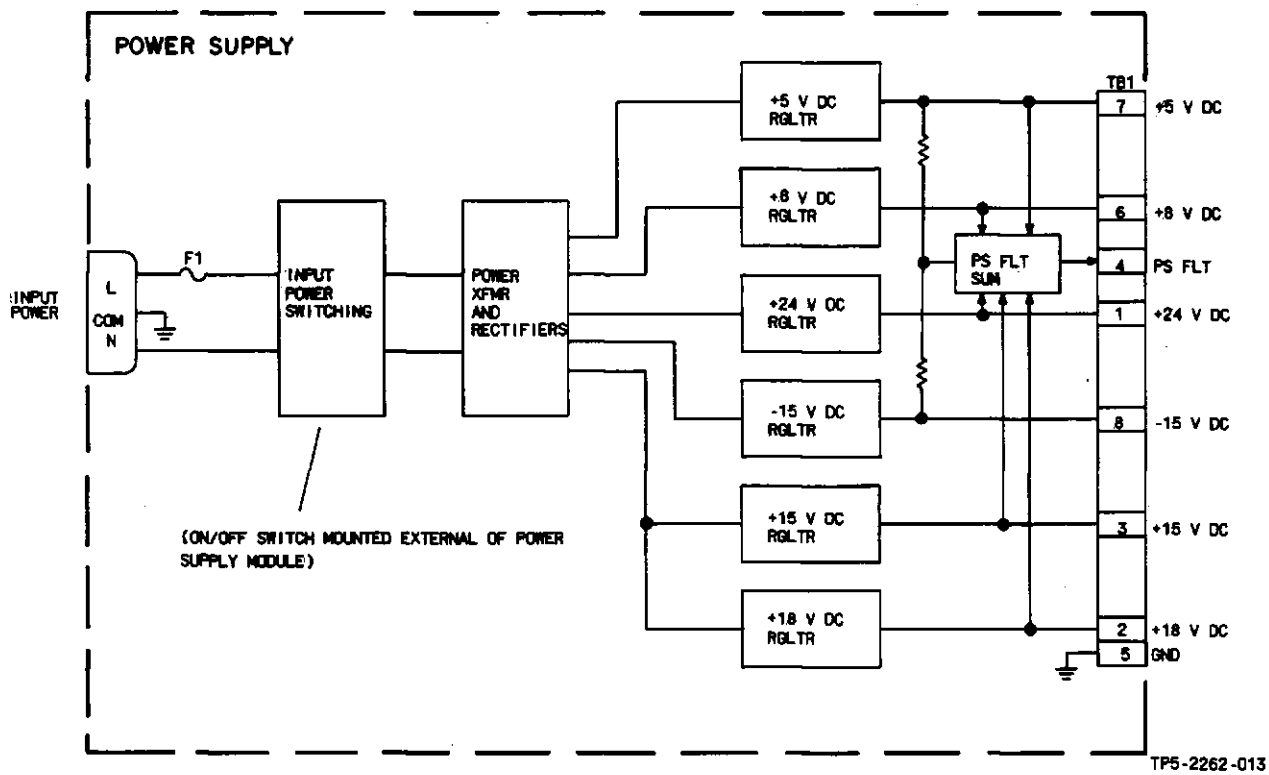
2.3 Power Transformer, Rectifiers, and Regulators (Refer to figure 4.)

Power supply outputs are generated by the dual secondary of T1, full-wave rectified by five rectifier circuits, and regulated by six micromodule regulators. Each regulator has its own input rectifier circuit, except the +18- and +15-V dc regulators share a rectifier.

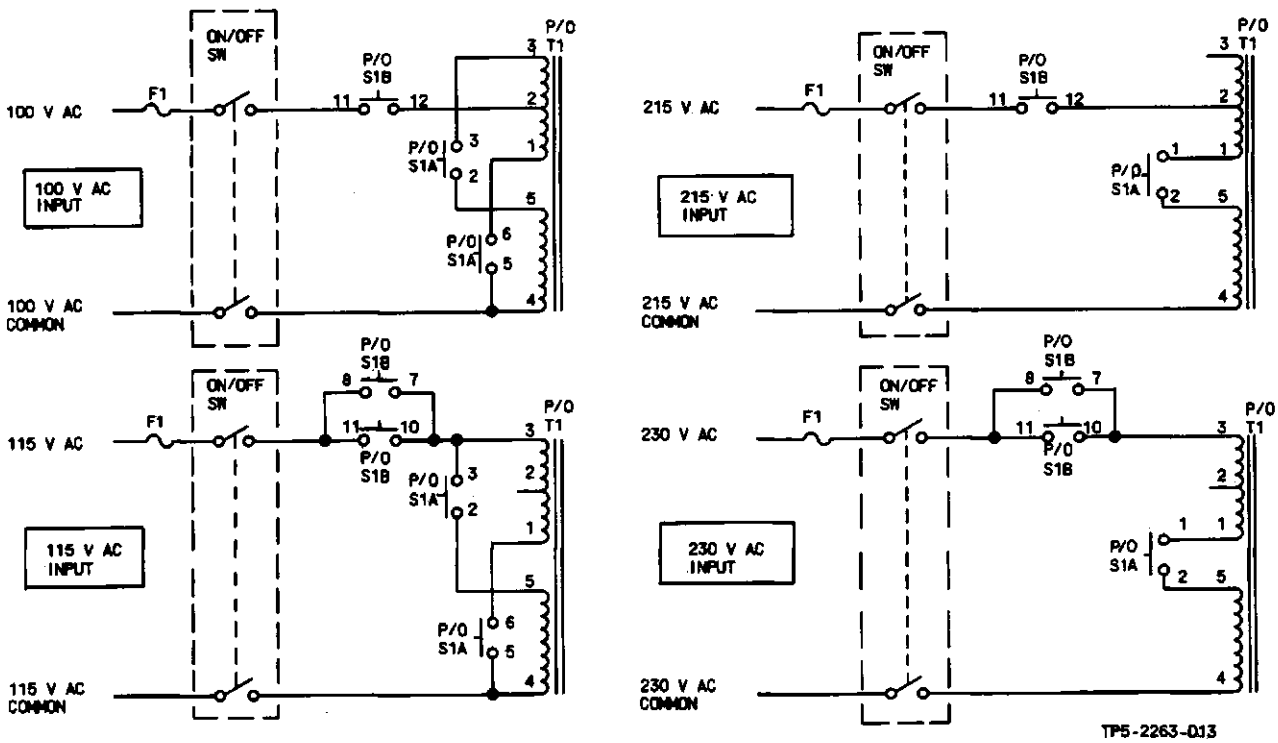
2.4 Fault Summary (Refer to figure 5.)

A fault summary circuit provides constant monitoring of power supply outputs and generates a fault output if any positive output drops below +5 V dc or if the negative output goes any more positive than -5 V dc.

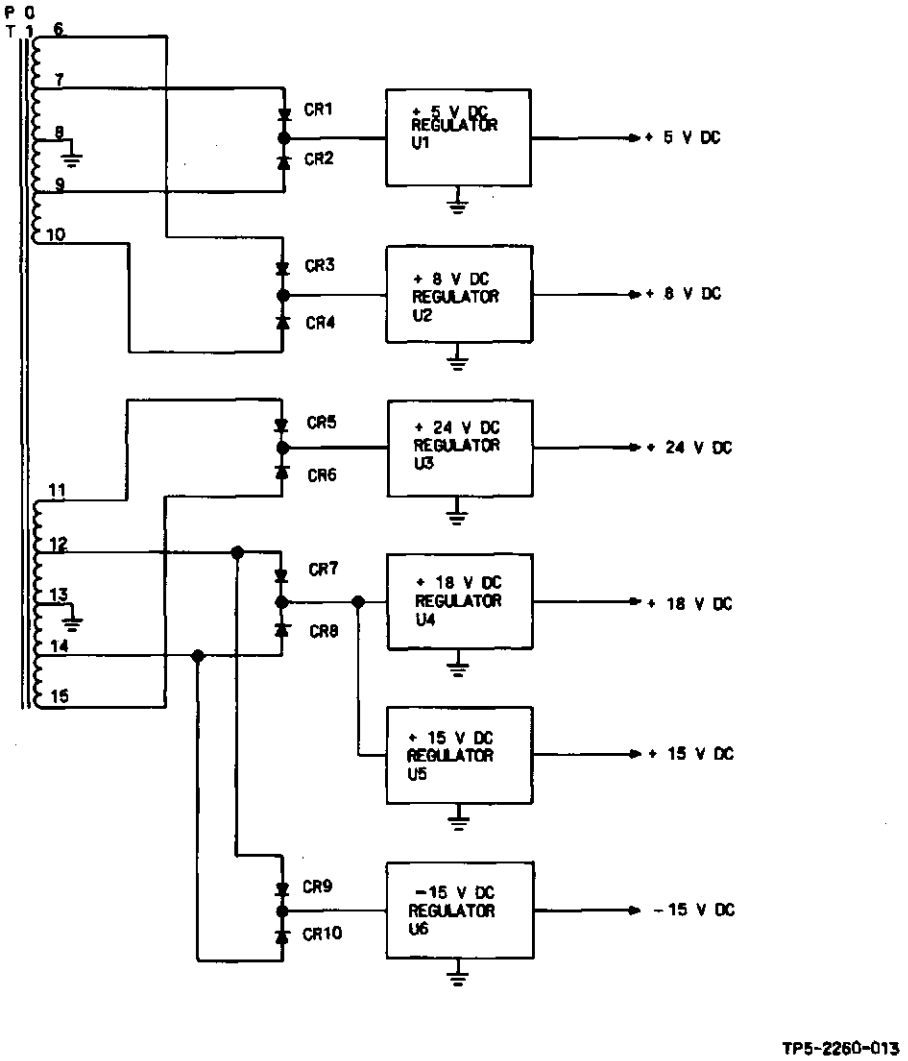
NOTICE: This section replaces first edition dated 1 June 1977.



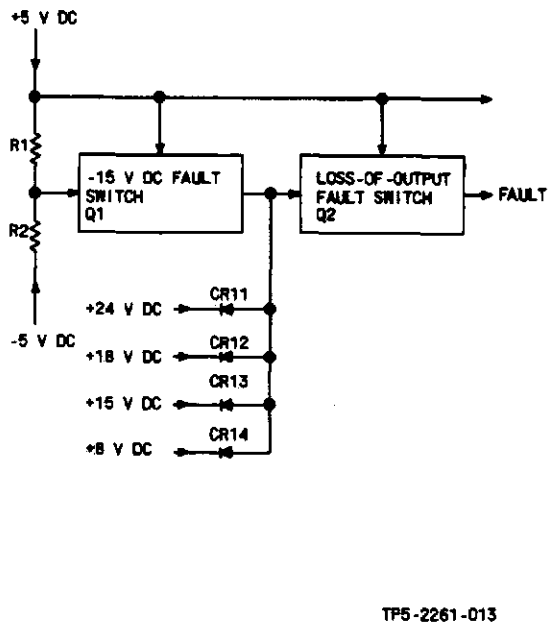
Power Supply, Block Diagram
Figure 2



Input Power Transformer Switching
Figure 3



Power Transformer, Rectifiers, and Regulators
Figure 4



Fault Summary
Figure 5

With all outputs normal, Q1 is cut off and +5 V dc is supplied through R4 and R6 to switch on Q2. This provides a logic 0 (ground) fault summary output, indicating all supplies are operating.

If the +5-V dc output decreases to a level low enough to cut off Q2, the logic 0 (ground) fault signal is removed and a logic 1 (open circuit) fault signal is supplied.

With +5 V dc at normal, if the -15-V dc output goes positive to a level at approximately -5 V dc or less, Q1 switches on and supplies a ground signal through R6 to cut off Q2. The logic 0 (ground) fault signal is removed and a logic 1 (+5-V dc) fault signal is supplied.

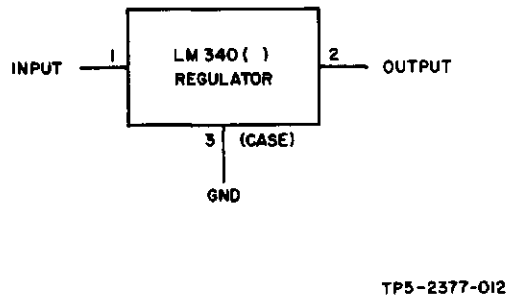
With +5 V dc at normal, if the +24-, +18-, +15-, or +8-V dc output falls below approximately +5 V dc, Q2 is cut off, the logic 0 (ground) fault signal is removed, and a logic 1 (+5-V dc) fault signal is supplied.

2.5 Voltage Regulators (Refer to figure 6 and to table 1.)

The LM340/320 series of three terminal regulators is available with several fixed output voltages, making them useful in a wide range of applications. One of these is local on-card regulation, eliminating the distribution problems associated with single-point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, and other solid-state electronic equipment. Although designed as fixed-voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

Table 1. Electrical Characteristics.

CHARACTERISTIC	LM340T-5/ 7805KC	LM340T-8/ 7808KC	LM340T-15/ 7815KC	LM320K-15	LM340T-18/ 7818KC	LM340T-24/ 7824KC
Max input voltage	35 V (except LM340T-24, 40 V)					
Operating temperature	0 to +70 °C (+32 to +158 °F)					
Storage temperature	-65 to +150 °C (-85 to +302 °F)					
Line regulation						
100 mA out	50 mV max	80 mV max	150 mV max	150 mV max	180 mV max	240 mV max
500 mA out	100 mV max	160 mV max	300 mV max	300 mV max	360 mV max	480 mV max
Output voltage	4.75 V min	7.6 V min	14.25 V min	14.25 V min	17.1 V min	22.8 V min
	5.25 V max	8.4 V max	15.75 V max	15.75 V max	18.9 V max	25.2 V max
Ripple rejection	60 dB typical	55 dB typical	50 dB typical	50 dB typical	48 dB typical	44 dB typical



Voltage Regulator
Figure 6

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the power supply module are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 2 check total performance of the power supply module. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

Table 2. Power Supply, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove bottom cover of unit containing power supply to be tested. **Note** For a quick check these loads need not be installed. Leave power supply connected in unit and perform all test procedures. b. Disconnect all output leads from A1TB1. c. Connect the following loads between A1TB1 pins indicated and A1TB1-5 (black wire). A1TB1- (WIRE COLOR) LOAD 7 (violet) 5 Ω 6 (blue) 10 Ω 1 (brown) 40 Ω 2 (red) 22 Ω 3 (orange) 15 Ω 8 (gray) 22 Ω		
2. LINE SELECTOR switch	a. Connect power supply to 50-V ac source and set power on. b. Measure dc voltage at A1E5 with LINE SELECTOR switch set at each of the following positions:		Check CR5, CR6, S1A, S1B, and T1.
(Cont)	100 V	14.8 to 16.0 V dc	

Table 2. Power Supply, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	115 V	13.0 to 14.0 V dc	
	215 V	6.9 to 7.5 V dc	
	230 V	6.5 to 7.0 V dc	
	c. Set power off and remove 50-V ac source.		
3. Output voltage	a. Connect power supply to 103-V ac source.		
	b. Set LINE SELECTOR switch to 115 V and set power on.		
	c. Measure dc voltage at each of the following outputs:		Check the following components and circuits associated with each:
	A1TB1-		
	7 (+5 V)	+4.8 to +5.2 V dc.	U1, CR1, CR2, and T1.
	6 (+8 V)	+7.6 to +8.4 V dc.	U2, CR3, CR4, and T1.
	1 (+24 V)	+23 to +25 V dc.	U3, CR5, CR6, and T1.
	2 (+18 V)	+15.5 to +18.7 V dc.	U4, CR7, CR8, and T1.
	3 (+15 V)	+14.4 to +15.6 V dc.	U5, CR7, CR8, and T1.
	8 (-15 V)	-14.6 to -15.4 V dc.	U6, CR9, CR10, and T1.
	d. Set power off. Disconnect 103-V ac source and connect power supply to 127-V ac source.		
	e. Set power on and measure dc voltage at each of the following outputs:		
	A1TB1-		
	7 (+5 V)	+4.8 to +5.2 V dc.	U1, CR1, CR2, and T1.
	6 (+8 V)	+7.6 to +8.4 V dc.	U2, CR3, CR4, and T1.
	1 (+24 V)	+23 to +25 V dc.	U3, CR5, CR6, and T1.
	2 (+18 V)	+17.3 to +18.7 V dc.	U4, CR7, CR8, and T1.
	3 (+15 V)	+14.4 to +15.6 V dc.	U5, CR7, CR8, and T1.
	8 (-15 V)	-14.6 to -15.6 V dc.	U6, CR9, CR10, and T1.
	f. Set power off and disconnect 127-V ac source.		

Table 2. Power Supply, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. Output ripple	a. Connect power supply to 103-V ac source.		
	b. Set LINE SELECTOR switch to 115 V and set power on.		
	c. Measure ac ripple voltage at each of the following outputs:		Check the following components and circuits associated with each.
	A1TB1-		
	7 (+5 V)	NMT 5 mV.	C14, CR1, CR2, and T1.
	6 (+8 V)	NMT 5 mV.	C15, CR3, CR4, and T1.
	1 (+24 V)	NMT 5 mV.	C16, CR5, CR6, and T1.
	2 (+18 V)	NMT 350 mV.	C17, CR7, CR8, and T1.
	3 (+15 V)	NMT 5 mV.	C18, CR7, CR8, and T1.
	8 (-15 V)	NMT 5 mV.	C18, CR9, CR10, and T1.
	d. Set power off. Disconnect 103-V ac source and connect power supply to 127-V ac source.		
	e. Set power on and measure ac ripple voltage at each of the following outputs:		
	A1TB1-		
	7 (+5 V)	NMT 5 mV.	C14, CR1, CR2, and T1.
	6 (+8 V)	NMT 5 mV.	C15, CR3, CR4, and T1.
	1 (+24 V)	NMT 5 mV.	C16, CR5, CR6, and T1.
	2 (+18 V)	NMT 5 mV.	C17, CR7, CR8, and T1.
	3 (+15 V)	NMT 5 mV.	C18, CR7, CR8, and T1.
	8 (-15 V)	NMT 5 mV.	C19, CR9, CR10, and T1.
	f. Set power off and disconnect 127-V ac source.		

Table 2. Power Supply, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. Fault	a. Connect power supply to 103-V ac source.	**Note**	
	b. Set LINE SELECTOR switch to 115 V and set power on.	There is no +5-V dc output fault indication in the power supply.	
	c. Measure dc output voltage at A1TB1-4 (fault) as each of the following dc output voltages is shorted to A1TB1-5 (ground).	+5-V dc output fault indicated by associated control card circuits and front-panel indicator.	Check the following components and circuits associated with each.
	Note Only one short applied at a time.		
	A1TB1-		
	7 (+5 V)	NMT 0.10 V dc.	R5, Q2, and Q1.
	6 (+8 V)	+4.5 to +5.5 V dc.	CR14.
	1 (+24 V)	+4.5 to +5.5 V dc.	CR11.
	2 (+18 V)	+4.5 to +5.5 V dc.	CR12.
	3 (+15 V)	+4.5 to +5.5 V dc.	CR13.
	8 (-15 V)	+4.5 to +5.5 V dc.	R1 and Q1.
	d. Measure dc output voltage at A1TB1-4 (fault) with no shorted outputs applied.	NMT 0.2 V dc.	R2, Q1, R4, R6, R3, and Q2.
	e. Check that all output voltages are restored when shorts are removed.		
	f. Set power off and disconnect 103-V ac source.		
6. Transformer regulation	a. Remove all output loads.		
	b. Connect power supply to 125-V ac source.		
	c. Set LINE SELECTOR switch to 115 V and set power on.		
	d. Measure dc voltage at CR5 and CR6 cathode.	NMT 15.0 V dc.	Check T1 and associated circuits.
	e. Set power off and disconnect 127-V ac source.		

4. REPAIR

Repair of the power supply module is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

5. PARTS LIST/DIAGRAMS

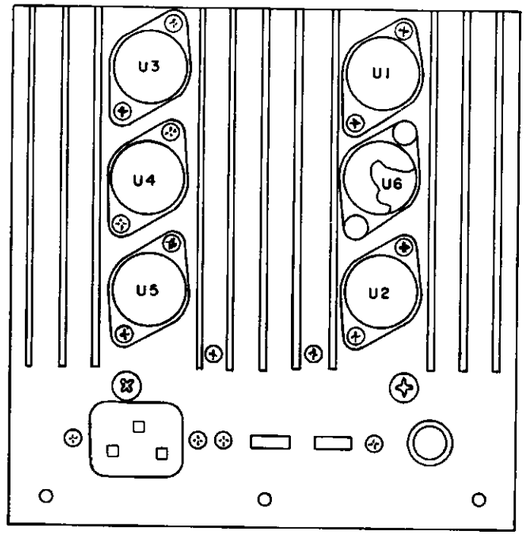
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram figure 7. The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

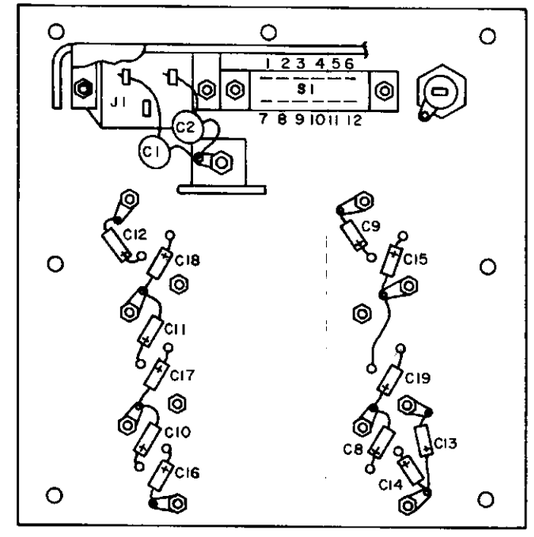
Use the reference designator indicated on the schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description is listed for each reference designator.

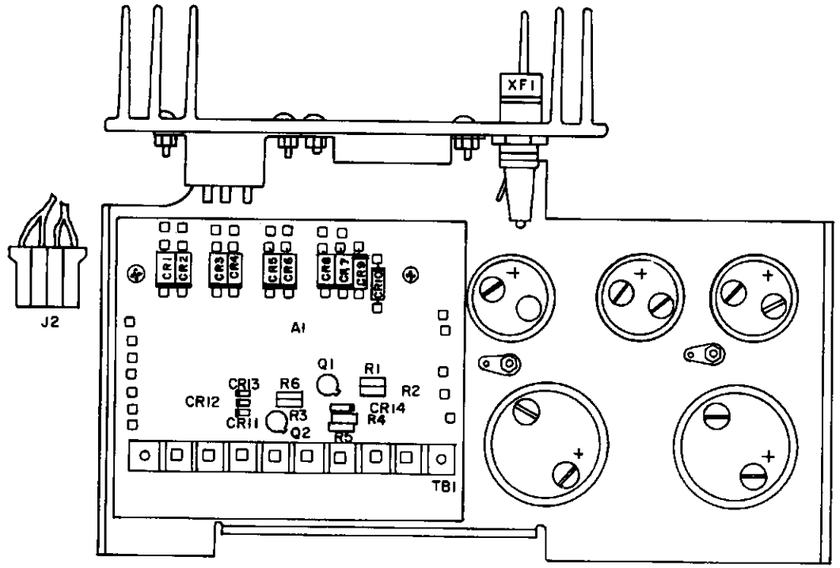
Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Power Supply Module	635-9649-001	REV C
Circuit Card A1	635-0903-001	REV A







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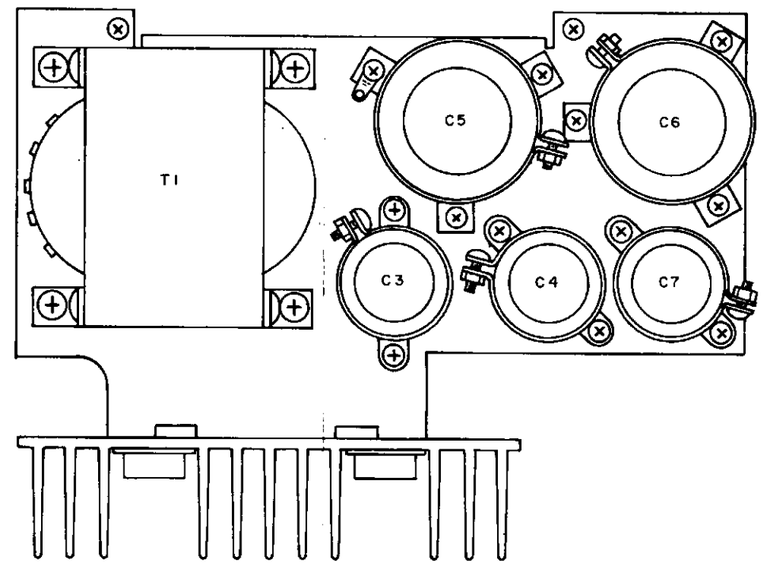


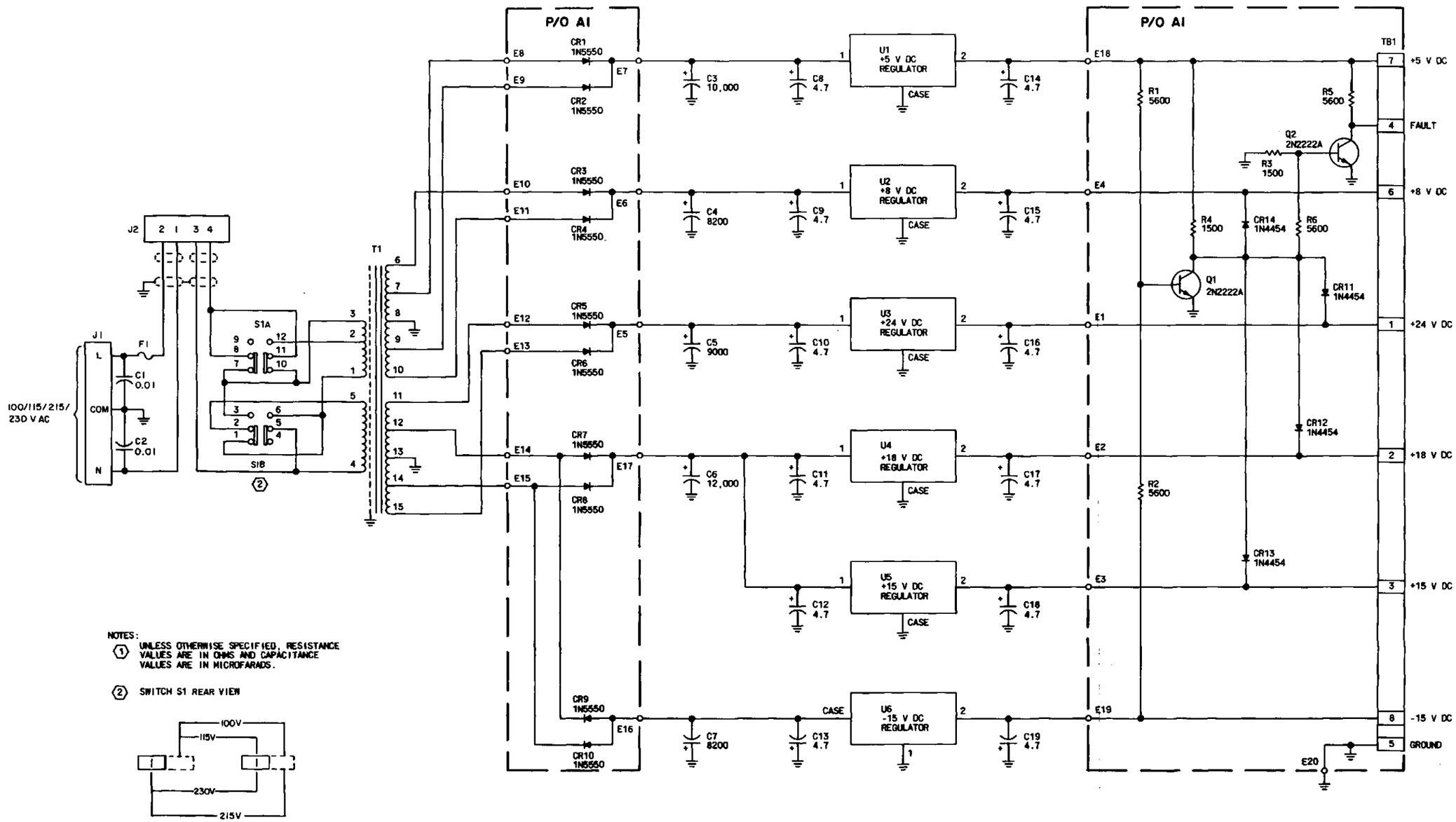
TP5-1021-029

Power Supply, Schematic Diagram
Figure 7 (Sheet 1 of 3)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	POWER SUPPLY 635-9649-001		
A1	POWER SUPPLY CARD	635-0903-001	
C1,C2	CAPACITOR,FXD,CER DIEL,10000pF,20%,500V	913-3013-000	
C3	CAPACITOR,FXD,ELCTLT,10000μF,-10%+100%,15V	183-1278-030	
C4	CAPACITOR,FXD,ELCTLT,8200μF,40%,50V	183-1278-580	
C5	CAPACITOR,FXD,ELCTLT,9000μF,-10%+100%,50V	183-1278-380	
C6	CAPACITOR,FXD,ELCTLT,12000μF,-10%+100%,40V	183-1278-190	
C7	CAPACITOR,FXD,ELCTLT,8200μF,40%,50V	183-1278-580	
C8-C19	CAPACITOR,FXD,ELCTLT,4.7μF,20%,50V	184-9067-560	
J1	CONNECTOR,RCPT,ELEC	368-0385-010	
J2	HOUSING,SOCKET	372-5884-490	
S1	SWITCH,SLIDE	266-0217-030	
T1	TRANSFORMER,PW	662-0805-010	
U1	INTEGRATED CKT,7805KC	351-1120-080	
U2	INTEGRATED CKT,7808KC	351-1120-100	
U3	INTEGRATED CKT,7824KC	351-1120-140	
U4	INTEGRATED CKT,7818KC	351-1120-130	
U5	INTEGRATED CKT,7815KC	351-1120-120	
U6	INTEGRATED CKT,LM320K15	351-1124-030	
XF1	FUSEHOLDER	265-1171-000	
	POWER SUPPLY CARD A1 635-0903-001		
CR1-CR10	SEMICOND DEVICE, 1N5550	353-3718-040	
CR11-CR14	SEMICOND DEVICE, 1N4454	353-3644-010	
Q1,Q2	TRANSISTOR,2N2222A	352-0661-020	
R1,R2	RESISTOR,FXD,CMPSN,5.6kω,10%,1/4W	745-0776-000	
R3,R4	RESISTOR,FXD,CMPSN,1.5kω,10%,1/4W	745-0755-000	
R5,R6	RESISTOR,FXD,CMPSN,5.6kΩ,10%,1/4W	745-0776-000	
TB1	TERMINAL BOARD	367-1599-070	

Power Supply, Schematic Diagram
Figure 7 (Sheet 2)



Power Supply, Schematic Diagram
Figure 7 (Sheet 3)

LED Status Display, 635-0825-( )

Rockwell International

instructions

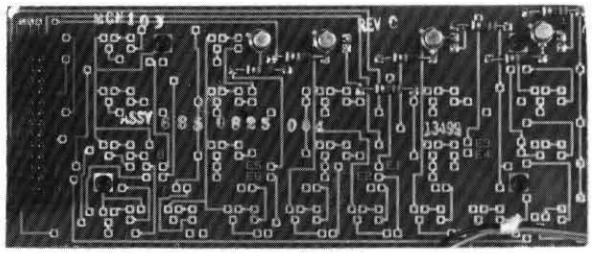
Collins Telecommunications Products Division

Printed in USA

523-0767946-002211
2nd Edition, 1 June 1978

1. DESCRIPTION

The LED Status Display 635-0825-( ), shown in figure 1, consists of up to 23 transistor-switch-controlled 5-V dc LED's. LED's are lighted when +5 V dc is applied at connector pin 25, a ground is applied at connector pin 16, and a positive voltage is applied to the connector pin associated with the individual LED. Refer to table 1 and figure 2 for signals (positive to light) and their associated connector pins and LED's.



TP5-2347-017

LED Status Display
Figure 1

2. TESTING/TROUBLESHOOTING PROCEDURES

2.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the LED status display are listed in the maintenance section of this instruction book.

2.2 Testing

The test procedures in table 2 check total performance of the LED status display. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

3. REPAIR

Repair of the LED status display is accomplished using the standard planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

NOTICE: This section replaces first edition dated 1 June 1977.

Table 1. LED Status Display, Configuration Matrix.

LED	APPLIED SIGNAL (SILKSCREEN IF DIFFERENT)	JUMPER	INPUT PIN (A2J3)	LED STATUS DISPLAY 635-0825-( )								
				-001	-002	-003	-004	-005	-006	-007	-008	-009
DS1	Sidetone en (RF OUT)		9		X	X		X	X	X		X
DS2	PA READY ind		10		X	X		X	X	X		X
DS3	PA FAULT ind		11		X	X		X	X	X		X
DS4	KEY ind		12		X	X		X	X	X		X
DS5	R/E FAULT ind		13			X			X			
DS5	RCV FAULT ind		13	X			X				X	
DS5	EXC TR FAULT ind		13		X			X		X		X
DS6	RCV OVERLOAD		14	X		X	X		X		X	
DS7	(Reserved)		15									
DS8	COUPLER FAULT ind		8		X	X		X	X	X		X
DS9	LSB (FL2)	R9 to E2	17		X	X						X
DS9	AM en	R9 to E1	4	X							X	
DS10	SSB en (SSB/CW)	R10 to E3	5	X							X	
DS10	CW en	R10 to E4	2		X	X						X
DS11	ISB en		1		X	X						X
DS12	USB (FL1)	R12 to E6	18		X	X						X
DS12	ISB en	R12 to E5	1	X							X	
DS13	AM en	R13 to E7		4		X	X					X
DS13	(Reserved)	R13 to E8	3									
DS14	16 (FL8)		24	X							X	
DS15	A (FL3)		22	X							X	
DS16	B (FL4)		21	X							X	
DS17	USB (FL1) (U)		18	X							X	
DS18	LSB (FL2) (L)		17	X							X	
DS19	C (FL5)		19	X							X	
DS20	D (FL6)		20	X							X	
DS21	E (FL7)		23	X							X	
DS22	BUSY		6	X	X	X						X
DS23	PRESEL FAULT ind		7	X		X	X		X	X	X	X

NOTES:

X indicates LED and associated circuit are installed in LED status display and any associated jumpers are installed.

A blank indicates LED and associated circuit are <u>not</u> installed in LED status display, and any associated jumpers are removed.

Table 2. LED Status Display, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of unit containing LED status display to be tested. b. If local unit, remove control card A10. Install A10 extender. If control unit, remove parallel output card A12. Install A12 extender. **Note** Control card A10 in local unit or parallel output card A12 in control unit is not installed during these tests. c. Connect a test lead to (+5 V dc). **Note** This test lead is used for biasing on the switching transistors.		
2. LED Status Display 635-0825-001 and 635-0825-008	a. Check that none of the LED's listed in step d are lighted before associated extender pin is connected to test lead. b. Check that each LED goes out when test lead is removed from associated extender pin. c. Connect test lead to extender pin indicated in step d and check that associated LED lights when test lead is connected.		
	d. EXTENDER PIN NO / A2J3 PIN NO / PANEL MARKING	ASSOCIATED LED	CHECK
	74 / 1 / ISB	DS12	DS12, Q12, R12, and R34.
	8 / 4 / AM	DS9	DS9, Q9, R9, R31, Q23, and R45.
	72 / 5 / SSB/CW	DS10	DS10, Q10, R10, and R32.
	7 / 6 / BUSY	DS22	DS22, Q22, R22, and R44.
	28 / 7 / PRESEL FAULT	DS23	DS23, Q24, R46, and R47.
	12 / 13 / RCV FAULT	DS5	DS5, Q5, R5, and R27.
	67 / 14 / RCV OVERLOAD	DS6	DS6, Q6, R6, and R28
(Cont)			

Table 2. LED Status Display, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE			NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	EXTENDER PIN NO	A2J3 PIN NO	PANEL MARKING	ASSOCIATED LED	CHECK
	97	17	L	DS18	DS18, Q18, R18, and R40.
	32	18	U	DS17	DS17, Q17, R17, and R39.
	34	19	C	DS19	DS19, Q19, R18, and R41.
	35	20	D	DS20	DS20, Q20, R20, and R42.
	98	21	B	DS16	DS16, Q16, R16, and R38.
	33	22	A	DS15	DS15, Q15, R15, and R37.
	99	23	E	DS21	DS21, Q21, R21, and R43.
	100	24	16	DS14	DS14, Q14, R14, and R36.
	e. Connect +5 V dc to extender pin 8 (A2J3-4).			DS9 (AM) lights.	DS9, Q9, R9, R31, Q23, and R45.
	f. Connect test lead to extender pin 74 (A2J3-1).			DS12 (ISB) lights and DS9 (AM) goes out.	DS12, Q12, R12, and R24. Q23 and R45.
	g. Remove +5 V dc from extender pin 8 and test lead from extender pin 74.				
3. LED Status Display 635-0825-002	a. Check that none of the LED's listed in step d are lighted before associated extender pin is connected to test lead.				
	b. Check that each LED goes out when test lead is removed from associated extender pin.				
	c. Connect test lead to extender pin indicated in step d and check that associated LED lights when test lead is connected.				
	d. EXTENDER PIN NO	A2J3 PIN NO	PANEL MARKING	ASSOCIATED LED	CHECK
	74	1	ISB	DS11	DS11, Q11, R11, and R33.
	9	2	CW	DS10	DS10, Q10, R10, and R32.
(Cont)	8	4	AM	DS13	DS13, Q13, R13, and R35.

Table 2. LED Status Display, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE			NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	EXTENDER PIN NO	A2J3 PIN NO	PANEL MARKING	ASSOCIATED LED	CHECK
	7	6	BUSY	DS22	DS22, Q22, R22, and R44.
	13	8	COUPLER FAULT	DS8	DS8, Q8, R8, and R30.
	5	9	RF OUT	DS1	DS1, Q1, R1, and R23.
	69	10	PA READY	DS2	DS2, Q2, R2, and R24.
	77	11	PA FAULT	DS3	DS3, Q3, R3, and R25.
	68	12	KEY	DS4	DS4, Q4, R4, and R26.
	12	13	EXCTR FAULT	DS5	DS5, Q5, R5, and R27.
	97	17	LSB	DS9	DS9, Q9, R9, Q23, and R45.
	32	18	USB	DS12	DS12, Q12, R12, and Q34.
	e. Connect +5 V dc to extender pin 97 (A2J3-17)			DS9 (LSB) lights.	DS9, Q9, R9, R31, Q23, and R45.
	f. Connect test lead to extender pin 74 (A2J3-1).			DS11 (ISB) lights and DS9 (LSB) goes out.	DS11, Q11, R11, and R33. Q23 and R45.
	g. Remove +5 V dc from extender pin 97 and test lead from extender pin 74.				
4. LED Status Display 635-0825-003 (Cont)	a. Check that none of the LED's listed in step d are lighted before associated extender pin is connected to test lead.				
	b. Check that each LED goes out when test lead is removed from associated extender pin.				
	c. Connect test lead to extender pin indicated in step d and check that associated LED lights when test lead is connected.				

Table 2. LED Status Display, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE			NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	EXTENDER PIN NO	A2J3 PIN NO	PANEL MARKING	ASSOCIATED LED	CHECK
	74	1	ISB	DS11	DS11, Q11, R11, and R33.
	9	2	CW	DS10	DS10, Q10, R10, and R32.
	8	4	AM	DS13	DS13, Q13, R13, and R35.
	7	6	BUSY	DS22	DS22, Q22, R22, and R44.
	28	7	PRESEL	DS23	DS23, Q24, R46, and R47.
	13	8	COUPLER FAULT	DS8	DS8, Q8, R8, and R30.
	5	9	RF OUT	DS1	DS1, Q1, R1, and R23.
	69	10	PA READY	DS2	DS2, Q2, R2, and R24.
	77	11	PA FAULT	DS3	DS3, Q3, R3, and R25.
	68	12	KEY	DS4	DS4, Q4, R4, and R26.
	12	13	R/E FAULT	DS5	DS5, Q5, R5, and R27.
	67	14	RCV OVERLOAD	DS6	DS6, Q6, R6, and R28.
	97	17	LSB	DS9	DS9, Q9, R9, R31, Q23, and R45.
	32	18	USB	DS12	DS12, Q12, R12, and Q34.
	e. Connect +5 V dc to extender pin 97 (A2J3-17).			DS9 (LSB) lights.	DS9, Q9, R9, R31, Q23, and R45.
	f. Connect test leads to extender pin 74 (A2J3-1).			DS11 (ISB) lights and DS9 (LSB) goes out.	DS11, Q11, R11, and R33. Q23 and R45.
	g. Remove +5 V dc from extender pin 97 and test lead from extender pin 74.				
5. LED Status Display 635-0825-004 (Cont)	a. Check that none of the LED's listed in step d are lighted before associated extender pin is connected to test lead.				
	b. Check that each of the LED's go out when test lead is removed from associated extender pin.				

Table 2. LED Status Display, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE			NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	c. Connect test lead to extender pin indicated in step d and check that associated LED lights when test lead is connected.				
	d. EXTENDER PIN NO	A2J3 PIN NO	PANEL MARKING	ASSOCIATED LED	CHECK
	71	7	PRESEL FAULT	DS23	DS23, Q24, R46, and R47.
	3	13	RCV FAULT	DS5	DS5, Q5, R5, and R27.
	67	14	RCV OVERLOAD	DS6	DS6, Q6, R6, and R28.
6. LED Status Display 635-0825-005	a. Check that none of the LED's listed in step d are lighted before associated extender pin is connected to test lead.				
	b. Check that each LED goes out when test lead is removed from associated extender pin.				
	c. Connect test lead to extender pin indicated in step d and check that the associated LED lights when test lead is connected.				
	d. EXTENDER PIN NO	A2J3 PIN NO	PANEL MARKING	ASSOCIATED LED	CHECK
	70	8	COUPLER FAULT	DS8	DS8, Q8, R8, and R30.
	5	9	RF OUT	DS1	DS1, Q1, R1, and R23.
	69	10	PA READY	DS2	DS2, Q2, R2, and R24.
	4	11	PA FAULT	DS3	DS3, Q3, R3, and R25.
	68	12	KEY	DS4	DS4, Q4, R4, and R26.
	3	13	EXCTR FAULT	DS5	DS5, Q5, R5, and R27.
7. LED Status 635-0825-006	a. Check that none of the LED's listed in step d are lighted before associated extender pin is connected to test lead.				
(Cont)	b. Check that each LED goes out when test lead is removed from extender associated extender pin.				

Table 2. LED Status Display, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE			NORMAL INDICATION	IF INDICATION IS ABNORMAL
7. (Cont)	c. Connect test lead to extender pin indicated in step d and check that associated LED lights when test lead is connected.				
	d. EXTENDER PIN NO	A2J3 PIN NO	PANEL MARKING	ASSOCIATED LED	CHECK
	71	7	PRESEL FAULT	DS23	DS23, Q24, R46, and R47.
	70	8	COUPLER FAULT	DS8	DS8, Q8, R8, and R30.
	5	9	RF OUT	DS1	DS1, Q1, R1, and R23.
	69	10	PA READY	DS2	DS2, Q2, R2, and R24.
	4	11	PA FAULT	DS3	DS3, Q3, R3, and R25.
	68	12	KEY	DS4	DS4, Q4, R4, and R26.
	3	13	R/E FAULT	DS5	DS5, Q5, R5, and R27.
	67	14	RCV OVERLOAD	DS6	DS6, Q6, R6, and R28.
8. LED Status Display 635-0825-007	a. Check that none of the LED's listed in step d are lighted before associated extender pin is connected to test lead.				
	b. Check that each LED goes out when test lead is removed from associated extender pin.				
	c. Connect test lead to extender pin indicated in step d and check that associated LED lights when test lead is connected.				
	d. EXTENDER PIN NO	A2J3 PIN NO	PANEL MARKING	ASSOCIATED LED	CHECK
	71	7	PRESEL FAULT	DS23	DS23, Q24, R46, and R47.
	70	8	COUPLER FAULT	DS8	DS8, Q8, R8, and R30.
	5	9	RF OUT	DS1	DS1, Q1, R1, and R23.
	69	10	PA READY	DS2	DS2, Q2, R2, and R24.
	4	11	PA FAULT	DS3	DS3, Q3, R3, and R25.
	68	12	KEY	DS4	DS4, Q4, R4, and R26.
	3	13	EXCTR FAULT	DS5	DS5, Q5, R5, and R27.

Table 2. LED Status Display, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE			NORMAL INDICATION	IF INDICATION IS ABNORMAL
9. LED Status Display 635-0825-009	a. Check that none of the LED's listed in step d are lighted before associated extender pin is connected to test lead.				
	b. Check that each LED goes out when test lead is removed from associated extender pin.				
	c. Connect test lead to extender pin indicated in step d and check that associated LED lights when test lead is connected.				
	d. EXTENDER PIN NO	A2J3 PIN NO	PANEL MARKING	ASSOCIATED LED	CHECK
	74	1	ISB	DS11	DS11, Q11, R11, and R33.
	9	2	CW	DS10	DS10, Q10, R10, and R32.
	8	4	AM	DS13	DS13, Q13, R13, and R35.
	7	6	BUSY	DS22	DS22, Q22, R22, and R44.
	71	7	PRESEL FAULT	DS23	DS23, Q24, R46, and R47.
	70	8	COUPLER FAULT	DS8	DS8, Q8, R8, and R30.
	5	9	RF OUT	DS1	DS1, Q1, R1, and R23.
	69	10	PA READY	DS2	DS2, Q2, R2, and R24.
	4	11	PA FAULT	DS3	DS3, Q3, R3, and R25.
	68	12	KEY	DS4	DS4, Q4, R4, and R26.
	3	13	EXCTR FAULT	DS5	DS5, Q5, R5, and R27.
	97	17	LSB	DS9	DS9, Q9, R9, Q23, and R45.
	32	18	USB	DS12	DS12, Q12, R12, and Q34.
(Cont)					

Table 2. LED Status Display, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
9. (Cont)	e. Connect +5 V dc to extender pin 97 (A2J3-17).	DS9 (LSB) lights.	DS9, Q9, R9, R31, Q23, and R45.
	f. Connect test lead to extender pin 74 (A2J3-1).	DS11 (ISB) lights and DS9 (LSB) goes out.	DS11, Q11, R11, and R33. Q23 and R45.
	g. Remove +5 V dc from extender pin 97 and test lead from extender pin 74.		

4. PARTS LIST/DIAGRAMS

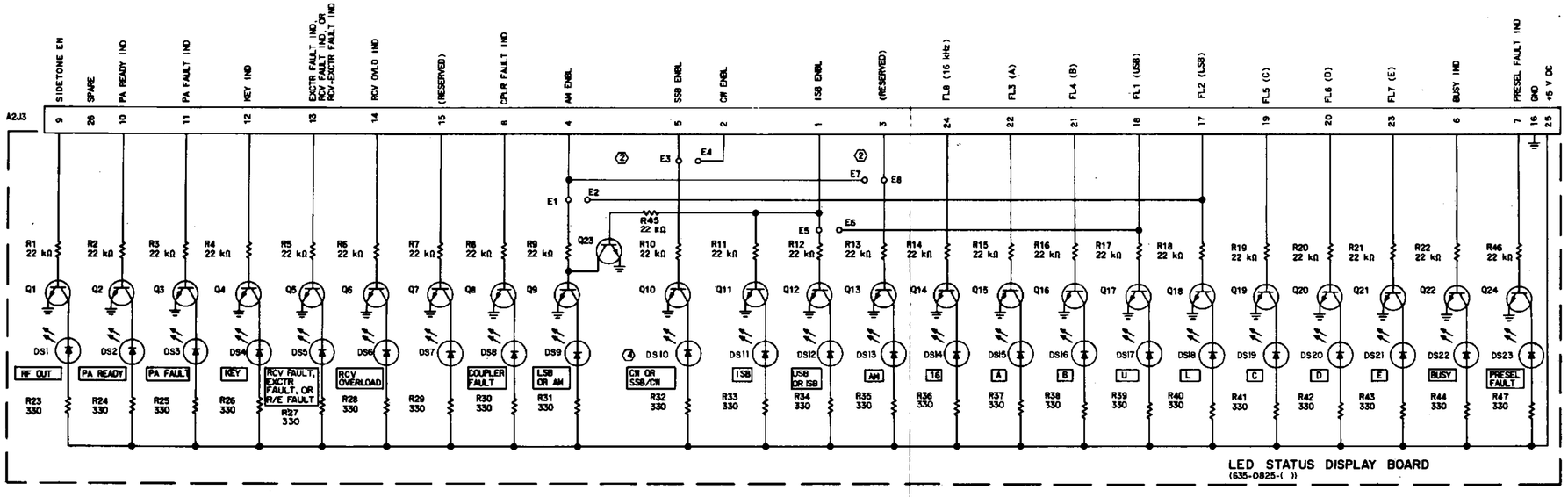
This paragraph assists in identification, requisition, and issuance of parts, and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram, figure 2. The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on the schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description is listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list, in parentheses, and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

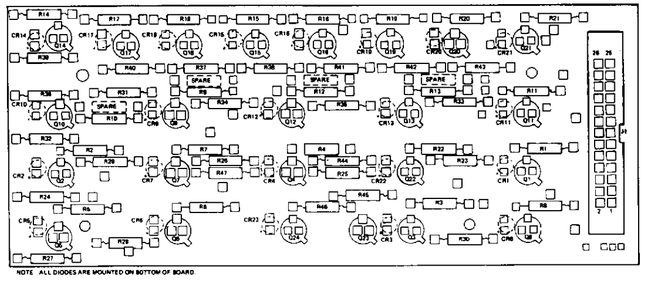
Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
LED status display	635-0825-001	REV C
LED status display	635-0825-002	REV D
LED status display	635-0825-003	REV D
LED status display	635-0825-004	REV C
LED status display	635-0825-005	REV C
LED status display	635-0825-006	REV C
LED status display	635-0825-007	REV G
LED status display	635-0825-008	REV —
LED status display	635-0825-009	REV H



NOTES:

1. Q1-Q24 ARE TYPE 2N2222A.
   DS3, DS5, DS6, DS8 AND DS23 ARE TYPE HP5082-4684 (RED) LED.
   DS1, DS2, DS4, DS7, AND DS9-DS22 ARE TYPE HP5082-4584 (YELLOW) LED.
2. FOR RECEIVER CONTROL UNITS, CONNECT R9 TO E1, R10 TO E3, R12 TO E5, R13 TO E8.
   FOR EXCITER OR RECEIVER/EXCITER CONTROL UNITS, CONNECT R9 TO E2, R10 TO E4, R12 TO E6, R13 TO E7.
3. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS.



TPS-1156-019

TPA-0155-024

LED Status Display, Schematic Diagram
Figure 2 (Sheet 1 of 2)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	INDICATOR BOARD A2A1 635-0825-001		
DS1-DS4	NOT USED		
DS5, DS6	DIODE, LE 5082-4684	353-0232-030	
DS7, DS8	NOT USED		
DS9-DS10	DIODE, LE 5082-4584	353-0232-010	
DS11	NOT USED		
DS12	DIODE, LE, 5082-4584	353-0232-010	
DS13	NOT USED		
DS14-DS22	DIODE, LE, 5082-4584	353-0232-010	
DS23	DIODE, LE, 5082-4684	353-0232-030	
Q1-Q4	NOT USED		
Q5, Q6	TRANSISTOR, 2N2222A	352-0661-020	
Q7, Q8	NOT USED		
Q9, Q10	TRANSISTOR, 2N2222A	352-0661-020	
Q11	NOT USED		
Q12	TRANSISTOR, 2N2222A	352-0661-020	
Q13	NOT USED		
Q14-Q24	TRANSISTOR, 2N2222A	352-0661-020	
R1-R4	NOT USED		
R5, R6	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R7, R8	NOT USED		
R9, R10	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R11	NOT USED		
R12	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R13	NOT USED		
R14-R22	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R23-R26	NOT USED		
R27, R28	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R29, R30	NOT USED		
R31, R32	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R33	NOT USED		
R34	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R35	NOT USED		
R36-R44	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R45, R48	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R47	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
	INDICATOR BOARD A2A1 635-0825-002		
DS1, DS2	DIODE, LE, 5082-4582	353-0232-010	
DS3	DIODE, LE, 5082-4684	353-0232-030	
DS4	DIODE, LE, 5082-4584	353-0232-010	
DS5	DIODE, LE, 5082-4684	353-0232-030	
DS6, DS7	NOT USED		
DS8	DIODE, LE, 5082-4684	353-0232-030	
DS9-DS13	DIODE, LE, 5082-4584	353-0232-010	
DS14-DS21	NOT USED		
DS22	DIODE, LE, 5082-4584	353-0232-010	
Q1-Q5	TRANSISTOR, 2N2222A	352-0661-020	
Q6, Q7	NOT USED		
Q8-Q13	TRANSISTOR, 2N2222A	352-0661-020	
Q14-Q21	NOT USED		
Q22, Q23	TRANSISTOR, 2N2222A	352-0661-020	
R1-R5	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R6,R7	NOT USED		
R8-R13	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R14-R21	NOT USED		
R22	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R23-R27	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R28, R29	NOT USED		
R30-R35	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R36-R43	NOT USED		
R44	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R45	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
	INDICATOR BOARD A2A1 635-0825-003		
DS1, DS2	DIODE, LE, 5082-4584	353-0232-010	
DS3	DIODE, LE, 5082-4684	353-0232-030	
DS4	DIODE, LE, 5082-4584	353-0232-010	

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART	USABLE ON CODE
DS5, DS6	DIODE, LE, 5082-4684	353-0232-030	
DS7	NOT USED		
DS8	DIODE, LE, 5082-4684	353-0232-030	
DS9-DS13	DIODE, LE, 5082-4584	353-0232-010	
DS14-DS21	NOT USED		
DS22	DIODE, LE, 5082-4584	353-0232-010	
DS23	DIODE, LE, 5082-4684	353-0232-030	
Q1-Q6	TRANSISTOR, 2N2222A	352-0661-020	
Q7	NOT USED		
Q8-Q13	TRANSISTOR, 2N2222A	352-0661-020	
Q14-Q21	NOT USED		
Q22-Q24	TRANSISTOR, 2N2222A	352-0661-020	
R1-R6	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R7	NOT USED		
R8-R13	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R14-R21	NOT USED		
R22	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R23-R28	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R29	NOT USED		
R30-R35	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R36-R43	NOT USED		
R44	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R45, R46	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R47	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
	INDICATOR BOARD A2A1 635-0825-004		
DS1-DS4	NOT USED		
DS5, DS6	DIODE, LE, 5082-4684	353-0232-030	
DS7-DS22	NOT USED		
DS23	DIODE, LE, 5082-4684	353-0232-030	
Q1-Q4	NOT USED		
Q5, Q6	TRANSISTOR, 2N2222A	352-0661-020	
Q7-Q23	NOT USED		
Q24	TRANSISTOR, 2N2222A	352-0661-020	
R1-R4	NOT USED		
R5, R6	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R7-R26	NOT USED		
R27, R28	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R29-R45	NOT USED		
R46	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R47	RESISTOR, FSD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
	INDICATOR BOARD A2A1 635-0825-005		
DS1, DS2	DIODE, LE, 5082-4584	353-0232-010	
DS3	DIODE, LE, 5082-4684	353-0232-030	
DS4	DIODE, LE, 5082-4584	353-0232-010	
DS5	DIODE, LE, 5082-4684	353-0232-030	
DS6, DS7	NOT USED		
DS8	DIODE, LE, 5082-4684	353-0232-030	
Q1-Q5	TRANSISTOR, 2N2222A	352-0661-020	
Q6, Q7	NOT USED		
Q8	TRANSISTOR, 2N2222A	352-0661-020	
R1-R5	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R6, R7	NOT USED		
R8	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R9-R22	NOT USED		
R23-R27	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R28, R29	NOT USED		
R30	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
	INDICATOR BOARD A2A1 635-0825-006		
DS1, DS2	DIODE, LE, 5082-4584	353-0232-010	
DS3	DIODE, LE, 5082-4684	353-0232-030	
DS4	DIODE, LE, 5082-4584	353-0232-010	
DS5, DS6	DIODE, LE, 5082-4684	353-0232-030	
DS7	NOT USED		
DS8	DIODE, LE, 5082-4684	353-0232-030	
DS9-DS22	NOT USED		

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
DS23	DIODE, LE, 5082-4684	353-0232-030	
Q1-Q6	TRANSISTOR, 2N2222A	352-0661-020	
Q7	NOT USED		
Q8	TRANSISTOR, 2N2222A	352-0661-020	
Q9-Q23	NOT USED		
Q24	TRANSISTOR, 2N2222A	352-0661-020	
R1-R6	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R7	NOT USED		
R8	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R9-R22	NOT USED		
R23-R28	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R29	NOT USED		
R30	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R31-R45	NOT USED		
R46	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R47	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
	LED STATUS DISPLAY 635-0825-008		
DS1-DS4	NOT USED		
DS5, DS6	DIODE, LE, 5082-4684	353-0232-030	
DS7, DS8	NOT USED		
DS9, DS10	DIODE, LE, 5082-4584	353-0232-010	
DS11	NOT USED		
DS12	DIODE, LE, 5082-4584	353-0232-010	
DS13	NOT USED		
DS14-DS21	DIODE, LE, 5082-4584	353-0232-010	
DS22	NOT USED		
DS23	DIODE, LE, 5082-4684	353-0232-030	
Q1-Q4	NOT USED		
Q5, Q6	TRANSISTOR, 2N2222A	352-0661-020	
Q7, Q8	NOT USED		
Q9, Q10	TRANSISTOR, 2N2222A	352-0661-020	
Q11	NOT USED		
Q12	TRANSISTOR, 2N2222A	352-0661-020	
Q13	NOT USED		
Q14-Q21	TRANSISTOR, 2N2222A	352-0661-020	
Q22	NOT USED		
Q23, Q24	TRANSISTOR, 2N2222A	352-0661-020	
R1-R4	NOT USED		
R5, R6	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R7, R8	NOT USED		
R9, R10	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R11	NOT USED		
R12	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R13	NOT USED		
R14-R21	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R22-R26	NOT USED		
R27, R28	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R29, R30	NOT USED		
R31, R32	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R33	NOT USED		
R34	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R35	NOT USED		
R36-R43	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R44	NOT USED		
R45, R46	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R47	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
	LED STATUS DISPLAY 635-0825-007		
DS1, DS2	DIODE, LE, 5082-4584	353-0232-010	
DS3	DIODE, LE, 5082-4684	353-0232-030	
DS4	DIODE, LE, 5082-4584	353-0232-010	
DS5	DIODE, LE, 5082-4684	353-0232-030	
DS6, DS7	NOT USED		
DS8	DIODE, LE, 5082-4684	353-0232-030	
DS9-DS22	NOT USED		
DS23	DIODE, LE, 5082-4684	353-0232-030	
Q1-Q5	TRANSISTOR, 2N2222A	352-0661-020	

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
Q6, Q7	NOT USED		
Q8	TRANSISTOR, 2N2222A	352-0661-020	
Q9-Q23	NOT USED		
Q24	TRANSISTOR, 2N2222A	352-0661-020	
R1-R5	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R6, R7	NOT USED		
R8	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R9-R22	NOT USED		
R23-R27	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R28, R29	NOT USED		
R30	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R31-R45	NOT USED		
R46	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R47	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
	LED STATUS DISPLAY 635-0825-009		
DS1, DS2	DIODE, LE, 5082-4584	353-0232-010	
DS3	DIODE, LE, 5082-4684	353-0232-030	
DS4	DIODE, LE, 5082-4584	353-0232-010	
DS5	DIODE, LE, 5082-4684	353-0232-030	
DS6, DS7	NOT USED		
DS8	DIODE, LE, 5082-4684	353-0232-030	
DS9-DS13	DIODE, LE, 5082-4584	353-0232-010	
DS14-DS21	NOT USED		
DS22	DIODE, LE, 5082-4584	353-0232-010	
DS23	DIODE, LE, 5082-4684	353-0232-030	
Q1-Q5	TRANSISTOR, 2N2222A	352-0661-020	
Q6, Q7	NOT USED		
Q8-Q13	TRANSISTOR, 2N2222A	352-0661-020	
Q14-Q21	NOT USED		
Q22-Q24	TRANSISTOR, 2N2222A	352-0661-020	
R1-R5	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R6, R7	NOT USED		
R8-R13	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R14-R21	NOT USED		
R22	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R23-R27	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R28, R29	NOT USED		
R30-R35	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R36-R43	NOT USED		
R44	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
R45, R46	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R47	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	

LED Status Display, Schematic Diagram
Figure 2 (Sheet 2)

Count/Store Assembly (638-6063-001)

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

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1. DESCRIPTION

The Count/Store Assembly 638-6063-001, shown in figure 1, is a two-layer circuit board using a ribbon-type cable connector. The count/store assembly consists of the following functional circuits: 500- to 600-Hz oscillator, divide-by-64 divider, frequency change rate counter, frequency change rate storage register, dial lock circuit, and an up/down change control.

(To Be Supplied)

1.1 Optical Tuning Switch Assembly (610-2150-001)

The Optical Tuning Switch Assembly, Collins part number 610-2150-001, shown in figure 2, contains two boards, a lens ring, and a control knob. The emitter board contains a photoemissive device, the detector board contains a photosensitive device, and a lens ring coupled to the control knob separates the two boards. The detector board contains two clock generators to develop an up/down signal and a rate change signal.

Count/Store Assembly
Figure 1

2. PRINCIPLES OF OPERATION

2.1 General (Refer to figure 3.)

The count/store assembly receives two clock signals which are frequency direction phase-shifted, a local enable input, a dial lock input, and a clock inhibit input; and provides fire bcd rate control outputs and an up/down signal output.

(To Be Supplied)

The optical tuning switch assembly provides two output clock signals. The directional that the control knob (front-panel TUNING knob) is tuned determines the phase-relationship of the clock signals.

Optical Tuning Switch Assembly
Figure 2

2.2 Up/Down Control

When the front-panel TUNING knob is tuned in a clockwise direction, clock B leads clock A; thus, clock B is positive when the positive going edge of clock A appears. U6A is set by the logic 1 at U6A-D when U6A is clocked and provides a logic 1 up/$\overline{\text{down}}$ (up) signal to U4-D2.

When the front-panel TUNING knob is turned in a counterclockwise direction, clock A leads clock B; thus, clock B is negative when the positive going edge of clock A appears. U6A is reset by the logic 0 at U6A-D when U6A is clocked and provides a logic 0 up/$\overline{\text{down}}$ (down) signal to U4-D2.

2.3 Rate Control

Rate control outputs are controlled by the frequency with which clock A pulses are applied to the count/store assembly. Clock A pulses are supplied through clock gate U11D, count/store inhibit gate U10C, and applied to the oscillator/clock-window circuit. Clock-window gate U11B is enabled at an 8- to 10-Hz rate with a 100- to 120-ms pulse. During the elapsed time (100 to 120 ms) of the clock window, the rate counter U2 counts the number of clock pulses until the clock window is removed. The output of counter is coupled through storage register U3/U4 to the rate outputs.

The rate that pulses can be applied using the optical tuning switch assembly is 0 to approximately 270 Hz. (There are 90 pulses applied per rotation of the control knob, and maximum rotation speed is approximately 3 turns per second.)

Clock gate U11D provides an output pulse only when a logic 1 input is first applied. If a steady logic 1 or logic 0 input was applied, the output of U11D would go to logic 1 after the RC time constant of R1-C1 had elapsed. This device causes a logic 1 output to be supplied from U11D with any fixed logic level input.

Count/store inhibit gate U10C prevents clock pulses from being applied if: (1) +5-V dc power has just been applied, (2) +5- and +15-V dc power is $\overline{\text{up to power}}$, (3) a $\overline{\text{dial lock}}$ signal is applied, and (4) a $\overline{\text{clock inhibit}}$ signal is applied. When all of the preceding conditions are initiated, U10C is enabled and U3/U4 is enabled.

When U10C is enabled, clock pulses are supplied through U10C to U7D (rate window gate) and U11B (rate count gate).

In the inactive state (no clock pulses applied), the following conditions are set up in the rate window and rate count circuits. U9 count is latched; that is, count 64 at Q7 is logic 1 which inhibits counter oscillator gate U10A and prevents further counting of U9. U8D output is logic 0 which causes U10B output to go to logic 1, enabling U7D (rate window gate) to receive a clock pulse. The logic 0 U8D output also causes output of U10D to go to logic 1 setting U6B. The output of U6B goes to logic 0 and U7C goes to logic 1, enabling reset gate U1B. The logic 1 output of U10D also resets rate count of U2 to 0.

When clock pulse is applied to U7D, it is transferred through U7D and U1B and resets U9. The output at U9-Q7 goes to logic 0, and counter oscillator gate U10A is enabled; U9 is clocked (and counts) at a 500- to 650-Hz rate through 64 counts. While counter U9 is counting through 64, a clock window is developed by U8D and U11B which allows input clock pulses to be applied through U11B and U5C to U2. Up to 31 counts can be applied to U2 in this window before clock inhibit gate U5C is inhibited by AND gate circuit (U5D, U1A, U1C). When 64 clocks are received by rate window counter U9, the rate window and rate count circuits are reset and the count starts over from 0.

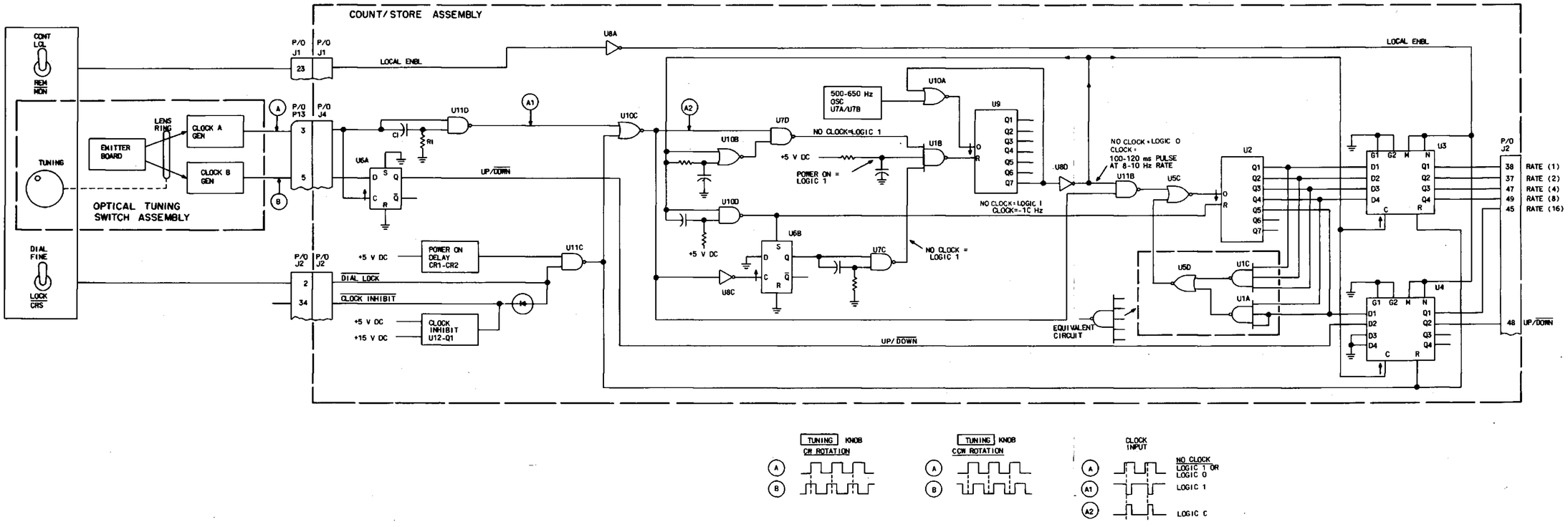
3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test and troubleshoot the count/store assembly and the optical tuning switch assembly are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 1 check the total performance of the count/store assembly. The test procedures in table 2 check the total performance of the optical tuning switch assembly. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.



TPA-0797-015

Count/Store Assembly and Optical Tuning Switch Assembly, Block Diagram
Figure 3

Table 1. Count/Store Assembly, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	**Note** In these testing and troubleshooting procedures, two TTL logic level, square wave pulse train inputs to the count-store assembly (clock A and clock B) are required. The two pulse trains must be displaced by 90 ±20 degrees, with clock A lagging clock B for an up count, and clock A leading clock B for a down count. Circuits to generate the two square wave pulse trains may be incorporated into a test fixture so that only a single external pulse generator is required. a. Remove top and bottom cover of unit containing the count/store assembly that is to be tested. b. Disconnect P13 that connects count/store assembly J4 to optical tuning switch assembly. **Note** Upon completion of count/store assembly testing, reconnect P13 and J4. c. Set unit LINE SELECTOR for power source available (100/115/215/230 V ac). **Note** Ensure that proper fuse is installed for power source used. d. Connect unit to available power source.		
2. Initial checks	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to any. BANDWIDTH to any. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw. b. Measure dc voltages between the following points and ground (TP1): J2-10 J2-16 J4-1	 +15 ±1.0 V dc. +5 ±0.5 V dc. +5 ±0.5 V dc.	 Check associated power supply.

Table 1. Count/Store Assembly, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. Count window oscillator	a. Front-panel controls set as follows: PWR to on. COUNT to LCL. MODE to any. BANDWIDTH to any. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Connect clock A, set at 25 Hz, to J4-3 (clock A, count) and clock B, set at 25 Hz, to J4-5 (clock B, up/down).		
	c. Measure the count window oscillator frequency at U7B-4.	545 to 665 Hz	Check U7A, U7B, and associated circuit.
	d. Measure pulse width of count window at TP2.	120 to 100 ms.	Check U11D, U10C, U7D, U1B, U10A, U9, and associated circuits.
	e. Remove clock A and clock B inputs from J4-3 and J4-5.		
	f. Measure voltage level at TP2.	NLT +3.0 V dc.	Same as step 3.d.
4. Counter weight	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to any. BANDWIDTH to any. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Connect clock A, set at 25 Hz to J4-3 (clock A, count) and clock B, set at 25 Hz, to J4-5 (clock B, up/down).		
	c. Vary the input clock frequency and measure the input frequency required to maintain a steady logic 1 (NLT +3.0 V dc) output on only one of each of the counter weight outputs.		If test 3 is okay, check U8D, U15B, U5C, U2, U3, U4, and associated circuits.
	J2-38 (rate 1)	33 to 45 Hz	
	J2-37 (rate 2)	67 to 83 Hz	
	J2-47 (rate 4)	135 to 165 Hz	
	J2-49 (rate 8)	270 to 330 Hz	
	J2-45 (rate 16)	540 to 660 Hz	

Table 1. Count/Store Assembly, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. Up/$\overline{\text{down}}$ direction	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to any. BANDWIDTH to any. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Connect clock A, set at 25 Hz, to J4-3 (clock A, count) and clock B, set at 25 Hz, to J4-5 (clock B, up/down).		
	c. Vary the phase of clock A and clock B, and measure the dc voltage at J2-48 (up/down).	Clock A leads clock B by 90; J2-48 = NMT +0.5 V dc. Clock A lags clock B by 90; J2-48 = NLT +3.0 V dc.	Check U6A, U4, and associated circuits.
6. $\overline{\text{Dial lock}}$	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to any. BANDWIDTH to any. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Connect clock A, set at 25 Hz, to J4-3 (clock A, count) and clock B, set at 25 Hz to J4-5 (clock B, up/down).		
	c. Vary the phase of clock A and clock B, and measure the voltages at each rate output.		Check U11C and associated circuits.
	J2-38 (rate 1) J2-37 (rate 2) J2-47 (rate 4) J2-49 (rate 8) J2-45 (rate 16)	NMT 0.5 V dc	
	d. Set DIAL switch to FINE.		
	e. Repeat step 4.c.	Same as step 4.c.	Same as step 4.c.

Table 1. Count/Store Assembly, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
7. Local/remote	a. Front-panel controls set as follows: PWR to on. CONT to REM. MODE to any. BANDWIDTH to any. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Measure input at U3-1, -2 and U4-1, -2.	NLT +3.0 V dc.	Check U8A and associated circuit.
	c. Set CONT switch to LCL.		
	d. Measure input at U3-1, -2, and U4-1, -2.	NMT 0.5 V dc.	Same as step 7.b.
8. Continuous/ single clock	a. Front-panel controls set as follows: PWR to on. CONT to LCL MODE to any. BANDWIDTH to any. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Connect clock A, set at 25 Hz, to J4-3 (clock A, count) and clock B, set at 25 Hz, to J4-5 (clock B, up/down).		
	c. Measure the pulses at TP3.	10- to 30-μs pulse width, 100 to 120 μs between pulses.	If test 3 and 4 are okay, check U5B and associated circuit.
	d. Remove clock A and block B inputs from J4-3 and J4-5.		
	e. Measure the pulses at TP3 while applying a single clock A pulse at J4-3.	Should be two pulses generated as indicated in step 8.c.	Same as step 8.c.
	f. Measure the rate 1 output at J2-38 while applying a single clock A pulse at J4-3.	Should go momentarily to logic 1 (NLT +3 V dc) then return to logic 0.	Same as test 4.
9. Power off check (Cont)	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to any. BANDWIDTH to any. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		

Table 1. Count/Store Assembly, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
9. (Cont)	b. Measure dc voltage at J2-34 (clock inhibit) while momentarily setting PWR switch off and returning it on.	Goes to logic 0 (NMT 0.5 V dc) for 2 to 20 seconds after power is restored, then switches to logic 1 (NLT +3.0 V dc).	Check U12 and associated circuit.
10. Test complete	a. Set PWR switch off. b. Disconnect external power from rear panel. c. Remove test equipment from J4 and reconnect P13 to count/store assembly J4. d. Reinstall top cover of unit.		

Table 2. Optical Tuning Switch Assembly, Testing Procedures.

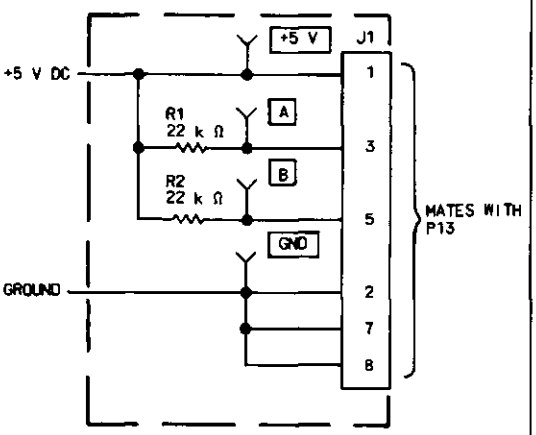
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top and bottom cover of unit containing the optical tuning switch assembly to be tested. b. Disconnect P13 that connects count/store assembly J4 to optical tuning switch assembly. **Note** Upon completion of optical tuning switch assembly testing reconnect P13 and J4. c. Connect the test jig shown below to P13. **Note** It is not necessary to apply power to the unit.  		If any abnormal indications occur in the optical tuning switch assembly, return it to the factory for repair.
2. Static state	With power applied check static state outputs of A and B.	Logic 1 or logic 0 are acceptable. Logic 1 = NLT +3 V dc. Logic 0 = NMT 0.5 V dc.	
3. TUNING knob rotation (Cont)	a. Connect a dual-trace oscilloscope to test jig: A to input A and trigger t, and B to input B. b. Note waveforms when rotating TUNING knob in a clockwise direction.	Waveform A lags Waveform B by 90 ±20 degrees.	

Table 2. Optical Tuning Switch Assembly, Testing Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	c. Note waveforms when rotating TUNING knob in a counterclockwise direction.	Waveform A leads waveform B by 90 ±20 degrees.	
4. Test complete	a. Remove test equipment from P13 and reconnect P13 to count/store assembly J4. b. Reinstall top cover of unit.		

4. REPAIR

Repair of the count/store assembly is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

Field repair of the optical tuning switch assembly is not recommended. If it fails, return it to the factory for service.

5. PARTS LIST/DIAGRAMS

This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figure 4). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

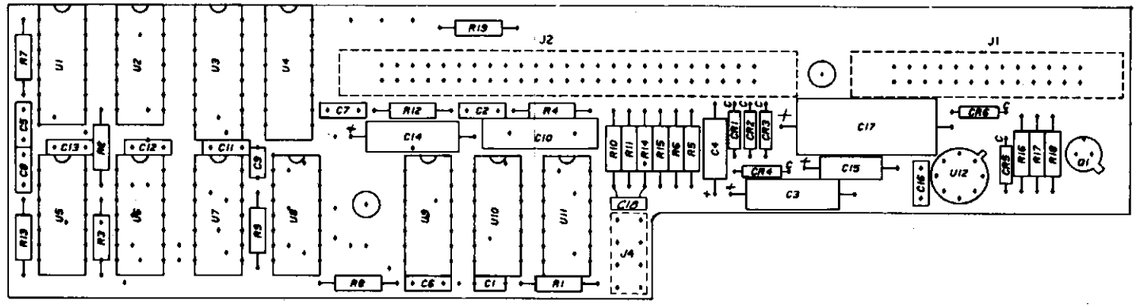
Use the reference designator indicated on the schematic and parts location diagram to locate part in the parts list tabulation. The Collins part number and description are listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points to the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

A schematic diagram only (no parts list) is given for the optical tuning switch assembly (figure 5).

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Count/store assembly	638-6063-001	REV A
Optical tuning switch assembly	610-2150-001	REV —



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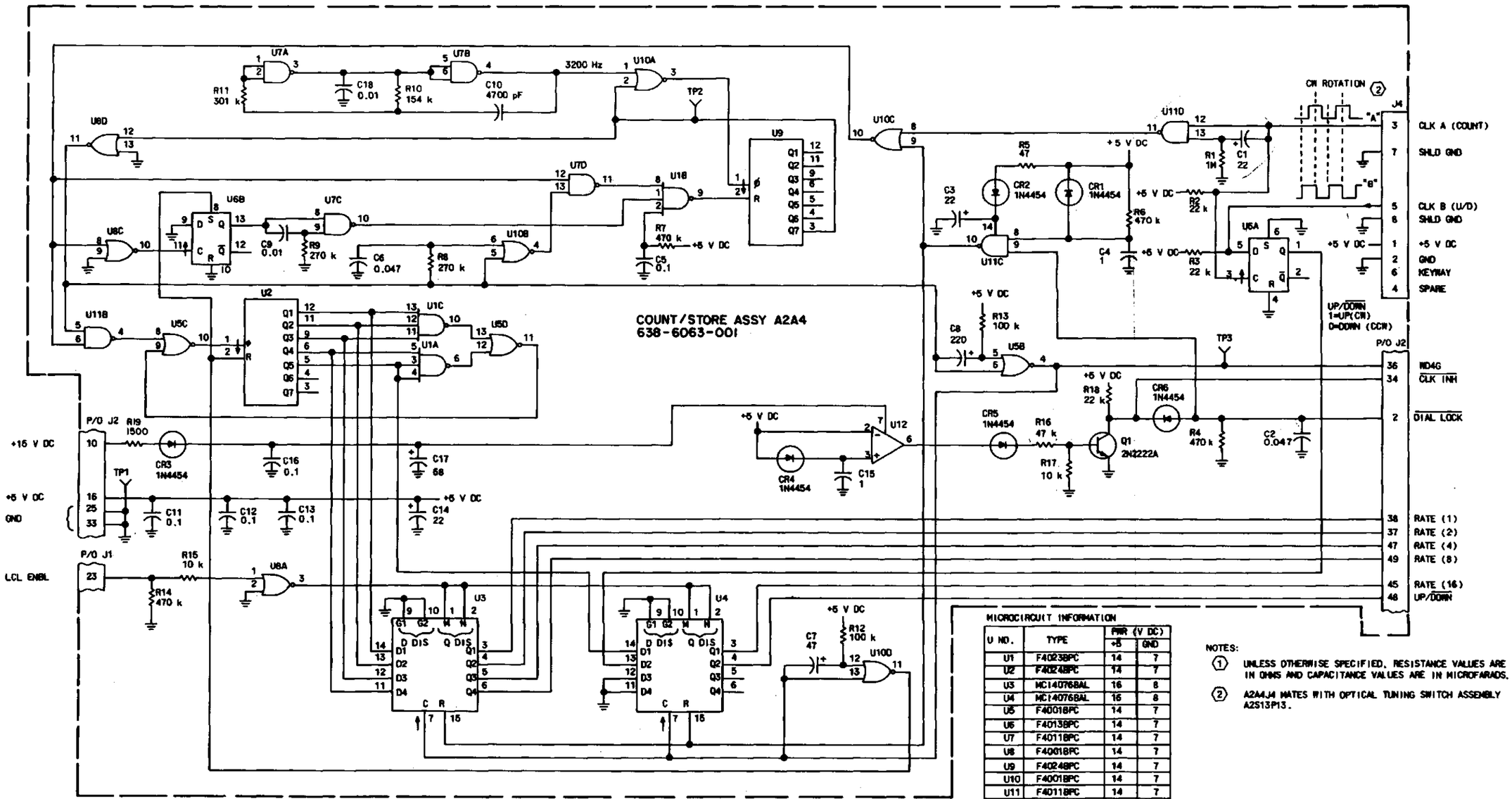
Count/Store Assembly, Schematic Diagram
Figure 4 (Sheet 1 of 3)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
	COUNT/STORE ASSEMBLY	638-6063-001	
CR1-CR6	SEMICOND DEVICE 1N4454	353-3644-010	
C1	CAPACITOR,FXD CER DIEL, 22PF, 10%, 200V	913-5019-050	
C2	CAPACITOR,FXD CER DIEL, 0.047UF, 10%, 100V	913-5019-400	
C3	CAPACITOR,FXD ELCTLT, 22UF, 10%, 15V	184-9086-310	
C4	CAPACITOR,FXD ELCTLT, 1UF, 10%, 50V	184-9087-430	
C5	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C6	CAPACITOR,FXD CER DIEL, 0.047UF, 10%, 100V	913-5019-400	
C7	CAPACITOR,FXD CER DIEL, 47PF, 10%, 200V	913-4002-080	
C8	CAPACITOR,FXD CER DIEL, 220PF, 10%, 200V	913-4010-000	
C9	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C10	CAPACITOR,FXD MICA DIEL, 4700PF, 5%, 300V	912-3366-000	
C11-C13	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C14	CAPACITOR,FXD ELCTLT, 22UF, 10%, 15V	184-9086-310	
C15	CAPACITOR,FXD ELCTLT, 1UF, 10%, 50V	184-9087-430	
C16	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C17	CAPACITOR,FXD ELCTLT, 68UF, 10%, 20V	184-9086-580	
C18	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
Q1	TRANSISTOR 2N2222A	352-0661-020	
R1	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R2,R3	RESISTOR,FXD CMPSN, 22K, 10%, 1/4W	745-0797-000	
R4	RESISTOR,FXD CMPSN, 0.47MEGO, 10%, 1/4W	745-0845-000	
R5	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/4W	745-0701-000	
R6,R7	RESISTOR,FXD CMPSN, 0.47MEGO, 10%, 1/4W	745-0845-000	
R8,R9	RESISTOR,FXD CMPSN, 0.27MEGO, 10%, 1/4W	745-0836-000	
R10	RESISTOR,FXD FILM, 154K, 1%, 1/8W	705-1101-000	
R11	RESISTOR,FXD FILM, 301K, 1%, 1/8W	705-1115-000	
R12,R13	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000	
R14	RESISTOR,FXD CMPSN, 0.47MEGO, 10%, 1/4W	745-0845-000	
R15	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000	
R16	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W	745-0809-000	
R17	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000	
R18	RESISTOR,FXD CMPSN, 22K, 10%, 1/4W	745-0797-000	
R19	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/4W	745-0755-000	
U1	INTEGRATED CIRCUIT F4023BPC	351-8159-360	
U2	INTEGRATED CIRCUIT F4024BPC	351-8159-100	
U3,U4	INTEGRATED CIRCUIT MC14076BAL	351-8386-010	
U5	INTEGRATED CIRCUIT F4001BPC	351-8159-320	
U6	INTEGRATED CIRCUIT F40138PC	351-8159-110	
U7	INTEGRATED CIRCUIT F4011BPC	351-8159-340	
U8	INTEGRATED CIRCUIT F4001BPC	351-8159-320	
U9	INTEGRATED CIRCUIT F4024BPC	351-8159-100	
U10	INTEGRATED CIRCUIT F4001BPC	351-8159-320	
U11	INTEGRATED CIRCUIT F40110PC	351-8159-340	
U12	INTEGRATED CIRCUIT UA741HC	351-1029-010	

Count/Store Assembly, Schematic Diagram
Figure 4 (Sheet 2)



MICROCIRCUIT INFORMATION

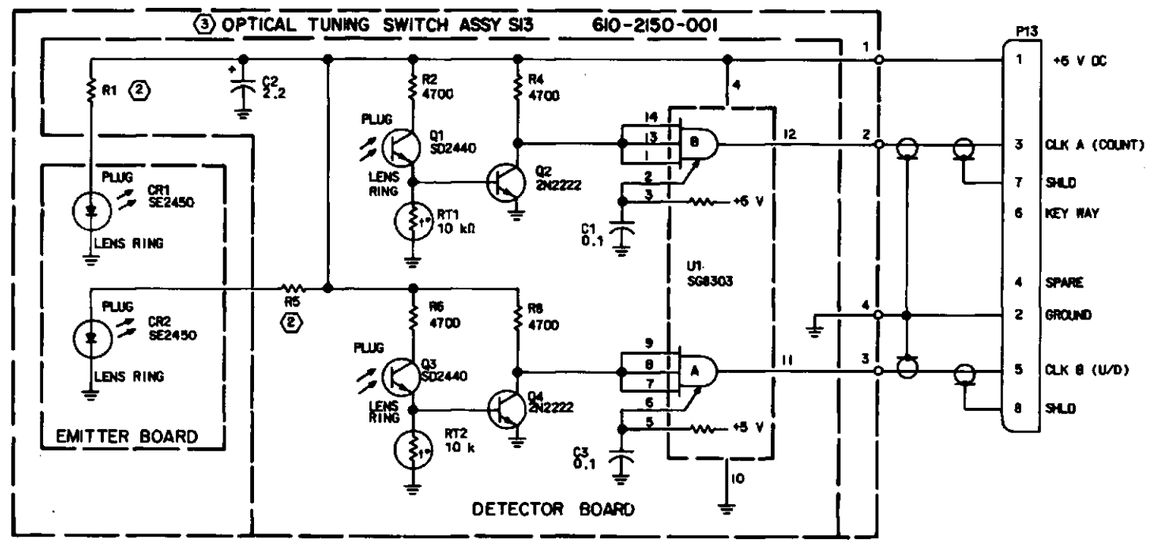
U NO.	TYPE	PWR (V DC) +5	PWR (V DC) GND
U1	F40238PC	14	7
U2	F40248PC	14	7
U3	MC14076BAL	16	8
U4	MC14076BAL	16	8
U5	F40018PC	14	7
U6	F40138PC	14	7
U7	F40118PC	14	7
U8	F40018PC	14	7
U9	F40248PC	14	7
U10	F40018PC	14	7
U11	F40118PC	14	7
U12	UA741HC		4

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS.
2. A2A4J4 MATES WITH OPTICAL TUNING SWITCH ASSEMBLY A2S13P13.

TPA-0624-016 SH 4

Count/Store Assembly, Schematic Diagram
Figure 4 (Sheet 3)



NOTES:

① UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS.

② VALUE SELECTED IN FINAL TEST.

③ FIELD REPAIR OF OPTICAL TUNING SWITCH ASSEMBLY IS NOT RECOMMENDED.

TPA-0624-016 SH 3

Optical Tuning Switch Assembly, Schematic Diagram
Figure 5

Frequency Display (637-1781-( ))

Rockwell International

instructions

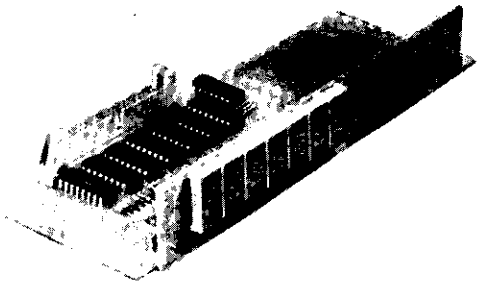
Collins Telecommunications Products Division

Printed in USA

523-0767975-003211
3rd Edition, 1 January 1979

1. DESCRIPTION

The Frequency Display 635-1781-( ) consists of two subassemblies hard-wired together. One subassembly, the frequency display driver board, contains the logic and decoder/driver circuits. The other, the frequency display board, contains the 7-segment displays. The subassemblies are 2-layer circuit boards with a cable connector on the section containing the decoder/drivers. Figure 1 is a picture of the assembled subassemblies.



TP5-2370-017

Frequency Display
Figure 1

2. PRINCIPLES OF OPERATION

2.1 General

The frequency display configuration differences are as follows:

a. 637-1781-001, 100 Hz operating frequency display and no BFO frequency display.
b. 637-1781-002, 10 Hz operating frequency display and no BFO frequency display.
c. 637-1781-003, 10 Hz operating frequency display and BFO frequency display of ±0-9990 Hz (operating frequency can be expanded to 1 Hz by adding display device U27).
d. 637-1781-004, 1 Hz operating frequency display and BFO frequency display of ±0-9990 Hz.
e. 637-1781-005, 100 Hz operating frequency display and no BFO frequency display (can be expanded to 10/1 Hz operating frequency display and/or BFO frequency display by adding display devices U26/U27 and/or U15 through U19).

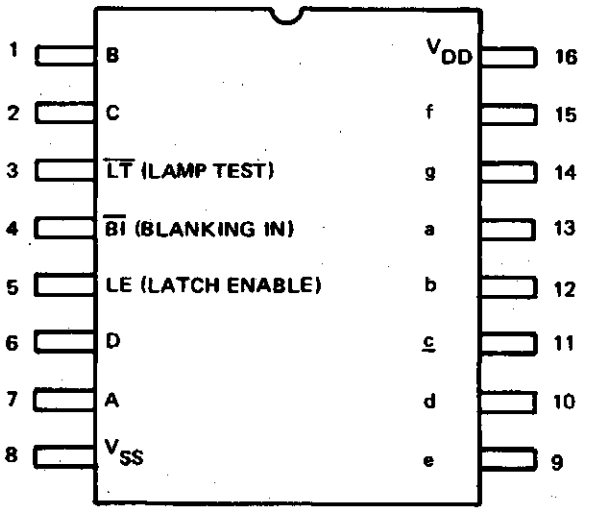
2.2 Theory of Operation (Refer to figure 4.)

For each frequency digit, a 4-bit binary input is applied to the decoder/driver. This input data is decoded into seven binary outputs. These logic-level outputs are applied directly to the 7-segment display associated with the decoder/driver. Each output causes a certain LED segment to light to form a part of the numeral equivalent to the 4-bit binary input to the board.

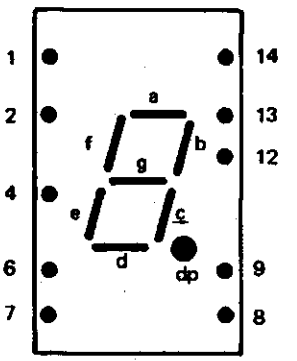
Figure 2 shows the decoder/driver input-output truth table and the 7-segment display connections.

The units and tens megahertz displays are blanked if the frequency is not within the 1- to 30-MHz range (for which these digits would be needed). This suppresses the leading zeros in lower frequency displays. The blanking (suppression) input ($\overline{BI}$ at logic 0 level) is generated by OR gates U6B-U6D. When all inputs

NOTICE: This section replaces second edition dated 1 June 1978.



BCD–TO–7–SEGMENT DECODER/DRIVER



TRUTH TABLE

INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
0	0	1	X	X	X	X	0	0	0	0	0	0	0	BLANK
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	BLANK
0	1	1	1	0	1	1	0	0	0	0	0	0	0	BLANK
0	1	1	1	1	0	0	0	0	0	0	0	0	0	BLANK
0	1	1	1	1	0	1	0	0	0	0	0	0	0	BLANK
0	1	1	1	1	1	0	0	0	0	0	0	0	0	BLANK
0	1	1	1	1	1	1	0	0	0	0	0	0	0	BLANK

X = DON'T CARE

7–SEGMENT LED DISPLAY

PIN NO.	PIN CONNECTIONS
1	ANODE F
2	ANODE G
3	NO PIN
4	COMMON CATHODE
5	NO PIN
6	ANODE E
7	ANODE D
8	ANODE C
9	ANODE DP
10	NO PIN
11	NO PIN
12	COMMON CATHODE
13	ANODE B
14	ANODE A

TP5-2300-011

Decoder/Driver and Display Elements Operation
Figure 2

to the decoder/driver are at logic 0, the OR gate outputs cause the $\overline{BI}$ input to be logic 0, causing a blanking command to be applied to the display. For this input to the indicators, no LED segments light and the display remains off, or blank.

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test and troubleshoot the frequency display board are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 1 check the total performance of the frequency display. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

4. REPAIR

Repair of the frequency display is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

5. PARTS LIST/DIAGRAMS

This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figure 3). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on the schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

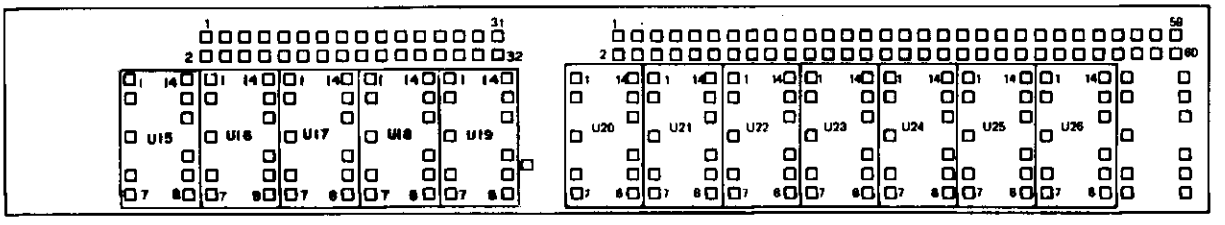
Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points to the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

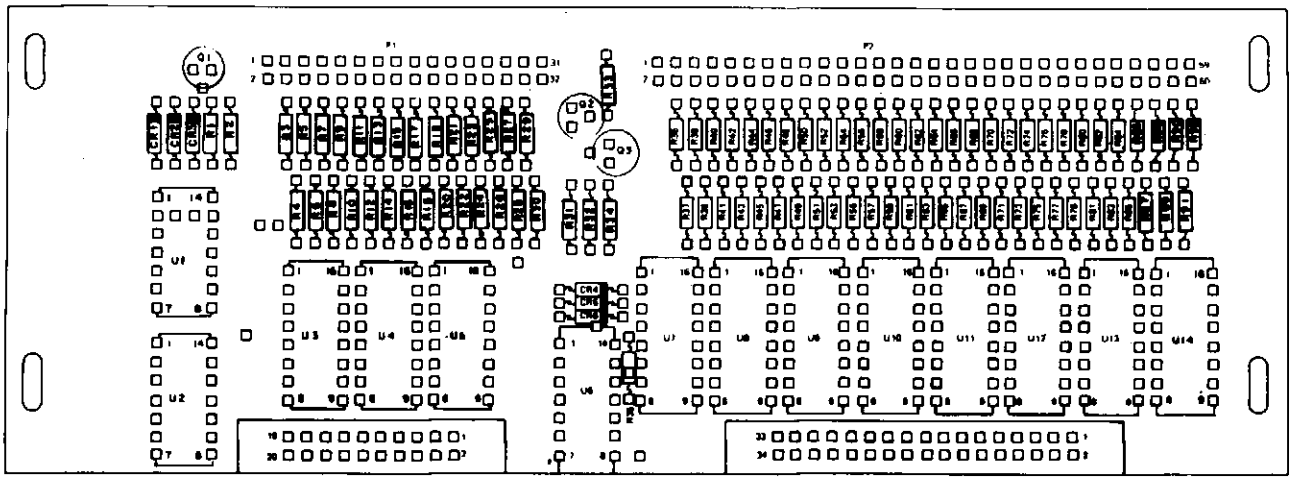
CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Frequency Display	637-1781-001	REV B
Frequency Display	637-1781-002	REV B
Frequency Display	637-1781-003	REV E
Frequency Display	637-1781-004	REV D
Frequency Display	637-1781-005	REV E
Frequency Display Driver Board	635-0896-001	REV H
Frequency Display Driver Board	635-0896-002	REV H
Frequency Display Driver Board	635-0896-004	REV G
Frequency Display Board	635-0897-001	REV C
Frequency Display Board	635-0897-002	REV C
Frequency Display Board	635-0897-003	REV D
Frequency Display Board	635-0897-004	REV E

Table 1. Frequency Display Testing and Troubleshooting Procedures.

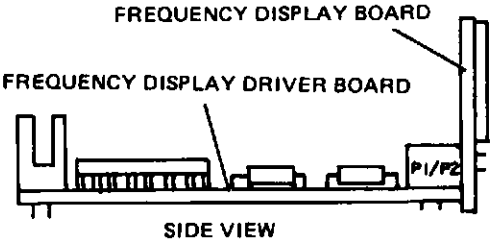
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Test setup	Set all FREQUENCY switches to 0. Turn on PWR switch and set CONT switch to TEST.		
2. Zero suppression and decimal point display	Observe FREQUENCY readout display.	Units' and tens' zeros of MHz range suppressed (blanked). Zeros for kHz and tenths displayed. Decimal point after fifth digit from left displayed.	If MHz-range zeros displayed, troubleshoot U6B, U6C, U6D, and U7. If decimal point not displayed, troubleshoot U24.
3. Digit selection and display	Rotate each FREQUENCY switch through all its positions. (Leftmost switch has positions 0, 1, and 2 only.) Observe readout display to see that corresponding selected digit is displayed. **Note** Wait approx 1 second after switching for time delay to elapse and circuit to strobe in new digit. If switch is changed too slowly, strobe signal may be generated while old number is still applied to circuit. In this case, the new number will not be displayed even though switch is set to new position. Switch away from and back to new position if this occurs.	Readout digit displayed corresponds to that selected on thumbwheel switch.	Refer to schematic diagram and troubleshoot decoder/driver and readout unit corresponding to selected digit showing malfunction. For normal display, decoder/driver inputs and outputs at logic 1 are listed below for each digit. DIGIT — INPUTS — OUTPUTS 0 — (all 0's) — a+b+c+d+e+f 1 — A — b+c 2 — B — a+b+c+e+g 3 — A+B — a+b+c+d+g 4 — C — b+c+f+g 5 — A+C — a+c+d+f+g 6 — B+C — c+d+e+f+g 7 — A+B+C — a+b+c 8 — D — a+b+c+d+e+f+g 9 — A+D — a+b+c+f+g



FREQUENCY DISPLAY BOARD 635-0897- ( )



FREQUENCY DISPLAY DRIVER BOARD 635-0896- ( )



SIDE VIEW
(ASSEMBLED)
637-1781- ( )

TP5 -1039 -019

Frequency Display, Schematic Diagram
Figure 3 (Sheet 1 of 4)

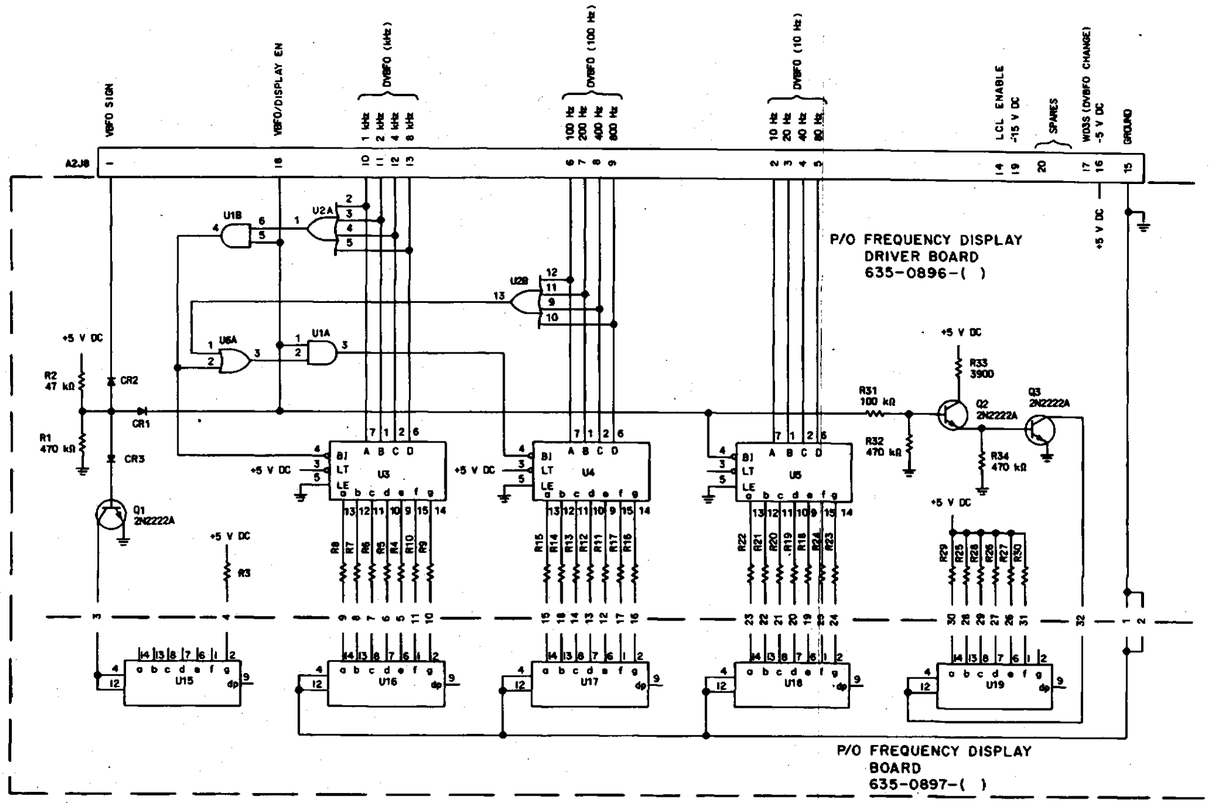
PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	FREQUENCY DISPLAY 637-1781-001		A
	FREQUENCY DISPLAY 637-1781-002		B
	FREQUENCY DISPLAY 637-1781-003		C
	FREQUENCY DISPLAY 637-1781-004		D
	FREQUENCY DISPLAY 637-1781-005		E
	FREQUENCY DISPLAY DRIVER BD	635-0896-001	A
	FREQUENCY DISPLAY DRIVER BD	635-0896-002	B
	FREQUENCY DISPLAY DRIVER BD	635-0896-004	C,D,E
	FREQUENCY DISPLAY BD	635-0897-001	A,E
	FREQUENCY DISPLAY BD	635-0897-002	B
	FREQUENCY DISPLAY BD	635-0897-003	C
	FREQUENCY DISPLAY BD	635-0897-004	D
	FREQUENCY DISPLAY DRIVER BD	635-0896-001	
CR1-CR3	NOT USED		
CR4-CR6	SEMICOND DEVICE, 1N4454	353-3644-010	
R1-R34	NOT USED		
R35	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/8W	745-2449-000	
R36-R76	RESISTOR, FXD, CMPSN, 180Ω, 10%, 1/8W	745-2314-000	
U1-U5	NOT USED		
U6	INTEGRATED CKT, MC14071BCP	351-8287-010	
U7-U12	INTEGRATED CKT, MC14511BCP	351-8304-010	
	FREQUENCY DISPLAY DRIVER BD	635-0896-002	
CR1-CR3	NOT USED		
CR4-CR6	SEMICOND DEVICE, 1N4454	353-3644-010	
R1-R34	NOT USED		
R35	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/8W	745-2449-000	
R36-R85	RESISTOR, FXD, CMPSN, 180Ω, 10%, 1/8W	745-2314-000	
U6	INTEGRATED CKT, MC14071BCP	351-8287-010	
U7-U13	INTEGRATED CKT, MC14511BCP	351-8304-010	
	FREQUENCY DISPLAY DRIVER BD	635-0896-004	
CR1-CR6	SEMICOND DEVICE, 1N4454	353-3644-010	
Q1-Q3	TRANSISTOR, 2N2222A	352-0661-020	
R1	RESISTOR, FXD, CMPSN, 470kΩ, 10%, 1/8W	745-2437-000	
R2	RESISTOR, FXD, CMPSN, 47kΩ, 10%, 1/8W	745-2401-000	
R3-R30	RESISTOR, FXD, CMPSN, 180Ω, 10%, 1/8W	745-2314-000	
R31	RESISTOR, FXD, CMPSN, 100kΩ, 10%, 1/8W	745-2413-000	
R32	RESISTOR, FXD, CMPSN, 470kΩ, 10%, 1/8W	745-2437-000	
R33	RESISTOR, FXD, CMPSN, 3.9kΩ, 10%, 1/8W	745-2362-000	
R34	RESISTOR, FXD, CMPSN, 470kΩ, 10%, 1/8W	745-2437-000	
R35	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/8W	745-2449-000	
R36-R92	RESISTOR, FXD, CMPSN, 180Ω, 10%, 1/8W	745-2314-000	
U1	INTEGRATED CKT, MC14081BCP	351-8287-030	
U2	INTEGRATED CKT, MC14072BCP	351-8287-040	
U3-U5	INTEGRATED CKT, MC14511 BCP	351-8304-010	
U6	INTEGRATED CKT, MC14071BCP	351-8287-010	
U7-U14	INTEGRATED CKT, MC14511BCP	351-8304-010	
	FREQUENCY DISPLAY BD 635-0897-001		
U1-U19	NOT USED		
U20-U25	SEMICOND DEVICE, MAN3640A	262-1461-010	
	FREQUENCY DISPLAY BD 635-0897-002		
U1-U19	NOT USED		
U20-U26	SEMICOND DEVICE, MAN3640A	262-1461-010	
	FREQUENCY DISPLAY BD 635-0897-003		
U1-U14	NOT USED		
U15-U26	SEMICOND DEVICE, MAN3640A	262-1461-010	
	FREQUENCY DISPLAY BD 635-0897-004		
U1-U14	NOT USED		
U15-U27	SEMICOND DEVICE, MAN 3640A	262-1461-010	

Frequency Display, Schematic Diagram
Figure 3 (Sheet 2)

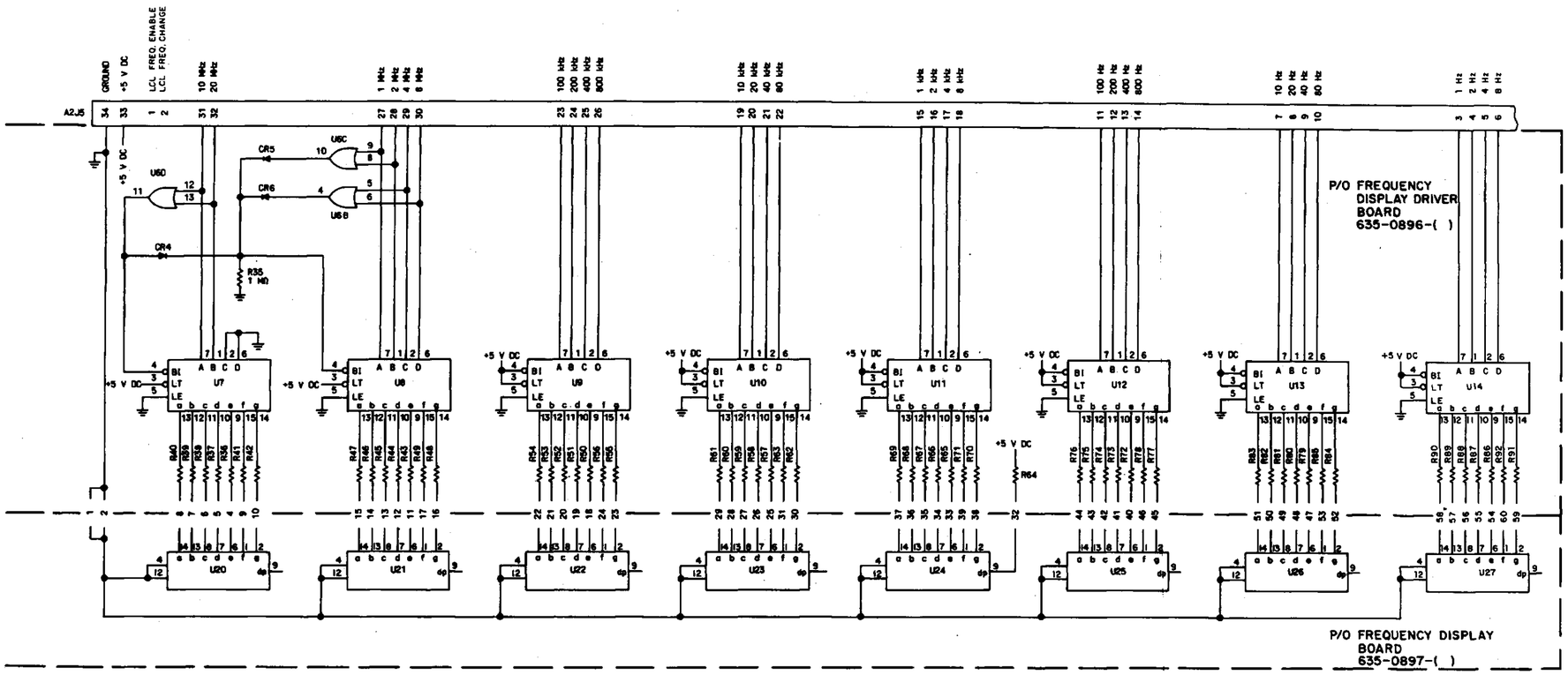
CIRCUITS USED PER FREQUENCY DISPLAY

		CIRCUIT	637-1781-()				
			-001	-002	-003	-004	-005
FREQUENCY DISPLAY DRIVER BOARD	VBFO DISPLAY ENABLE	VBFO DISPLAY ENABLE	U1			X	X	X
		1 kHz	U2			X	X	X
		100 Hz	U3			X	X	X
		10 Hz	U4			X	X	X
		DISPLAY BLANKING	U5			X	X	X
	OPER FREQ DISPLAY DRIVERS	10 MHz	U6	X	X	X	X	X
		1 MHz	U7	X	X	X	X	X
		100 kHz	U8	X	X	X	X	X
		10 kHz	U9	X	X	X	X	X
		1 kHz	U10	X	X	X	X	X
		100 Hz	U11	X	X	X	X	X
		10 Hz	U12	X	X	X	X	X
		1 Hz	U13		X	X	X	X
FREQUENCY DISPLAY BOARD	VBFO DISPLAY	SIGN	U14			X	X	X
		1 kHz	U15			X	X	
		100 Hz	U16			X	X	
		10 Hz	U17			X	X	
		1 Hz	U18			X	X	
	OPER FREQ DISPLAY	10 MHz	U19			X	X	
		1 MHz	U20	X	X	X	X	X
		100 kHz	U21	X	X	X	X	X
		10 kHz	U22	X	X	X	X	X
		1 kHz	U23	X	X	X	X	X
		100 Hz	U24	X	X	X	X	X
		10 Hz	U25	X	X	X	X	X
		1 Hz	U26		X	X	X	
			U27				X	



TPA-0277-025

Frequency Display, Schematic Diagram
Figure 3 (Sheet 3)



NOTES:

1. RESISTORS R3 THRU R30 AND R36 THRU R92 ARE 180 OHM.
2. DIODES ARE TYPE 1N4454.
3. POWER AND GROUND CONNECTIONS

U NO.	TYPE	POWER (V DC)	
		+5	GND
U1	MC14081BCP	14	7
U2	MC14072BCP	14	7
U3, U4, U5, AND U7 THRU U14	MC14511BCP	16	8
U6	MC14071BCP	14	7
U15 THRU U27	MAN3640A		

TPA-0277-025

Frequency Display, Schematic Diagram
Figure 3 (Sheet 4)

VBFO
(638-6067-001)

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

523-0769219-001211
1 January 1979

Instructions VBFO (638-6067-001)

1. DESCRIPTION

VBFO 638-6067-001, shown in figure 1, is a 2-layer planar card with a 56-pin edge-on connector (2 layers, 28 pins each) and two subminiax rf connectors.

The VBFO consists of a synthesized bfo, a bcd up/-down counter, an end-stop circuit, and a polarity change control circuit.

2. PRINCIPLES OF OPERATION

2.1 General

The vbfo receives the following inputs:

a. 450-kHz reference
b. Preset vbfo (parallel bcd) input or vbfo tune input
c. Vbfo/450-kHz switching inputs
d. Necessary associated control signals to activate and control the vbfo output frequency.

The vbfo produces the following outputs:

a. A bfo offset if frequency output (440.01 to 459.99 kHz in 10-Hz steps)
b. A parallel bcd output for displays

The vbfo circuits are enabled by a vbfo enable signal (logic 1) at P1-46. The vbfo/450-kHz control enables the vco, output switching, and the phase/frequency discriminator. Refer to figure 2.

2.2 Synthesized BFO

A 450-kHz reference input signal at J2 is applied through buffer circuit Q16 and is divided by 1500 (by fixed dividers U38, U39, and U33) to produce 300-Hz reference frequency signals that are applied to sampling gates U9A, U9B, U9C, and U9D, in the voltage-controlled oscillator (vco), through sampling logic circuits U34, Q4, and Q5.

(To Be Supplied)

VBFO
Figure 1

Decade counters U19, U24, U27, U31, and U32 form a programmable frequency divider with variable division ratios ranging from 44 001 to 45 999, with 45 000 the division ratio for 0 vbfo offset from the selected operating frequency. The division ratios for the various vbfo settings are determined by the bcd frequency information from the preset vbfo (parallel bcd) input or parallel bcd output for the bcd up/down counter. The +/- signal is determined by the +/- input signal and by up/down and reset logic circuit U13, U14, and the vbfo polarity change circuit. The output of the programmable divider circuit is applied through the phase/frequency discriminator and then to the sampling gates in the vco assembly.

523-0769219-001211

The vco assembly generates an output frequency that ranges from 13.2003 to 13.7997 MHz with 13.5000 MHz as the center frequency (0 vbfo offset). The output from the vco assembly is used as the clock signal for the programmable divider circuit and is divided by 30 (by fixed divider circuits U3 and U1) to become the vbfo output signal that ranges from 440.01 to 459.99 kHz.

The division ratio of the programmable dividers is accomplished by loading 45 000 into the counters, adding the vbfo offset frequency, and then allowing the counters to count down to 00 000. Assume that the BFO is set to the maximum deviation, 9.990 kHz, above the operating frequency. The +/- input goes to + (logic 1), which causes the up/down and reset logic circuit to set the programmable divider circuit to the required 45 000 division ratio and to a countdown state. The 999 input from the bcd frequency input is loaded, making a total division ratio of 45 999 (the countdown starting point). The counter circuit then divides by counting down to 00 000. The clock input to the divider circuit, at this point, will be different from the required 13.7997 MHz (depending upon the previous vbfo offset frequency), which causes the output of the counter circuit applied to the sampling gates to be less than the 300-Hz nominal frequency. The sampling gates in the vco assembly function basically as a phase comparator. The 300-Hz control inputs, produced from the 450-kHz reference input, enable the gates at the 300-Hz control (logic 0) pulse rate. If the input signal from the programmable divider is out of phase, the out-of-phase portion of the signal is passed through the gates during the enable period. The more out of phase the input signal, the greater the amplitude of the output signal from the gates. The output of the gates is filtered and amplified by capacitor C29 and FET Q8 to produce a dc error voltage. The dc error voltage is applied across voltage variable capacitance diode VR4. As the voltage across VR4 increases, its capacitance decreases, thus increasing the frequency of the voltage-controlled oscillator circuit (U4). Conversely, as the dc error voltage across VR4 decreases, the capacitance increases and decreases the oscillator circuit frequency. As the vco output frequency increases, (toward 13.7997 MHz), the output frequency of the programmable divider circuit increases (toward 300 Hz) which, in turn, decreases the error voltage applied to VR4. When the oscillator output frequency reaches 13.7997 MHz, the output from the programmable divider circuit is 300 Hz (13.7997 MHz ÷ 45.999). The vco circuit locks at this frequency and remains until the bfo frequency information is changed. The 13.7997-MHz oscillator frequency is divided by 30 to produce the 459.99-kHz if output signal that is applied to if amplifier for use in the SSB, ISB, and CW modes of operation.

If the BFO is set to the maximum deviation below the operating frequency (9.990 kHz), the synthesizer functions are the same except the +/- input goes to - (logic 0) and the programmable divider circuit is set to a count-up state and begins counting at 55 000 plus the BFO offset (deviation) of 9.990 kHz or, a 55 999 start counting point. The count progresses toward a maximum count of 100 000. This produces the division ratio of 44 001 (100 000 - 55 999). The error voltage applied to VR4 decreases and causes the output frequency to decrease. When the output of the programmable divider reaches 300 Hz, the oscillator output frequency will lock at 13.2003 and, when divided by 30, will produce the 440.01-kHz vbfo output signal.

2.3 Input Control Signals

2.3.1 Parallel BCD Input (Remote control operation only.)

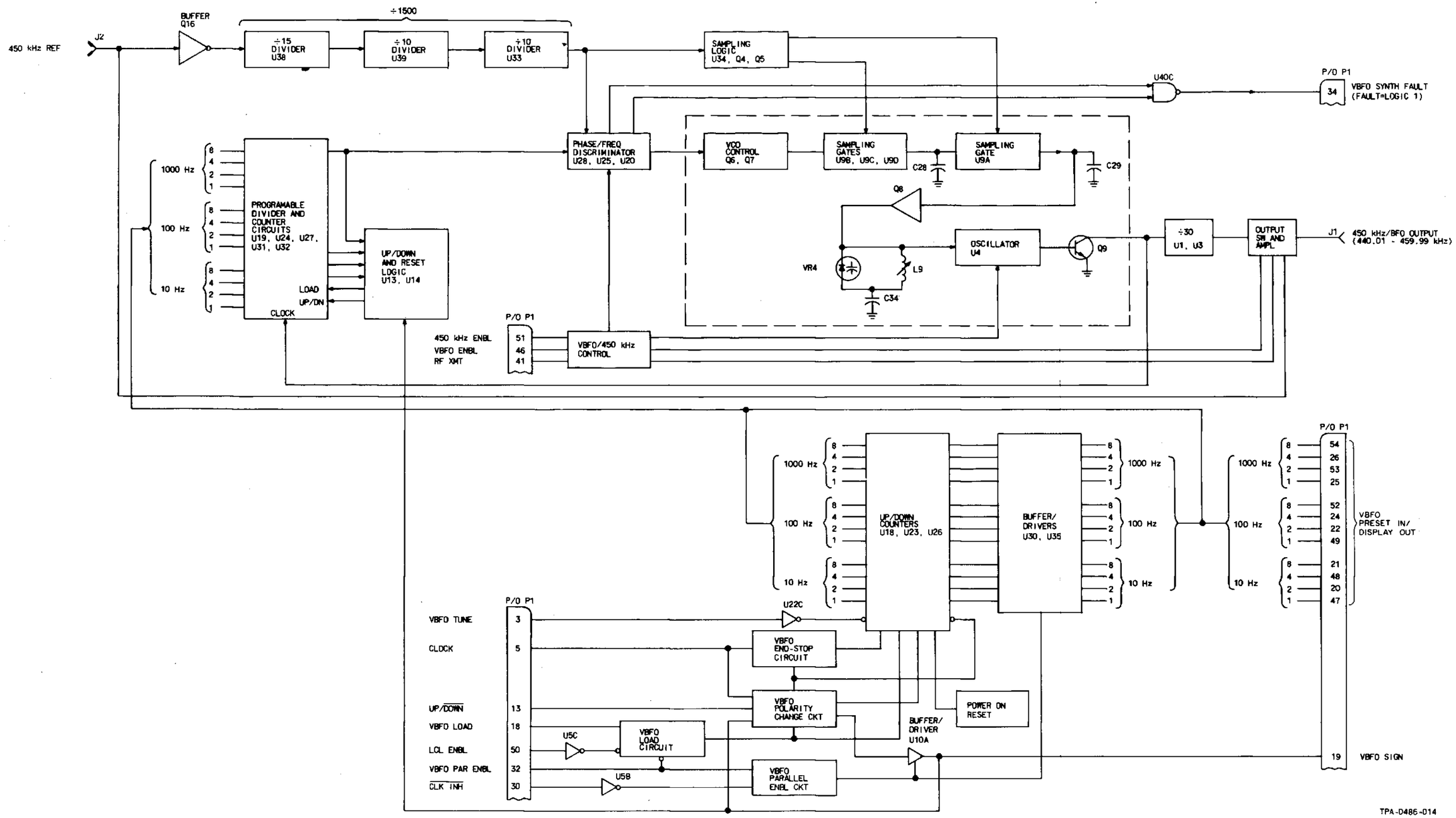
When applying the parallel bcd input signals at P1 to activate the vbfo, the vbfo parallel enable signal (logic 1) is applied at P1-32 and $\overline{\text{local enable}}$ (logic 0) is applied at P1-50. This allows the dual one-shot U6A and U6B to generate a preset enable input to the up/down counters each time a logic 1 vbfo pulse is applied to P1-18. The logic 1 preset enable input allows the up/down counters to be preset to the applied parallel input. When the preset enable is removed, the applied parallel input is stored in the up/down counters until a clock signal (C), reset signal (R), or another preset enable signal (PE) is applied.

2.3.2 VBFO Tune Input

When applying a vbfo tune input (logic 1) at P1-3 to activate the vbfo, the following signals are also applied:

a. Vbfo parallel enable (logic 0) at P1-32.
b. $\overline{\text{Clock inhibit}}$ (logic 0) at P1-30.
c. Vbfo load (logic 0) at P1-18
d. Up (logic 1) or down (logic 0) at P1-13
e. Clock at P1-5

With the above signals applied, the up/down counters count with the direction of count determined by the input at P1-13. A logic 1 input at P1-3 applies a logic 0 carry in (CI) input to counter U18, enabling the 10-Hz counter. As the clock pulses are received the counter counts.



VBFO, Block Diagram
Figure 2

When the 10-Hz count reaches 9 (on an up-count) a logic 0 carryout signal is supplied as a carry-in to the 100-Hz counter U23. On the next clock the 10-Hz counter is reset, the 100-Hz counter is clocked, and the carryout signal goes to a logic 1 stopping the count of the 100-Hz counter after 1 count. This type of sequence continues through the 10-Hz, 100-Hz, and 1000-Hz counters until a frequency bcd of 9990 (up-count) is reached. When 9990 (up-count) is reached, a carryout (logic 0) is supplied through inverter U5D to NAND gate U15C. The inverted carryout signal is NANDed with the up (logic 1) signal and supplied to U11A. In the up-count, this U11A input is logic 0 and 0Red with the inverted output of 10-Hz bcd 1 count (90 Hz = 10-Hz bcd, 8 + 1) and supplies a logic 0 to clock gate U21D. U21D is inhibited and clocking is stopped. Refer to figure 3.

When the 10-Hz count reaches 0 (on a down-count) a logic 0 carryout signal is supplied as a carry-in to the 100-Hz counter U23. On the next clock the 10-Hz counter is reset, the 100-Hz counter is clocked and the carryout signal goes to a logic 1 stopping the count of the 100-Hz counter after 1 count. This type of sequence continues through the 10-Hz, 100-Hz, and 1000-Hz counters until a frequency bcd of 0000 (down-count) is reached. When 0000 (down-count) is reached, a carryout (logic 0) is supplied through inverter U5D to up/down control circuit at U17-4, -11. A bcd $\overline{1}$ is also supplied through inverter U22B to up/down control circuit at U17-5, -10. These two inputs (k1, k2) along with the inverted down input at U17-9 (k3) allows flip-flop U17 to change states on the next clock producing a $\overline{Q}$ output which is NANDed with the k3 input causing U12B output to go to logic 0 and output of U12D to go to logic 1, initiating an up-count on the next pulse. Refer to figure 4.

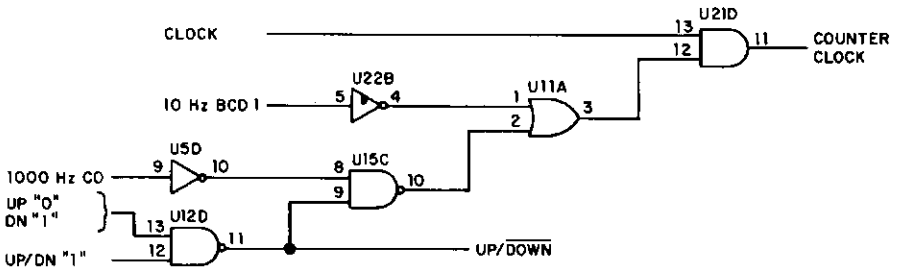
3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the vbfo are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in this section check total performance of the vbfo. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.



COUNT UP/DOWN	U5D		U12D			U15C			U22B		U11A			U21D			NOTES
	IN	OUT	IN		OUT	IN		OUT	IN	OUT	IN		OUT	IN		OUT	
	-9	-10	-12	-13	-11	-8	-9	-10	-5	-4	-1	-2	-3	-13	-12	-11	
9990 UP	0	1	1	0	1	1	1	0	1	0	0	0	0	CLK	0	0	INHIBITS CLK
9000 UP	1	0	1	0	1	0	1	1	1	0	0	1	1	CLK	1	CLK	CLOCK IS ENABLED
0000 UP	1	0	1	0	1	0	1	1	1	0	0	1	1	CLK	1	CLK	
0000 DN	0	1	1	1	0	0	0	1	1	0	0	0	1	CLK	1	CLK	
9000 DN	1	0	1	1	0	0	0	1	1	0	0	0	1	CLK	1	CLK	
9990 DN	1	0	1	1	0	0	0	1	0	1	1	0	1	CLK	1	CLK	

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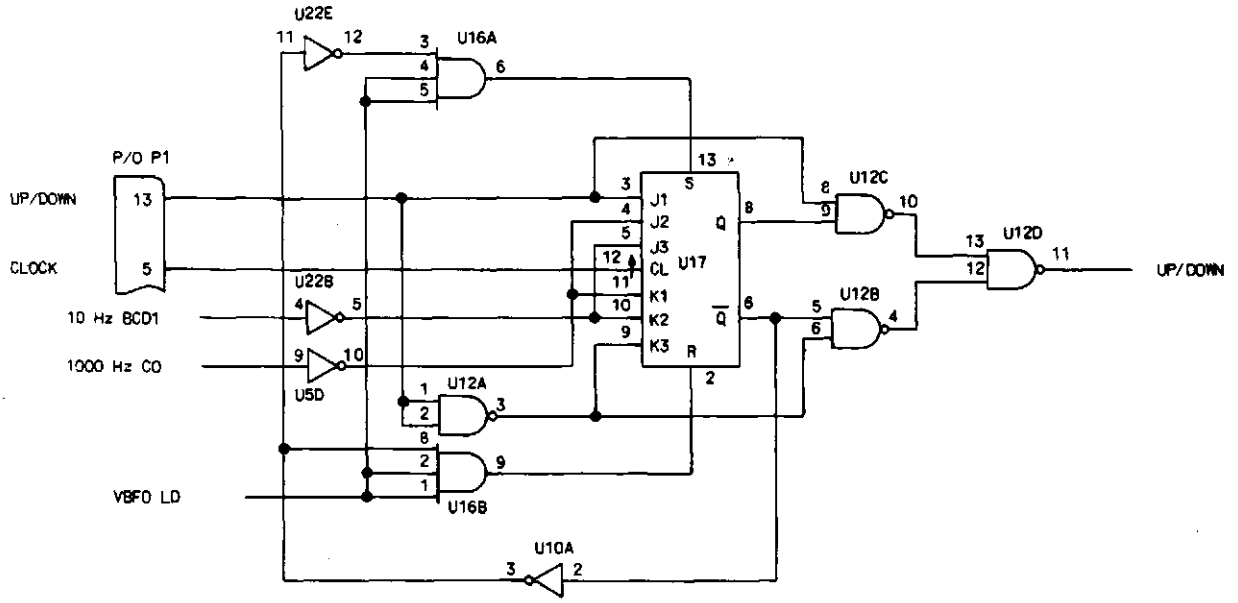
VBFO End-Stop Circuit
Figure 3



COUNT UP/DOWN	U22E		U22B		U5D		U12A		U16A			U16B			U17											U12B			U12C			U12D		
	IN	OUT	IN	OUT	IN	OUT	IN	OUT	IN		OUT	IN		OUT	S	R	J1	J2	J3	K1	K2	K3	Q	$\overline{Q}$	IN		OUT	IN		OUT	IN		OUT
	-11	-12	4	5	9	10	1	3	3	4	6	1	8	9	13	2	3	4	5	11	10	9	8	6	5	6	4	8	9	10	-12	-13	-11
9990 UP	1	0	1	0	1	0	1	0	0	1	1	1	1	0	1	0	1	0	0	1	0	0	0	1	1	0	1	1	0	1	1	0	1
9000 UP	1	0	0	1	0	1	1	0	0	1	1	1	1	0	1	0	1	1	1	0	1	0	0	1	1	0	1	1	0	1	1	0	1
0000 UP	1	0	0	1	0	1	1	0	0	1	1	1	1	0	1	0	1	1	1	0	1	0	0	1	1	0	1	1	0	1	1	0	1
0000 DN	0	1	0	1	1	0	0	1	1	1	0	1	0	1	0	1	0	0	1	1	1	1	1	0	0	1	1	0	1	1	1	1	0
9000 DN	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	1	1	0	0	1	1	0	1	1	1	1	0
9990 DN	0	1	1	0	0	1	0	1	1	1	0	1	0	1	0	1	0	1	0	0	0	1	1	0	0	1	1	0	1	1	1	1	0

NOTE:

WHEN 0000 DOWN COUNT IS REACHED, THE ABOVE LOGIC CIRCUITS ARE SET UP TO CHANGE DIRECTION (DOWN TO UP). WITH THE NEXT CLOCK INPUT (AFTER DOWN 0000) U17 CHANGES OUTPUT STATES. WHEN $\overline{Q}$ GOES TO LOGIC 1 U22E AND U16B SET U17 AND HOLD IT IN THE UP COUNT STATE.

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VBFO Polarity Change Circuit
Figure 4

Table 1. VBFO, Testing, and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of unit containing the vbfo that is to be tested.		
	b. If installed, remove parallel input, parallel output, and serial interface.		
	Note If removed, upon completion of control testing, reinstall parallel input, parallel output, and serial interface.		
	c. Remove vbfo card. Install it on an extender card and place it in the unit.		
	d. Set unit LINE SELECTOR for power source available (100/115/215/230 V ac).		
	Note Ensure that proper fuse is installed for power source used.		
	e. Connect unit to available power source.		
2. Initial check	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to SSB/CW. BANDWIDTH to 16. DIAL to FINE. BFO to HOLD. AGC to FAST. RF GAIN to full cw.		
	b. Measure dc voltages between the following points and ground (TP1).		Check associated power supply.
	P1-23	+15 ±1.0 V dc.	
	P1-27	+5 ±0.5 V dc.	
	c. Measure dc voltage between points A and B (as shown in figure 5).	NMT 0.2 V dc.	Check Q3 and associated circuit.
	Note If external keep-alive voltage is connected to unit under test, perform step 2.d.	**Note** Point A is 5-V dc keep-alive voltage. Point B is 5-V dc supply voltage.	
	d. Measure dc voltage between P1-45 and ground (TP1).	+5.0 to +12.0 V dc (depending on source used).	Check associated power supply.

Table 1. VBFO, Testing, and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. VBFO/450-kHz output switch	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to AM. BANDWIDTH to 16. DIAL to FINE. BFO to FIX. AGC to OFF. RF GAIN to full cw. **Note** Logic 1 = NLT +3.0 V dc. Logic 0 = NMT 0.5 V dc.		
	b. Note logic level at TP8.	Logic 0	Check U21 and associated circuit.
	c. Note output frequency at J1.	0 Hz	Check U21, U29, and associated circuits.
	d. Repeat steps 3.b and 3.c at each of the following conditions:		Same as step 3.b and 3.c.

MODE SWITCH	BFO SWITCH	TP8	J1
AM	TUNE	Logic 0	0 Hz
SSB/CW	FIX	Logic 0	450 kHz
SSB/CW	TUNE	Logic 1	*Vbfo

*Vbfo frequency equals 450 kHz plus the algebraic sum of the vbfo offset.

Caution

In the following procedures, when applying +5 V dc or 0 V dc (ground) to the indicated points, apply these levels through a 100-ohm series limiting resistor. The +5-V dc source should be obtained from the receiver power supply so that the integrated circuit supply voltages are not exceeded by the applied levels.

Note

450-kHz enable (P1-51).

(Cont)	e. Apply +5 V dc to TP4 (rf xmt).		

Table 1. VBFO, Testing, and Troubleshooting Procedures. (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	f. Repeat steps 3.b and 3.c at each of the following conditions:		Same as step 3.b and 3.c.

MODE SWITCH	BFO SWITCH	TP8	J1
AM	FIX	Logic 0	0 Hz
AM	TUNE	Logic 0	0 Hz
SSB/CW	FIX	Logic 0	450 kHz
SSB/CW	TUNE	Logic 1	450 kHz

PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
g. Remove +5 V dc from TP4.		
h. Connect a spectrum analyzer to J1.		
i. Set VBFO OFFSET HZ from 1000 Hz.		
j. Note level of 451-kHz if signal at J1.	Reference.	
k. Measure level of sidebands caused by 300-Hz VBFO reference signal at J1.	NLT 70 dB below 451-kHz reference.	Check bypass and feedthrough capacitors and circuits associated with J1 output or return to factory for repair.
l. Apply +5 V dc to TP4 (rf xmt).		
m. Measure level of 451 kHz if signal at J1.	NLT 70 dB below reference in step 3.j.	Check U29A and associated circuits.
n. Note level of 450 kHz if signal at J1.	Reference.	
o. Remove +5 V dc from TP4.		
p. Measure level of 450-kHz if signal at J1.	NLT 70 dB below reference in step 3.n.	Check U29D and associated circuits.
q. Set VBFO OFFSET HZ for 9990 Hz.		
r. Using a distortion analyzer, measure total harmonic distortion at J1.		
s. Set VBFO OFFSET HZ for 0000 Hz.		
t. Measure total harmonic distortion at J1.	NMT 3%.	Same as step 3.k.
u. Apply +5 V dc to TP4 (rf xmt).		
v. Measure total harmonic distortion at J1.	NMT 3%.	Same as step 3.k.
w. Remove +5 V dc from TP4.		

Table 1. VBFO, Testing, and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. Frequency accuracy	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to SSB/CW. BANDWIDTH to 16. DIAL to FINE. BFO to TUNE. AGC to OFF. RF GAIN to full cw.		
	b. Connect a frequency counter to J1.		
	c. Measure the frequency outputs listed below. Check both positive and negative offset.	±5 Hz of listed output.	Check phase-lock loop.
	d. At each frequency measure vbfo synthesizer fault output using a dvm connected at TP2.	NMT 0.5 V dc.	Check U40C and associated circuit.

OFFSET (Hz)	OUTPUT FREQUENCY	
	POSITIVE OFFSET	NEGATIVE OFFSET
9990	459.99 kHz	440.01 kHz
9980	459.98 kHz	440.02 kHz
9970	459.97 kHz	440.03 kHz
9960	459.96 kHz	440.04 kHz
9950	459.95 kHz	440.05 kHz
9940	459.94 kHz	440.06 kHz
9930	459.93 kHz	440.07 kHz
9920	459.92 kHz	440.08 kHz
9910	459.91 kHz	440.09 kHz
9900	459.90 kHz	440.10 kHz
9800	459.80 kHz	440.20 kHz
9700	459.70 kHz	440.30 kHz
9600	459.60 kHz	440.40 kHz
9500	459.50 kHz	440.50 kHz
9400	459.40 kHz	440.60 kHz
9300	459.30 kHz	440.70 kHz
9200	459.20 kHz	440.80 kHz
9100	459.10 kHz	440.90 kHz
9000	459.00 kHz	441.00 kHz
8000	458.00 kHz	442.00 kHz
7000	457.00 kHz	443.00 kHz
6000	456.00 kHz	444.00 kHz
5000	455.00 kHz	445.00 kHz
4000	454.00 kHz	446.00 kHz
3000	453.00 kHz	447.00 kHz
2000	452.00 kHz	448.00 kHz
1000	451.00 kHz	449.00 kHz
0000	450.00 kHz	450.00 kHz

Table 1. VBFO, Testing, and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. Local operation	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to SSB/CW. BANDWIDTH to 16. DIAL to FINE. BFO to TUNE. AGC to OFF. RF GAIN to full cw.		
	b. Connect an oscilloscope to TP5.		
	c. Note display on oscilloscope while rotating front-panel TUNING knob.	Clock pulses are continuous when TUNING knob is rotated between -9990 and +9990 VBFO OFFSET HZ. When VBFO OFFSET HZ reaches -9990 or +9990, clock pulses cease until the TUNING knob is rotated in the opposite direction. Frequency of clock pulses is increased by rotating the TUNING knob faster and decreased by rotating the TUNING knob slower.	Check U17, U21D, and associated circuit.
	d. Note display on oscilloscope while rotating front-panel TUNING knob. Set BFO switch to HOLD.	Clock pulses cease when BFO switch is set to HOLD. VBFO OFFSET HZ does not change while BFO is in HOLD position.	Check U18, U23, U26, U5D, U22C, and associated circuit.
	e. Set BFO switch to TUNE.		
	f. Apply +5 V dc to P1-32 (vbfo parallel enable).	VBFO OFFSET HZ display blanks.	Check U30, U35, and associated circuit.
	g. Remove +5 V dc from P1-32.	VBFO OFFSET HZ display lights on same frequency as before blanking.	Check U6, U18, U23, U26, U5C, and associated circuit.
(Cont)	h. Connect a ground to P1-30 ($\overline{\text{clock inhibit}}$).	VBFO OFFSET HZ display blanks.	Same as step 5.f.

Table 1. VBFO, Testing, and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	i. Remove P1-30 ground.	VBFO OFFSET HZ display lights on same frequency as before blanking.	Same as step 5.g.
	j. Note display on oscilloscope while rotating front-panel TUNING knob. Set CONT switch to REM.	CONT switch positioning has no effect on clock pulses.	Check U21D, U11A, and associated circuit.
6. Remote control	a. Front-panel controls set as follows: PWR to ON. CONT to REM. MODE to SSB/CW. BANDWIDTH to 16. DIAL to FINE. BFO to TUNE. AGC to OFF. RF GAIN to full cw.		
	b. Apply +5 V dc to P1-32 (vbfo parallel enable).		
	c. Connect an oscilloscope to TP7.		
	d. Momentarily apply +5 V dc to P1-18 (vbfo load).	Pulse at TP7 should be NLT 5 μs and NMT 20 μs.	Check U5C, U6, and associated circuit.
	e. Set CONT switch to LCL.		
	f. Repeat step d.	No pulse at TP7.	Same as step 6.d.
	g. Set CONT switch to REM.		
	h. Remove +5 V dc from P1-32.		
	i. Repeat step d.	No pulse at TP7.	Same as step 6.d.
(Cont)	j. Refer to chart and apply bcd frequency for -1230 vbfo offset frequency.		

Table 1. VBFO, Testing, and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
6. (Cont)			

VBFO OFFSET HZ	VBFO BCD FREQUENCY (HZ)												VBFO SIGN
	1000				100				10				
	8	4	2	1	8	4	2	1	8	4	2	1	
	P1-( )												
	54	26	53	25	52	24	22	49	21	48	20	47	19
-1230	0	0	0	1	0	0	1	0	0	0	1	1	0
0000	0	0	0	0	0	0	0	0	0	0	0	0	1 or 0
+9990	1	0	0	1	1	0	0	1	1	0	0	1	0
-9990	1	0	0	1	1	0	0	1	1	0	0	1	1
+8760	0	1	0	0	0	1	1	1	0	1	1	0	0
-2340	0	0	1	0	0	0	1	1	0	1	0	0	1
Logic 1 = NLT + 3.0 V dc; Logic 0 = NMT 0.5 V dc.													

k. Apply +5 V dc to P1-32 (vbfo parallel enable).		
l. Momentarily apply +5 V dc to P1-18 (vbfo load).	VBFO OFFSET HZ display indicates -1230.	Check inputs.
m. Remove -1230 bcd frequency input. (with no logic 1's applied, vbfo bcd frequency is pulled-down to all logic 0's.	VBFO OFFSET HZ display indicates 0000.	Check associated pull-down circuit.
n. Remove +5 V dc from P1-32.		
o. Set CONT switch to LCL.	VBFO OFFSET HZ display indicates -1230.	Check U18, U23, U26, and associated circuit.
p. Rotate TUNING knob each direction from set frequency.	Counter clockwise counts down, clockwise counts up.	Check input to P1-13 (Logic 1 = up; logic 0 = down), if okay check U17 and associated circuit.
(Cont) q. Set CONT switch to REM.		

Table 1. VBFO, Testing, and Troubleshooting Procedures (Cont)

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
6. (Cont)	r. Repeat steps 6.j thru 6.q. at each bcd frequency listed in chart.	VBFO OFFSET HZ display indicates vbfo bcd frequency applied in step 6.j. for steps 6.l and 6.o. VBFO OFFSET HZ display indicates 0000 for step 6.m. Step 6.p at -9990 will not count down and at +9999 will not count up.	Same as steps 6.j. thru 6.q.
7. Vbfo synthesizer fault	a. Front-panel controls set as follows: PWR to ON. CONT to LCL. MODE to SSB/CW. BANDWIDTH to 16. DIAL to FINE. BFO to TUNE. AGC to OFF. RF GAIN to full cw.		
	b. Using TUNING knob set VBFO OFFSET HZ to 00.		
	c. Measure output at P1-34 (vbfo synthesizer fault).	NMT 0.5 V dc.	Check U20 and associated circuit.
	d. Disconnect 450-kHz reference at J2.		
	e. Measure output at P1-34.	NLT +3.0 V dc.	Same as step 7.c.
	f. Reconnect 450-kHz reference at J2.		
	g. Measure output at P1-34.	NMT 0.5 V dc.	Same as step 7.c.
	h. Repeat steps 7.c thru 7.g with VBFO OFFSET HZ at each of the following settings: +7770 +3330 -3330 -7770	Same as steps 7.c thru 7.g.	Same as step 7.c.
8. External keep-alive (Cont)	a. Front-panel controls set as follows: PWR to ON. CONT to LCL. MODE to SSB/CW. BANDWIDTH to 16. DIAL to FINE. BFO to TUNE. AGC to OFF. RF GAIN to full cw.		

Table 1. VBFO, Testing, and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
8. (Cont)	b. Apply external keep-alive voltage (6 to 12 V dc) to rear panel of unit at TB3-4 (+) and TB3-5 (-).		
	c. Set PWR to off.		
	d. Measure dc voltage at capacitor C9 positive (+) lead.	7.0 ±1.5 V dc.	Check CR3, CR2, Q1, and associated circuit.
	e. Remove external keep-alive voltage.		
9. Internal keep-alive	a. Front-panel controls set as follows: PWR to ON. CONT to LCL. MODE to SSB/CW. BANDWIDTH to 16. DIAL to FINE. BFO to TUNE. AGC to OFF. RF GAIN to full cw.		
	b. Using TUNING knob set VBFO OFFSET HZ to +7770.		
	c. Set BFO to HOLD.		
	d. Set PWR to off.		
	e. After 5 minutes with PWR off, set PWR to on.	VBFO OFFSET HZ display indicates +7770.	Check C9 and associated circuits.
10. Test complete	a. Set PWR switch off.		
	b. Disconnect external power from rear panel.		
	c. Remove vbfo from extender and extender from unit.		
	d. Reinstall vbfo in unit.		
	e. If removed in setup, reinstall parallel input, parallel output, and serial interface.		
	f. Reinstall unit top cover.		

4. ALIGNMENT/ADJUSTMENT.

4.1 Voltage Adjustment

a. Perform table 1, test 1 and test 2.
b. Connect a dvm between bottom end of R28 and ground (TP1).
c. Set front-panel controls as follows:

PWR to on.
CONT to LCL.
MODE to SSB/CW.
BANDWIDTH to 16.
DIAL to FINE.
BFO to TUNE.
AGC to OFF.
RF GAIN to full cw.

d. Adjust R7 for 12.0 ±0.1 V dc at R28.
e. Remove dvm.

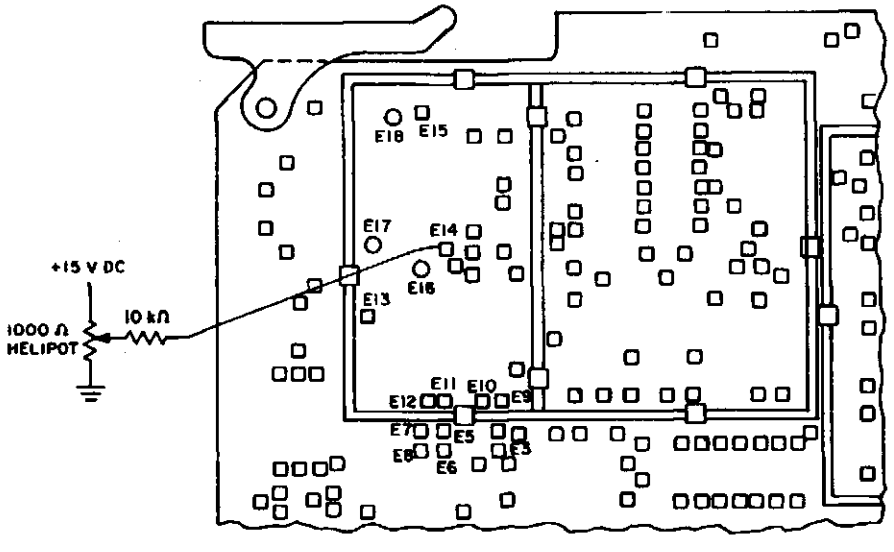
4.1 Oscillator Adjustments.

Note

To perform these adjustments, the oscillator can shield must be removed. Do not make these adjustments unless a repair has been made and necessary adjustment is indicated.

4.2.1 Oscillator Adjustment.

a. Perform table 1, test 2 and test 2.
b. Adjust R30 and R37 to maximum cw position.
c. Connect a helipot to C29, as shown in figure 5.



TPA-1361-011

Setup for Oscillator Adjustments
Figure 5

d. Connect a dvm to C29 (where helipot is connected.).
e. Apply a ground at bottom end of R13.
f. Connect a frequency counter at J1.
g. Set front-panel controls as follows:

PWR to on.
CONT to LCL.
MODE to SSB/CW.
BANDWIDTH to 16.
DIAL to FINE.
BFO to TUNE.
AGC to OFF.
RF GAIN to full cw.

i. Adjust the helipot for 5.5 ±0.1 V dc at C29.
j. Adjust L9 for a frequency of 450.0 ±0.33 kHz at J1. Tuning slug should be toward the top of L9.

4.2.2 Frequency Range

a. Adjust the helipot for 3.5 ±0.1 V dc at C29. Frequency should be 460.00 kHz minimum.
b. Adjust the helipot for 7.3 ±0.1 V dc at C29. Frequency should be 440.00 kHz maximum.

Note

If step a or b is out of range, readjustment of L9 in the direction of the range error could correct the problem. If both steps a and b are out of range, repair is indicated.

c. Remove helipot, dvm, and frequency counter.
d. Remove R13 ground.

4.3 Output Level

a. Perform table 1, test 1 and test 2.
b. Connect an rf voltmeter (with 50-Ω load) to J1.
c. Set front-panel controls as follows:
PWR to on.
CONT to LCL
MODE to SSB/CW.
BANDWIDTH to 16.
DIAL to FINE.
BFO to TUNE.
AGC to OFF.
RF GAIN to full cw.

d. Adjust R30 for 300 ±10 mV rms at J1.
e. Apply +5 V dc at TP4 (yellow).
f. Adjust R37 for 300 ±10 mV rms at J1.
g. Remove +5 V dc from TP4.
h. Remove rf voltmeter.

5. REPAIR

Repair of the vbfo is accomplished using the standard planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

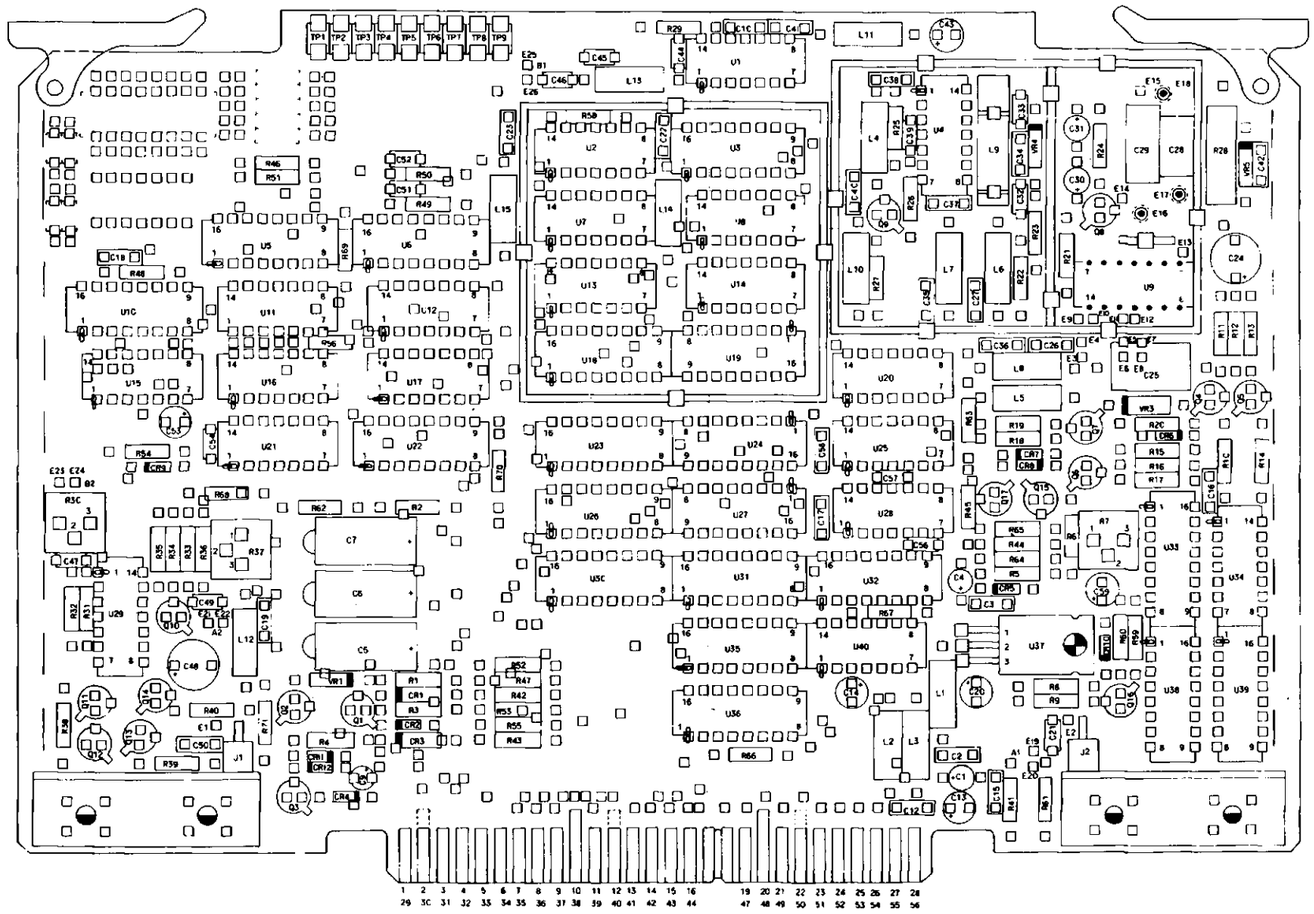
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figure 6). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Vbfo	638-6067-001	REV D



TPA-0809-019

VBFO, Schematic Diagram
Figure 6 (Sheet 1 of 4

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
	VBFO A4	638-6067-001	
CR1	SEMICOND DEVICE 1N3070	353-3083-000	
CR2	SEMICOND DEVICE 1N3070 (A3)	353-3083-000	
CR2	SEMICOND DEVICE 1N4454	353-3644-010	
CR3	SEMICOND DEVICE 1N3070	353-3083-000	
CR4-CR10	SEMICOND DEVICE 1N4454	353-3644-010	
CR11, CR12	SEMICOND DEVICE 1N4454 (A3)	353-3644-010	
C1	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C2,C3	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C4	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C5-C7	CAPACITOR,FXD ELCTLT, 330UF, PORM20%, 20V	184-9117-040	
C8	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V (A3)	913-5019-440	
C9	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C10	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C11	NOT USED		
C12	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C13	CAPACITOR,FXD ELCTLT, 4.7UF, 20%, 35V	184-9102-390	
C14	CAPACITOR,FXD ELCTLT, 22UF, 20%, 10V	184-9102-080	
C15-C19	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C20	CAPACITOR,FXD ELCTLT, 15UF, 20%, 20V	184-9102-180	
C21	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C22,C23	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C24	CAPACITOR,FXD ELCTLT, 47UF, 20%, 20V	184-9102-190	
C25	CAPACITOR,FXD PLSTC DIEL, 0.47UF, 5%, 50V	933-1084-210	
C26,C27	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C28	CAPACITOR,FXD PLSTC DIEL, 0.1UF, 10%, 50V	933-1081-080	
C29	CAPACITOR,FXD PLSTC DIEL, 0.047UF, 10%, 50V	933-1043-500	
C30,C31	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C32,C33	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C34-C38	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C39	CAPACITOR,FXD CER DIEL, 470PF, 10%, 200V	913-4014-000	
C40-C42	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C43	CAPACITOR,FXD ELCTLT, 22UF, 20%, 10V	184-9102-080	
C44	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C45,C46	CAPACITOR,FXD CER DIEL, 470PF, 10%, 200V	913-4014-000	
C47	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C48	CAPACITOR,FXD ELCTLT, 47UF, 20%, 20V	184-9102-190	
C49	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C50	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C51,C52	CAPACITOR,FXD CER DIEL, 100PF, 10%, 200V	913-4006-000	
C53	CAPACITOR,FXD ELCTLT, 10UF, 20%, 25V	184-9102-240	
C54	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C55	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V (A2)	913-4018-000	
C56,C57	CAPACITOR,FXD CER DIEL, 100PF, 10%, 200V	913-4006-000	
C58	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C59	CAPACITOR,FXD ELCTLT, 10UF, 20%, 25V (A4)	184-9102-240	
C60	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V (A5)	913-5019-440	
J1,J2	CONNECTOR,RCPT ELEC	357-7207-100	
L1	COIL,RF 33UH	240-2715-310	
L2,L3	COIL,RF 1UH	240-2715-130	
L4-L8	COIL,RF 10UH	240-2715-250	
L9	COIL,RF,VAR 2.4 TO 3.6UH	240-2739-010	
L10,L11	COIL,RF 10UH	240-2715-250	
L12	COIL,RF 1000UH	240-2715-490	
L13	COIL,RF 330UH	240-2715-430	
L14,L15	COIL,RF 10UH	240-2715-250	
Q1	TRANSISTOR 2N4091	352-0759-010	
Q2-Q5	TRANSISTOR 2N2222A	352-0661-020	
Q6	TRANSISTOR 2N2907A	352-0551-010	
Q7	TRANSISTOR 2N2222A	352-0661-020	
Q8	SEMICOND DEVICE 2N3796	352-1018-010	
Q9	TRANSISTOR 2N2369A	352-0596-030	
Q10-Q17	TRANSISTOR 2N2222A	352-0661-020	
R1	RESISTOR,FXD CMPSN, 33 OHMS, 10%, 1/4W	745-0695-000	
R2	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W (A3)	745-0821-000	
R2	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W	745-0809-000	
R3	RESISTOR,FXD CMPSN, 0.15MEGO, 10%, 1/4W (A3)	745-0827-000	
R3	RESISTOR,FXD CMPSN, 33K, 10%, 1/4W	745-0803-000	
R4	RESISTOR,FXD CMPSN, 22K, 10%, 1/4W (A3)	745-0797-000	
R4	RESISTOR,FXD CMPSN, 27K, 10%, 1/4W	745-0800-000	
R5	RESISTOR,FXD FILM, 243 OHMS, 1%, 1/8W (A4)	705-3600-670	
R5	RESISTOR,FXD FILM, 226 OHMS, 1%, 1/8W	705-0965-000	
R6	RESISTOR,FXD FILM, 1.91K, 1%, 1/8W	705-3605-130	
R7	RESISTOR,VAR 200 OHMS, 20%, 1/2W	382-0038-020	
R8	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000	
R9	RESISTOR,FXD CMPSN, 1K, 10%, 1/4W	745-0749-000	
R10	RESISTOR,FXD CMPSN, 5.6K, 10%, 1/4W	745-0776-000	
R11	RESISTOR,FXD CMPSN, 15K, 10%, 1/4W	745-0791-000	
R12	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/4W	745-0713-000	
R13	RESISTOR,FXD CMPSN, 15K, 10%, 1/4W	745-0791-000	
R14	RESISTOR,FXD CMPSN, 5.6K, 10%, 1/4W	745-0776-000	
R15	RESISTOR,FXD CMPSN, 330 OHMS, 10%, 1/4W	745-0731-000	
R16	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000	
R17	RESISTOR,FXD CMPSN, 68 OHMS, 10%, 1/4W	745-0707-000	
R18	RESISTOR,FXD CMPSN, 5.6K, 10%, 1/4W	745-0776-000	
R19	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/4W	745-0755-000	
R20	RESISTOR,FXD CMPSN, 33 OHMS, 10%, 1/4W	745-0695-000	
R21	RESISTOR,FXD FILM, 14.7K, 1%, 1/8W	705-1052-000	
R22	RESISTOR,FXD FILM, 31.6K, 1%, 1/8W	705-1068-000	
R23	RESISTOR,FXD FILM, 46.4K, 1%, 1/8W	705-1076-000	
R24	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W	745-0809-000	
R25	RESISTOR,FXD CMPSN, 3.9K, 10%, 1/4W	745-0770-000	
R26	RESISTOR,FXD CMPSN, 1K, 10%, 1/4W	745-0749-000	
R27	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/4W (A4)	745-0713-000	

PARTS LIST (Cont)

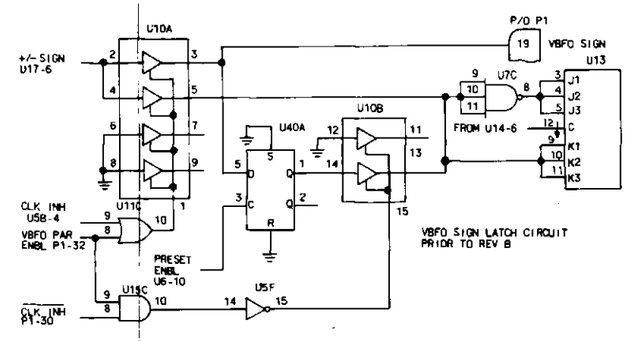
REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
R27	RESISTOR,FXD CMPSN, 180 OHMS, 10%, 1/4W	745-0722-000	
R28	RESISTOR,FXD FILM, 20.5K, 1%, 1/8W	705-1059-000	
R29	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/4W (A4)	745-0761-000	
R29	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/4W	745-0755-000	
R30	RESISTOR,VAR 1K, 20%, 1/2W	382-0038-040	
R31	RESISTOR,FXD CMPSN, 27K, 10%, 1/4W	745-0800-000	
R32	RESISTOR,FXD CMPSN, 33K, 10%, 1/4W (A4)	745-0803-000	
R32	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W	745-0809-000	
R33	RESISTOR,FXD CMPSN, 15K, 10%, 1/4W	745-0791-000	
R34	RESISTOR,FXD CMPSN, 12K, 10%, 1/4W	745-0788-000	
R35	RESISTOR,FXD CMPSN, 1K, 10%, 1/4W	745-0749-000	
R36	RESISTOR,FXD CMPSN, 820 OHMS, 10%, 1/4W (A4)	745-0746-000	
R36	RESISTOR,FXD CMPSN, 680 OHMS, 10%, 1/4W	745-0743-000	
R37	RESISTOR,VAR 200 OHMS, 20%, 1/2W (A4)	382-0038-020	
R37	RESISTOR,VAR 1K, 20%, 1/2W	382-0038-040	
R38	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000	
R39	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/4W	745-0713-000	
R40	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000	
R41	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W (A4)	745-0785-000	
R41	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R42,R43	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R44	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W (A4)	745-0857-000	
R44	RESISTOR,FXD CMPSN, 56K, 10%, 1/4W	745-0812-000	
R45	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000	
R46-R48	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R49,R50	RESISTOR,FXD CMPSN, 4.7K, 10%, 1/4W (A4)	745-0773-000	
R49,R50	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000	
R51-R53	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R54	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000	
R55	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R56	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000	
R57	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W (A6)	745-0821-000	
R58-R60	RESISTOR,FXD CMPSN, 1K, 10%, 1/4W	745-0749-000	
R61	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/4W	745-0713-000	
R62	RESISTOR,FXD CMPSN, 1K, 10%, 1/4W (A3)	745-0749-000	
R62	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000	
R63,R64	RESISTOR,FXD CMPSN, 1K, 10%, 1/4W	745-0749-000	
R65	RESISTOR,FXD CMPSN, 56K, 10%, 1/4W	745-0812-000	
R66	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W (A4)	745-0857-000	
R67	RESISTOR,FXD CMPSN, 56K, 10%, 1/4W (A4)	745-0812-000	
R68-R70	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W (A4)	745-0857-000	
TP1	JACK,TIP BRN	360-0484-070	
TP2	JACK,TIP RED	360-0484-020	
TP3	JACK,TIP ORN	360-0484-050	
TP4	JACK,TIP YEL	360-0484-060	
TP5	JACK,TIP GRN	360-0484-040	
TP6	JACK,TIP BLU	360-0484-080	
TP7	JACK,TIP VIO	360-0484-090	
TP8	JACK,TIP GRA	360-0484-100	
TP9	JACK,TIP WHT	360-0484-010	
U1	INTEGRATED CKT SN74LS90N	351-1636-010	
U2	INTEGRATED CKT SN74LS21N	351-1785-010	
U3	INTEGRATED CKT 74H106PC	351-7766-010	
U4	INTEGRATED CKT MC1648010	351-7768-010	
U5	INTEGRATED CKT F4049BPC	351-8159-210	
U6	INTEGRATED CKT MC14528BCP	351-8421-020	
U7	INTEGRATED CKT DM74LS10N	351-1523-230	
U8	INTEGRATED CKT N74LS00N	351-1523-110	
U9	INTEGRATED CKT MC14066BCP	351-8252-010	
U10	INTEGRATED CKT MC14503BCP	351-8490-010	
U11	INTEGRATED CKT MC14071BCP	351-8287-010	
U12	INTEGRATED CKT MC14011CP	351-8159-040	
U13,U14	INTEGRATED CKT 74H102	351-7767-010	
U15	INTEGRATED CKT CD4081BE (A1)	351-8287-030	
U15	INTEGRATED CKT MC14011CP	351-8159-040	
U16	INTEGRATED CKT MC14073BCP	351-8287-060	
U17	INTEGRATED CKT CD4095BE	351-8537-010	
U18	INTEGRATED CKT CD14510BCN	351-8497-010	
U19	INTEGRATED CKT SN74LS190N (A5)	351-1527-040	
U19	INTEGRATED CKT SN74LS190N	351-1948-010	
U20	INTEGRATED CKT N74LS74N883C	351-1525-040	
U21	INTEGRATED CKT MC14081BCP	351-8287-030	
U22	INTEGRATED CKT F4049BPC	351-8159-210	
U23	INTEGRATED CKT CD14510BCN	351-8497-010	
U24	INTEGRATED CKT SN74LS190N (A5)	351-1527-040	
U24	INTEGRATED CKT SN74LS190N	351-1948-010	
U25	INTEGRATED CKT N74LS00N	351-1523-010	
U26	INTEGRATED CKT CD4510BCN	351-8497-010	
U27	INTEGRATED CKT SN74LS190N (A5)	351-1527-040	
U27	INTEGRATED CKT SN74LS190N	351-1948-010	
U28	INTEGRATED CKT N74LS74N883C	351-1525-040	
U29	INTEGRATED CKT MC14066BCP	351-8252-010	
U30	INTEGRATED CKT MC14503BCP	351-8490-010	
U31-U33	INTEGRATED CKT SN74LS190N (A5)	351-1527-040	
U31-U33	INTEGRATED CKT SN74LS190N	351-1948-010	
U34	INTEGRATED CKT DM74LS10N	351-1523-230	
U35	INTEGRATED CKT MC14503BCP	351-8490-010	
U36	RESISTOR NTWK 220K, 5%, 1.25W PKG	350-4030-010	
U37	INTEGRATED,CKT LM317T	351-1271-010	
U38	INTEGRATED CKT SN74LS193N	351-1527-060	
U39	INTEGRATED CKT SN74LS190N (A5)	351-1527-040	
U39	INTEGRATED CKT SN74LS190N	351-1948-010	
U40	INTEGRATED CKT F4013BPC (A1)	351-8159-110	
U40	INTEGRATED CKT MC14011UBPC (A4)	351-8159-040	
U41	INTEGRATED CKT MC14011UBPC (A4)	351-8159-040	

PARTS LIST (Cont)

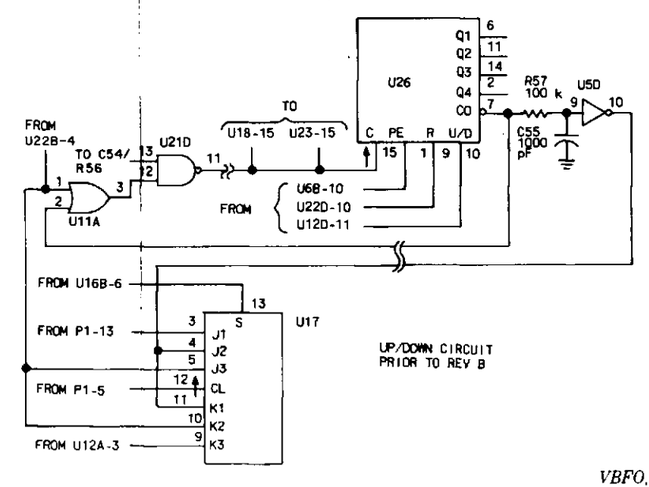
REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
VR1	SEMICOND DEVICE 1N4625 (A3)	353-3591-490	
VR1	SEMICOND DEVICE 1N4104	353-3591-060	
VR2	SEMICOND DEVICE 1N4627 (A3)	353-3591-510	
VR3	SEMICOND DEVICE 1N758A	353-2724-000	
VR4	SEMICOND DEVICE 1N5148A	922-6095-200	
VR5	SEMICOND DEVICE 1N4625	353-3591-490	

MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
	Note Changes A1 thru A4 may have been factory installed in some units prior to REV B. Inspection of the unit will determine if these changes are installed.	
A1	VBFO sign latch circuit changed. Circuit was as shown in diagram below. Deleted U40, type F4013BPC. Changed U15 from type CD4081BE to type MC14011CP.	REV B and above

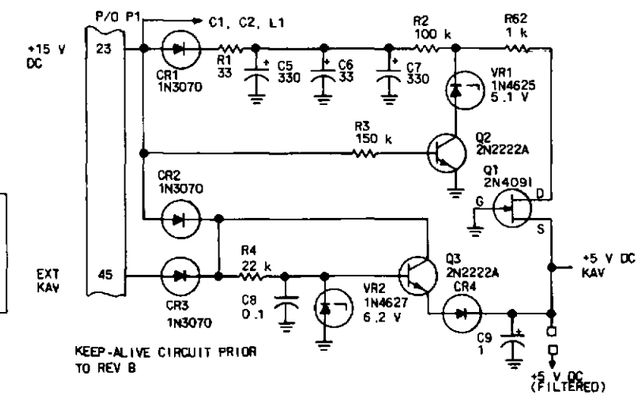


A2	Up/down circuit changed. Circuit was a shown in diagram below. Deleted C55,00pF	REV B and above



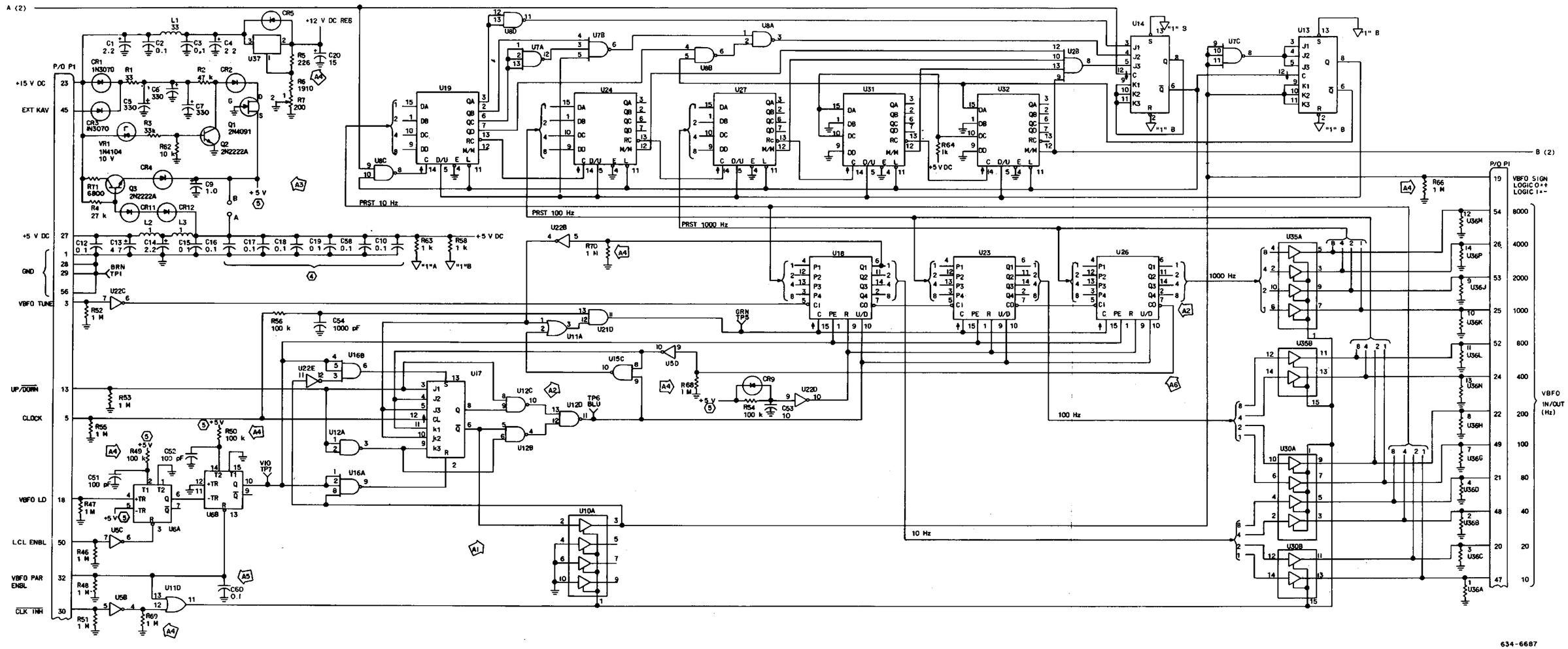
MODIFICATION HISTORY (Cont)

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A3	External KAV (keep-alive voltage) circuit changed. Circuit was as shown in diagram below. Deleted: C8, 0.1µF. VR2, type IN4627. Changed: CR2 from type IN3070 to type IN4454. R2 from 100kΩ to 47kΩ. R3 from 150kΩ to 33kΩ. R4 from 22kΩ to 27kΩ. R62 from 1kΩ to 10kΩ. VR1 from type IN4625 to type IN4104 Added: CR11, type IN4454. CR12, type IN4454. R71, 6800Ω.	REV B and above

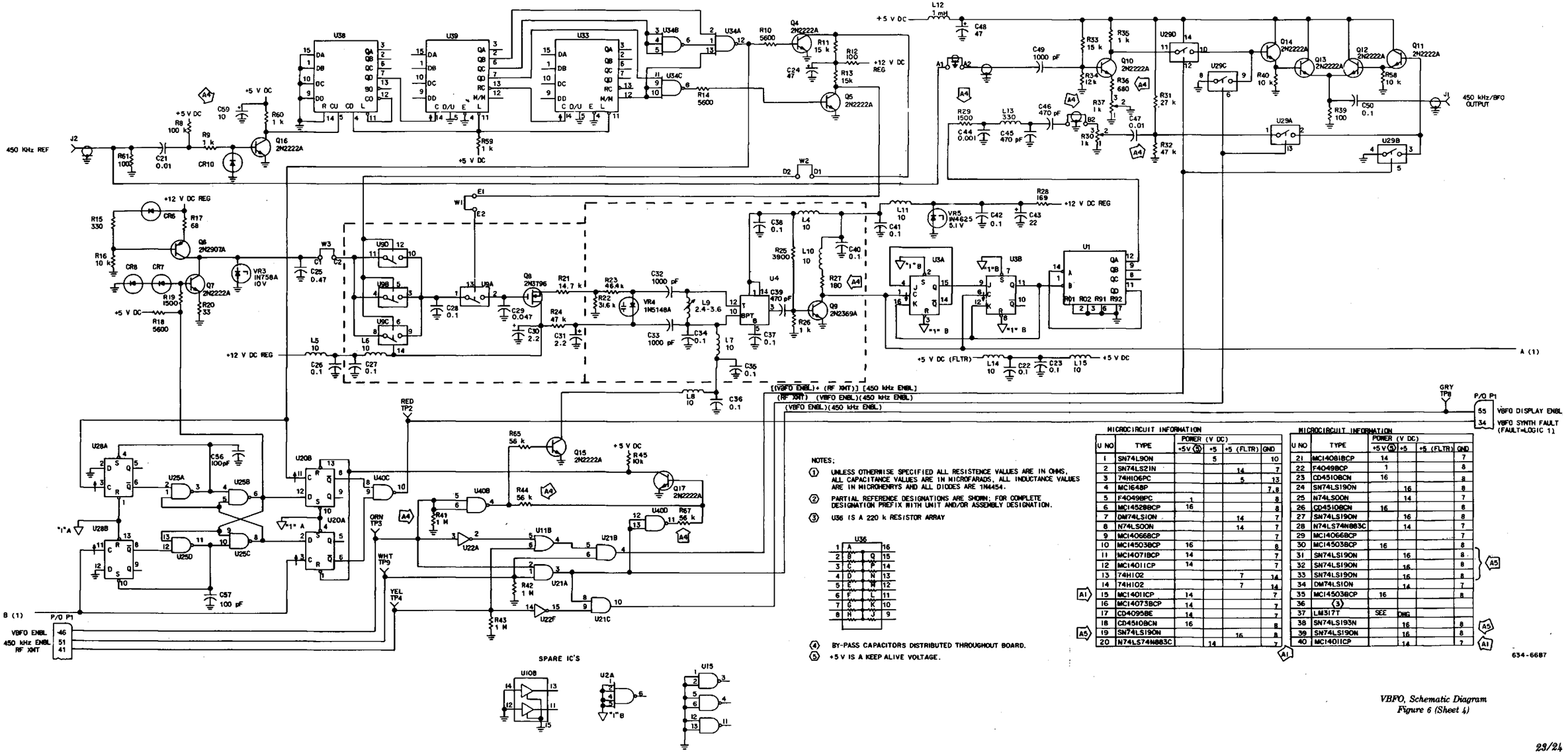


A4	Changed: R5 from 243Ω to 226Ω. R27 from 100Ω to 180Ω. R29 from 2200Ω to 1500Ω. R32 from 33kΩ to 47kΩ. R36 from 820Ω to 680Ω. R37 from 200Ω variable to 1kΩ variable. R41 from 10kΩ to 1MΩ. R44 from 1Mn to 56kΩ. R49 from 4700Ω to 100kΩ. R50 from 4700Ω to 100kΩ. U41, type MC14011CP to U40, type MC14011CP Added: C59, 10µF. R66, 1MΩ. R67, 56kΩ. R68, 1MΩ. R69, 1MΩ. R70, 1MΩ.	REV B and above.
A5	Changed U19, U24, U27, U31, U32, U33, and U39 from type SN74LS190N to type Added C60, 0.1µF.	REV C and above.
A6	Deleted R57, 100kΩ from in series with U26-7 and U5D-9.	REV D and above.

VBFO, Schematic Diagram
Figure 6 (Sheet 2)



VBFO, Schematic Diagram
Figure 6 (Sheet 3)



NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL RESISTENCE VALUES ARE IN OHMS, ALL CAPACITANCE VALUES ARE IN MICROFARADS, ALL INDUCTANCE VALUES ARE IN MICROHENRYS AND ALL DIODES ARE 1N4454.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. U36 IS A 220 k RESISTOR ARRAY

4. BY-PASS CAPACITORS DISTRIBUTED THROUGHOUT BOARD.
5. +5 V IS A KEEP ALIVE VOLTAGE.

MICROCIRCUIT INFORMATION

	U NO	TYPE	POWER (V DC) +5V (5)	+5	+5 (FLTR)	GND
	1	SN74L90N		5		10
	2	SN74LS21N			14	7
	3	74H106PC			5	13
	4	MC1648P				7,8
	5	F4049BPC	1			8
	6	MC14528BCP	16			8
	7	DM74LS10N			14	7
	8	N74LS00N			14	7
	9	MC14066BCP				7
	10	MC14503BCP	16			8
	11	MC14071BCP	14			7
	12	MC14011CP	14			7
	13	74H102			7	14
	14	74H102			7	14
A1	15	MC1401ICP	14			7
	16	MC14073BCP	14			7
	17	CD4095BE	14			7
	18	CD4510BCN	16			8
A5	19	SN74LS190N			16	8
	20	N74LS74N883C		14		7

MICROCIRCUIT INFORMATION

	U NO	TYPE	POWER (V DC) +5V (5)	+5	+5 (FLTR)	GND	
	21	MC14081BCP	14			7	
	22	F4049BCP	1			8	
	23	CD4510BCN	16			8	
	24	SN74LS190N		16		8	
	25	N74LS00N		14		7	
	26	CD4510BCN	16			8	
	27	SN74LS190N		16		8	
	28	N74LS74N883C		14		7	
	29	MC14066BCP				7	
	30	MC14503BCP	16			8	
	31	SN74LS190N		16		8	A5
	32	SN74LS190N		16		8	
	33	SN74LS190N		16		8	
	34	DM74LS10N		14		7	
	35	MC14503BCP	16			8	
	36	(3)					
	37	LM317T	SEE	DWG			
A5	38	SN74LS193N		16		8	A5
	39	SN74LS190N		16		8	A1
A1	40	MC14011CP		14		7	

634-6687

VBFO, Schematic Diagram
Figure 6 (Sheet 4)

Receive Audio (635-0748-001)

Rockwell International

instructions

Collins Telecommunications Products Division

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1st Revision, 1 January 1979

1. DESCRIPTION

Receive Audio 635-0748-001, shown in figure 1, is a 2-layer planar card with a 56-pin edge-on connector (2 layers, 28 pins each).

The receive audio card consists of audio input switching circuits, channel A line audio amplifier, channel B line audio amplifier, headphone audio amplifier, speaker audio amplifier, and squelch control circuits.

2. PRINCIPLES OF OPERATION

2.1 General

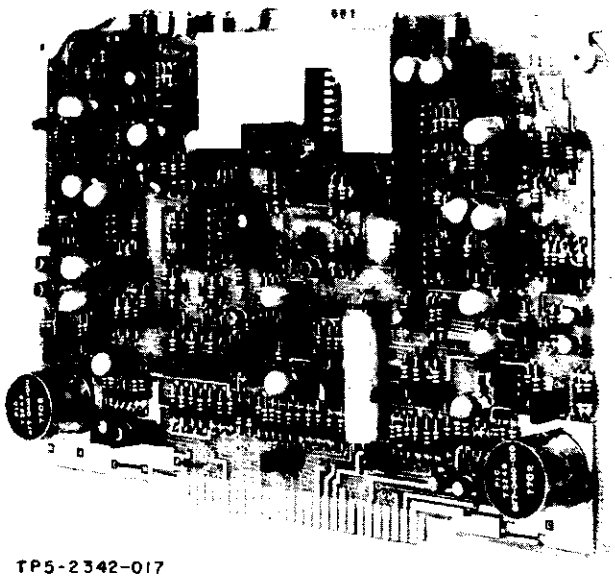
The receive audio card receives audio inputs from AM audio, FM audio, SSB audio, ISB audio, or sidetone audio circuits. These inputs are switched to common line audio amplifiers and supplied through output audio circuits to other audio circuits, speakers, headphones, and performance monitors.

The receive audio card also receives a level controlled speaker audio input and supplies a squelch/mute controlled speaker audio output.

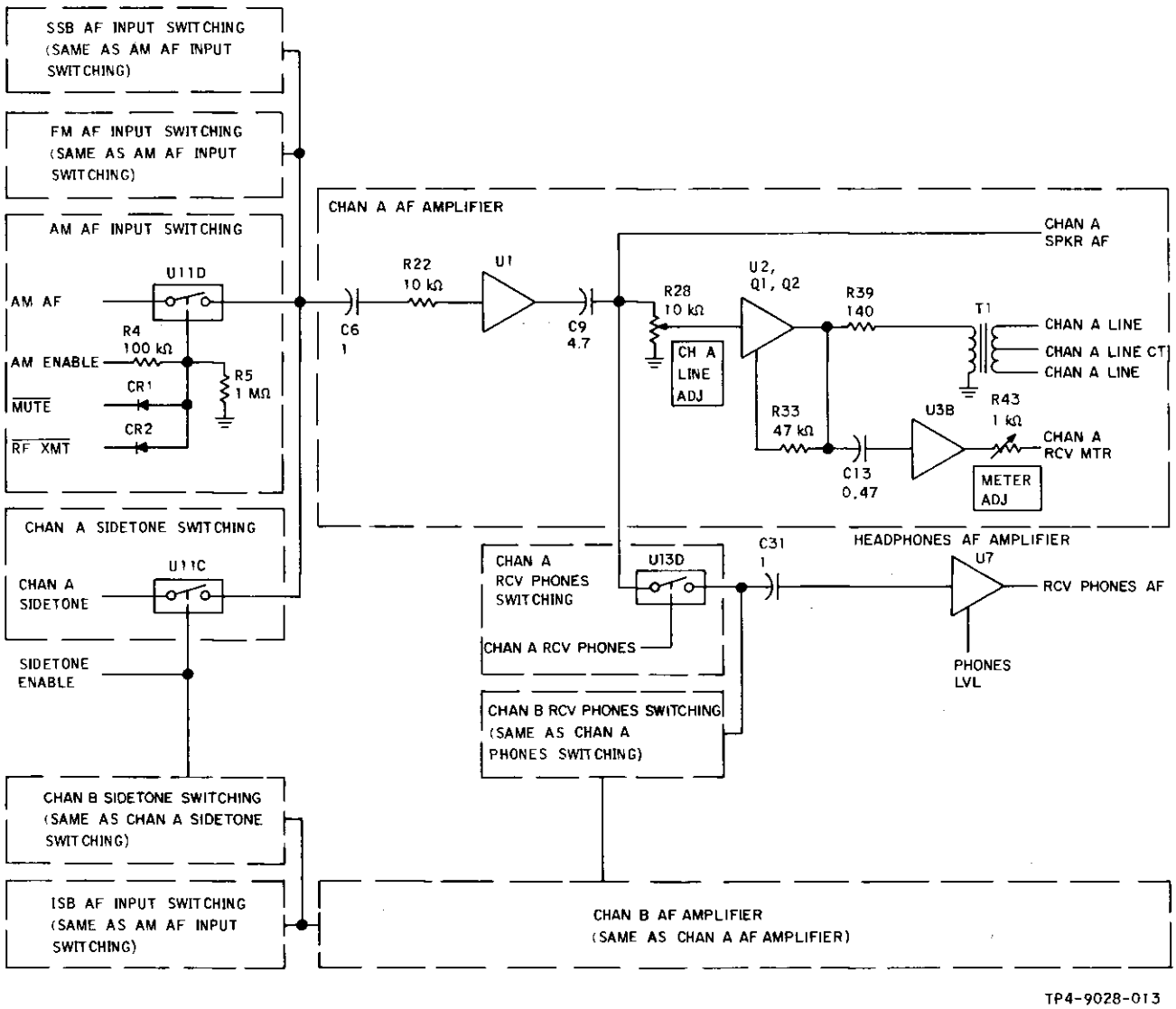
2.2 Audio Input Switching (Refer to figure 2.)

Since the audio input switching circuits are identical for all modes, the following discussion centers on the AM af (audio) input switching.

With an AM audio signal and an AM enable signal applied to bilateral switch U11D, AM audio is supplied through closed switch U11D to the input of the channel A audio amplifier. With a mute or rf xmt signal applied, the AM enable signal is removed. Switch U11D cannot be closed, and the AM audio signal is muted from the input of the channel A audio amplifier.



Receive Audio
Figure 1



Audio Input Switching and Associated Amplifiers
Figure 2

With a channel A sidetone signal and a sidetone enable signal applied to bilateral switch U11C, sidetone is applied through closed switch U11C to the input of the channel A audio amplifier. Note that sidetone and a sidetone enable signal are supplied only during transmit; thus the rf xmt signal is applied to all other audio input switching circuits and mutes these other audio signals.

2.3 Line Audio Amplifiers (Refer to figure 2.)

The line audio amplifiers consist of a channel A audio amplifier and a channel B audio amplifier. These two line audio amplifiers are identical in operation; thus the following paragraphs discuss only the channel A audio amplifier.

An audio input to the channel A audio amplifier is amplified by U1 and supplied as three audio outputs: input to the speaker audio amplifier, input to the headphones audio amplifier, and input to the channel A line audio amplifier.

The input to the channel A line audio amplifier is level controlled by the CH A LINE ADJ potentiometer and amplified by amplifiers U2, Q1, and Q2. The output of these amplifiers is supplied to performance monitor U3B and audio output transformer

T1. Audio output transformer T1 provides a balanced 600-ohm audio output for external use. U3B provides an adjustable (METER ADJ potentiometer) dc level output to the channel A receive level meter to allow constant monitoring of the channel A audio output level.

2.4 Headphones Audio Amplifier (Refer to figure 2.)

With an audio signal from the channel A input audio amplifier and a channel A receive phones enable signal applied, audio is supplied through closed bilateral switch U13D to headphones amplifier U7. The output of U7 is level controlled externally and supplies audio for an external headphone set.

The channel B headphone audio circuit is identical to the channel A circuit.

2.5 Speaker Audio Amplifier (Refer to figure 3.)

With a speaker audio input signal applied to transistor switch Q9 and the squelch signal removed from Q9, audio is supplied through a closed switch to speaker amplifier U8.

When a squelch signal is applied to Q9, Q9 is opened and speaker audio is squelched.

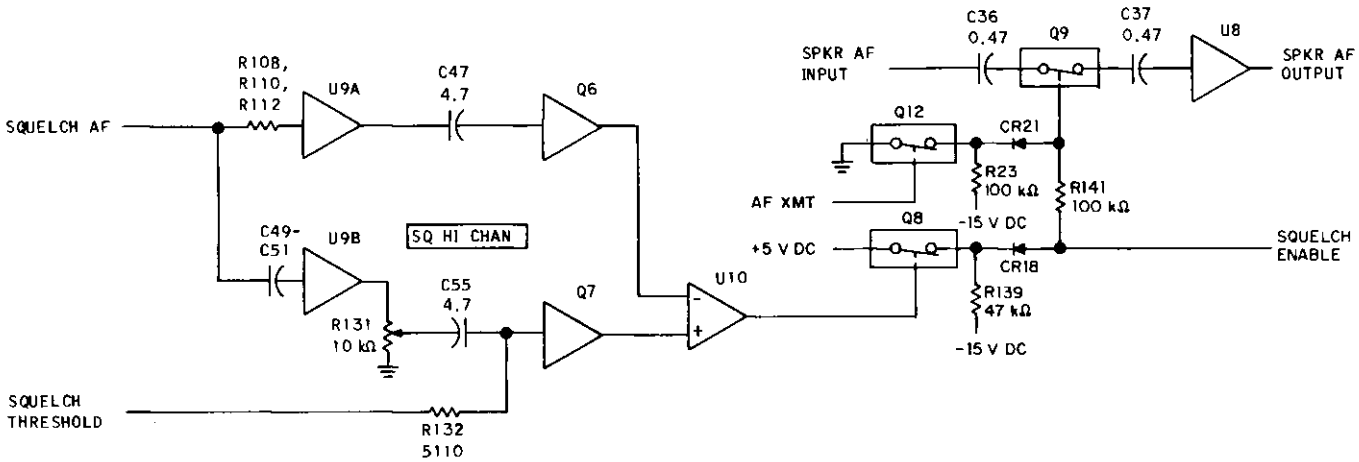
A speaker squelch signal can be applied from one of three sources; squelch enable input, af xmt input, or squelch control circuit.

2.6 Squelch Control Circuit (Refer to figure 3.)

Squelch audio (or noise) signals are supplied at squelch low channel input amplifier U9A and squelch high channel input amplifier U9B. The squelch low-channel signal is level detected by Q6 and applied to the inverting input of U10. The squelch high channel signal is level detected by R131 and Q7 and applied to the noninverting input of U10. When the output of Q7 is lower than the output of Q6, a negative signal is applied from U10 to Q8. Q8 is closed and the squelch signal is removed from Q9. When the output of Q7 exceeds the output of Q6, a positive signal is applied from U10 to Q8. Q8 is opened and the squelch signal is applied to Q9 (noise only or squelched audio condition).

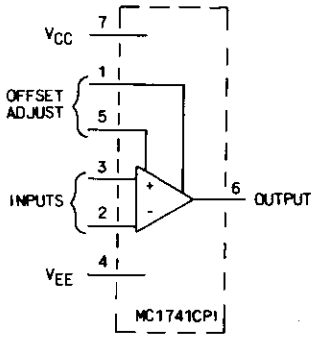
2.7 Operational Amplifier MC1741CP1 (Refer to figure 4.)

The MC1741CP1 is an operational amplifier designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.



TP4-9027-013

Speaker Amplifier and Squelch Control Circuit
Figure 3



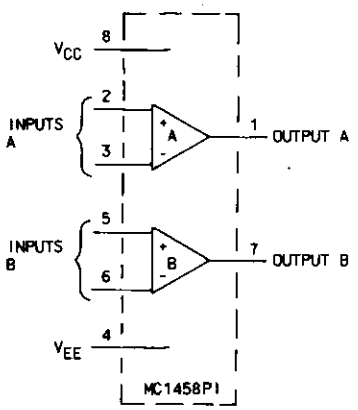
CHARACTERISTICS

SUPPLY VOLTAGE: V_{CC} +22 V DC MAX
V_{EE} -22 V DC MAX
INPUT DIFF VOLTAGE: ±30 V MAX
INPUT COMMON MODE VOLTAGE:
±15 V MAX (1)
OUTPUT SHORT CIRCUIT DURATION:
CONTINUOUS (2)
INPUT RESISTANCE: 300 kΩ MIN, 2.0 MΩ MAX
OUTPUT RESISTANCE: 75Ω TYPICAL
VOLTAGE GAIN: 25 MIN

NOTES:
(1) FOR SUPPLY VOLTAGE LESS THAN ±15.0 V, MAX INPUT VOLTAGE EQUAL TO SUPPLY VOLTAGE.
(2) SUPPLY VOLTAGE EQUAL TO OR LESS THAN 15 V.

TP5-2286-013

Operational Amplifier MC1741CP1
Figure 4



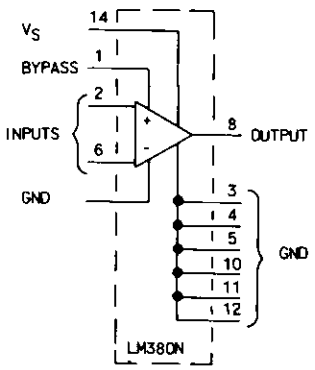
CHARACTERISTICS

SUPPLY VOLTAGE: V_{CC} +18 V DC MAX
V_{EE} -18 V DC MAX
INPUT DIFF VOLTAGE: ±30 V MAX
INPUT COMMON MODE VOLTAGE:
±15 V MAX (1)
OUTPUT SHORT CIRCUIT DURATION:
CONTINUOUS (2)
INPUT RESISTANCE: 300 kΩ MIN, 2.0 MΩ MAX
OUTPUT RESISTANCE: 75Ω TYPICAL
VOLTAGE GAIN: 15 MIN

NOTES:
(1) FOR SUPPLY VOLTAGE LESS THAN ±15.0 V, MAX INPUT VOLTAGE EQUAL TO SUPPLY VOLTAGE.
(2) SUPPLY VOLTAGE EQUAL TO OR LESS THAN 15 V.

TP5-2285-013

Dual Operational Amplifier MC1458P1
Figure 5



CHARACTERISTICS

SUPPLY VOLTAGE: +22 V DC MAX
INPUT DIFF VOLTAGE: ±0.5 V MAX
BANDWIDTH: 100 kHz TYPICAL
INPUT RESISTANCE: 150 kΩ TYPICAL
OUTPUT RESISTANCE: 8Ω TYPICAL
VOLTAGE GAIN: 40 MIN, 60 MAX
OUTPUT VOLTAGE SWING: 14 V p-p TYPICAL
OUTPUT POWER: 2.5 W MIN

TP5-2284-013

Audio Power Amplifier LM380N
Figure 6

2.8 Dual Operational Amplifier MC1458P1 (Refer to figure 5.)

The MC1458P1 consists of two operational amplifiers in one package designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components.

2.9 Audio Power Amplifier LM380N (Refer to figure 6.)

The LM380N is an audio power amplifier with an internal fixed gain of 34 dB.

2.10 COS/MOS Quad Bilateral Switch CD4066 (Refer to figure 7.)

CD4066 consists of four bilateral switches in one package. The CD4066 bilateral switches exhibit a low closed-switch impedance (60 to 360 Ω typical) and relative constant impedance (±5 Ω) over the full input signal range.

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the receive audio card are listed in the maintenance section of this instruction book.

3.2 Testing

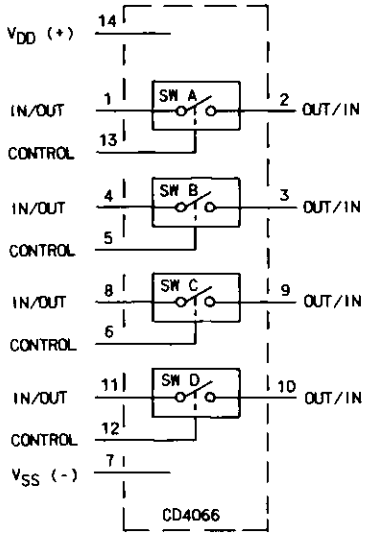
The test procedures in table 1 check the total performance of the receive audio card. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

4. ALIGNMENT/ADJUSTMENT

4.1 Channel A Receive Line Amplifier Adjustment

Adjustment of CH A RCV LINE ADJ (R28) is as follows:

a. Perform test setup of table 1, test 1.
b. Set front-panel MODE switch to AM.
c. Connect an audio oscillator to P1-35.
d. Set the audio oscillator to 1000 Hz at 10-mV rms output.
e. Connect a 600-Ω load across CH A AUD OUT terminals.
f. Connect an audio voltmeter across 600-Ω load.
g. Adjust CH A LINE ADJ (R28) for a 0-dB mW (+775-mV rms) reading on audio voltmeter.



TYPICAL CHARACTERISTICS

V_{DD} TO V_{SS} VOLTS	CONTROL VOLTS	CLOSED-SWITCH IMPEDANCE		TYPICAL OPEN-SWITCH IMPEDANCE
		TYPICAL	MAX	
15	15	60-145Ω	220-320Ω	10 kΩ
10	10	89-190Ω	400-550Ω	10 kΩ
5	5	160-360Ω	3000-5500Ω	10 kΩ

NOTE: CONTROL VOLTAGE MUST EQUAL V_{DD} TO CLOSE SWITCH.
CONTROL VOLTAGE MUST EQUAL V_{SS} TO OPEN SWITCH.

TP5-2283-013

COS/MOS Quad Bilateral Switch CD4066
Figure 7

Table 1. Receive Audio, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of unit containing the receive audio that is to be tested.		
	b. Remove receive audio card. Install it on an extender card and place it in the unit.		
	c. Set unit LINE SELECTOR switch to 115 V.		
	d. Connect unit to 115-V ac power source and set power on.		
	e. Measure dc voltages between the following pins and ground (TP1, brown):		
	P1-23	+15 ±1.0 V dc.	Check associated power supply.
	P1-27	+5 ±0.5 V dc.	
	P1-6	-15 ±1.0 V dc.	
	P1-18	+18 ±1.0 V dc.	
2. Channel A, line amplifier gain	a. Set front-panel MODE switch to AM.		
	b. Connect an audio oscillator to P1-35.		
	c. Adjust audio oscillator for 1000 Hz at 10 mV rms.		
	d. Connect a 600-Ω load across CH A AUD OUT terminals.		
	e. Connect an oscilloscope across the 600-Ω load.		
	f. Adjust R28 for maximum output with no visible distortion.		
	g. Connect audio voltmeter across 600-Ω load. Note output level.	NLT +15 dB mW.	Check Q1, Q2, U1, U2, and associated circuits.
	h. Adjust R28 for +10-dB mW output.	Reference.	
	i. Set front-panel MODE switch to SSB/CW.		
	j. Connect the audio oscillator to P1-34.		
	k. Set audio oscillator for 1000 Hz at 10 mV rms.		
	l. Note output level.	+10 ±1 dB mW.	If too high check U11D and associated circuit.
	Note Steps m thru p are applicable only if receiver has FM MODE switch position.		If too low check U11A and associated circuit.
(Cont)			

Table 1. Receive Audio, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	m. Connect the audio oscillator to P1-7.		
	n. Set front-panel MODE switch to FM.		
	o. Set audio oscillator for 1000 Hz at 10 mV rms.		
	p. Note output level.	+10 ±1 dB mW.	Check U11B and associated circuit.
	q. Connect an 800-Ω load between P1-5 and ground.		
	r. Connect the audio oscillator to P1-5.		
	s. Apply +5-V dc signal to P1-38.		
	t. Set audio oscillator for 1000 Hz at 10 mV rms.		
	u. Note output level.	+10 ±1 dB mW.	Check U11C and associated circuit.
	v. Remote +5 V dc from P1-38.		
	w. Set front-panel MODE switch to AM.		
	x. Connect the audio oscillator to P1-35.		
	y. Adjust audio oscillator for 1000 Hz at 10 mV rms.		
	z. Adjust R28 for 0-dB mW output level.		
3. Channel A, frequency response	a. Set front-panel MODE switch to AM.		
	b. Connect an audio oscillator to P1-35.		
	c. Connect a 600-Ω load across CH A AUD OUT terminals.		
	d. Connect an audio voltmeter across 600-Ω load.		
	e. Adjust audio oscillator from 0 to 10 000 Hz with a constant 10-mV rms output.		
	f. Note maximum level and frequencies at point 1 dB below maximum level.	Upper 1 dB frequency NLT 8000 Hz, NMT 12 kHz. Lower 1 dB frequency, NMT 250 Hz.	Check Q1, Q2, U1, U2, and associated circuits.
4. Channel A, total harmonic distortion (Cont)	a. Set front-panel MODE switch to AM.		
	b. Connect an audio oscillator to P1-35.		
	c. Connect a 600-Ω load across CH A AUD OUT terminals.		

Table 1. Receive Audio, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	d. Connect distortion analyzer across 600-Ω load.		
	e. Adjust audio oscillator to 300 Hz at 10-mV rms output.		
	f. Measure total harmonic distortion using distortion analyzer.	NMT 3%.	Check bypass and dc blocking capacitors.
	g. Repeat step f with audio oscillator set at:		
	1000 Hz 6000 Hz	NMT 0.5%. NMT 0.5%.	Same as step f.
5. Channel B, line amplifier gain	a. Set front-panel MODE switch to ISB.		
	b. Connect an audio oscillator to P1-50.		
	c. Adjust audio oscillator for 1000 Hz at 10 mV rms.		
	d. Connect a 600-Ω load across CH B AUD OUT terminals.		
	e. Connect an oscilloscope across the 600-Ω load.		
	f. Adjust R65 for maximum output with no visible distortion.		
	g. Note output level.	NLT 15 dB mW.	Check Q4, Q5, U4, U5, and associated circuits.
	h. Adjust R65 for +10-dB mW output.		
	i. Connect an 800-Ω load between P1-22 and ground.		
	j. Connect the audio oscillator to P1-22.		
	k. Apply +5-V dc signal to P1-38.		
	l. Set audio oscillator for 1000 Hz at 10 mV rms.		
	m. Note output level.	+10 ±1 dB mW.	If too high check U12B and associated circuits. If too low check U12C and associated circuits.
	n. Remove +5 V dc from P1-38.		
(Cont)	o. Connect the audio oscillator to P1-50.		

Table 1. Receive Audio, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	p. Adjust audio oscillator for 1000 Hz at 10 mV rms. q. Adjust R65 for 0-dB mW output level.		
6. Channel B, frequency response	a. Set front-panel MODE switch to ISB. b. Connect an audio oscillator to P1-50. c. Connect a 600-Ω load across CH B AUD OUT terminals. d. Connect an audio voltmeter across 600-Ω load. e. Adjust audio oscillator from 0 to 10 000 Hz with a constant 10-mV rms output. f. Note maximum level and frequencies at point 1 dB below maximum level.	Upper 1 dB frequency NLT 8000 Hz, NMT 12 kHz. Lower 1 dB frequency, NMT 250 Hz.	Check Q4, Q5, U4, U5, and associated circuit.
7. Channel B, total harmonic distortion	a. Set front-panel MODE switch to ISB. b. Connect an audio oscillator to P1-50. c. Connect a 600-Ω load across CH B AUD OUT terminals. d. Connect a distortion analyzer across 600-Ω load. e. Adjust audio oscillator to 300 Hz at 10-mV rms output. f. Measure total harmonic distortion using distortion analyzer. g. Repeat step f with audio oscillator set at:	NMT 3%.	Check bypass and dc blocking capacitors.
	1000 Hz 6000 Hz	NMT 0.5%. NMT 0.5%.	Same as step f.
8. Headphone amplifier, gain (Cont)	a. Set front-panel MODE switch to AM. b. Connect an audio oscillator to P1-35. c. Connect a distortion analyzer to P1-12. d. Adjust audio oscillator to 1000 Hz at 10-mV rms output. e. Set front panel PHONES level control to minimum.		

Table 1. Receive Audio, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
8. (Cont)	f. Set front-panel PHONES switch to CH A.		
	g. Note that a negligible audio output is present on the audio voltmeter.	NLT 30 dB below level of step i.	
	h. Set front-panel PHONES level control to maximum.		
	i. Note level on the audio voltmeter.	NLT +15 dB mW.	Check U13D, U7, and associated circuits.
	j. Set front-panel MODE switch to ISB.		
	k. Connect the audio oscillator to P1-50.		
	l. Adjust audio oscillator to 1000 Hz at 10-mV rms output.		
	m. Set front-panel PHONES switch to CH B.		
	n. Note level on the audio voltmeter.	NLT +15 dB mW.	Check U13B and associated circuits.
9. Headphone amplifier, frequency response	a. Set front-panel MODE switch to AM.		
	b. Connect an audio oscillator to P1-35.		
	c. Connect an audio voltmeter to P1-12.		
	d. Set front-panel PHONES level control to midrange.		
	e. Set front-panel PHONES switch to CH A.		
	f. Adjust audio oscillator from 0 to 10 000 Hz with a constant 10-mV rms output.		
	g. Note maximum output level and frequencies at point 1 dB below maximum level.	Upper 1-dB frequency NLT 6000 Hz. Lower 1-dB frequency, NLT 250 Hz.	Check U7 and associated circuits.
10. Headphone amplifier, total harmonic distortion	a. Set front-panel MODE switch to AM.		
	b. Connect an audio oscillator to P1-35.		
	c. Connect a distortion analyzer to P1-12.		
	d. Set front-panel PHONES switch to CH A.		
(Cont)	e. Adjust audio oscillator to 1000 Hz at 10-mV rms output.		

Table 1. Receive Audio, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
10. (Cont)	f. Adjust front-panel PHONES level control for 0 ±1 dB mW at P1-12.		
	g. Measure total harmonic distortion using distortion analyzer.	NMT 0.5%.	Check bypass and dc blocking capacitors.
11. Speaker amplifier, gain	a. Set front-panel MODE switch to AM.		
	b. Set front-panel SPKR switch to CH A.		
	c. Connect an audio oscillator to P1-35.		
	d. Connect an audio voltmeter between P1-19 and P1-17.		
	e. Adjust audio oscillator to 1000 Hz at 10-mV rms output.		
	f. Set SQUELCH control to off (fully ccw).		
	g. Increase front-panel AF GAIN control until distortion analyzer indicates 4 V rms.		
	h. Measure distortion using the distortion analyzer.	NMT 3%.	Check U8 and associated circuits.
	i. Set front-panel MODE switch to ISB.		
	j. Set front-panel SPKR switch to CH B.		
	k. Connect an audio oscillator to P1-50.		
	l. Adjust AF GAIN control until distortion analyzer indicates 4 V rms.		
	m. Measure distortion using the distortion analyzer.	NMT 3%.	Same as step h.
12. Speaker amplifier, frequency response	a. Set front-panel MODE switch to AM.		
	b. Set front-panel SPKR switch to CH A.		
	c. Connect an audio oscillator to P1-35.		
	d. Connect an audio voltmeter between P1-19 and P1-17.		
	e. Set SQUELCH control to off (fully ccw).		
	f. Adjust audio oscillator to 1000 Hz at 10-mV rms output.		
	g. Adjust AF GAIN control for 0.5 V rms as indicated on audio voltmeter.		
(Cont)	h. Adjust audio oscillator from 0 to 10 000 Hz.		

Table 1. Receive Audio, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
12. (Cont)	i. Note maximum output level and frequencies at point 1 dB below maximum level.	Upper 1 dB frequency, NLT 6000 Hz. Lower 1 dB frequency, NMT 250 Hz.	Check Q9, U8, and associated circuit.
13. Speaker amplifier, total harmonic distortion	a. Set front-panel MODE switch to AM.		
	b. Set front-panel SPKR switch to CH A.		
	c. Connect an audio oscillator to P1-35.		
	d. Connect a distortion analyzer between P1-19 and P1-17.		
	e. Set SQUELCH control to off (fully ccw).		
	f. Adjust audio oscillator to 1000 Hz at 10-mV rms outputs.		
	g. Adjust front-panel AF GAIN control until distortion analyzer indicates 4 V rms.		
	h. Measure total harmonic distortion using distortion analyzer.	NMT 3%.	Check bypass and dc blocking capacitors.
14. Squelch	a. Set front-panel MODE switch to AM.		
	b. Set front-panel SPKR switch to CH A.		
	c. Connect audio oscillator to P1-35.		
	d. Connect an audio voltmeter between P1-19 and P1-17.		
	e. Set front-panel SQUELCH control on (away from fully ccw).		
	f. Adjust the squelch threshold for minimum resistance (SQUELCH control near full ccw).		
	g. Set audio oscillator to 500 Hz at 10-mV rms output.		
	h. Set AF GAIN control for 0.5 V rms as indicated by audio voltmeter.		
	i. Slowly increase audio oscillator frequency until audio output is squelched. Note frequency.	Between 600 and 2500 Hz.	If too low, check Q7, U9B, and associated circuit. If too high, check Q6, U9A, and associated circuit.
(Cont)			

Table 1. Receive Audio, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
14. (Cont)	j. Return audio oscillator to 500 Hz and note that audio output returns.		
	k. Quickly switch from 500 to 3000 Hz audio and note time required for audio to squelch.	NMT 3 seconds.	Check Q7, U9B, U10, Q8, and associated circuit.
15. Channel A, performance monitor	a. Set front-panel MODE switch to AM.		
	b. Connect an audio oscillator to P1-35.		
	c. Connect a dvm to P1-2.		
	d. Set audio oscillator to 1000 Hz at 10-mV rms output.		
	e. Note dvm reading.	NMT 0.5 V dc.	Check U3A, Q10, and associated circuits.
	f. Decrease audio oscillator output by 10 dB.		
	g. Note dvm reading.	NLT +3.0 V dc.	Same as step e.
16. Channel B, performance monitor	a. Set front-panel MODE switch to ISB.		
	b. Connect an audio oscillator to P1-50.		
	c. Connect a dvm to P1-51.		
	d. Set audio oscillator to 1000 Hz at 10-mV rms output		
	e. Note dvm reading.	NMT 0.5 V dc.	Check U6B, Q11, and associated circuits.
	f. Decrease audio oscillator output by 10 dB.		
	g. Note dvm reading.	NLT +3.0 V dc.	Same as step e.
17. Channel A receive meter	a. Set front panel MODE switch to AM.		
	b. Connect an audio oscillator to P1-35.		
	c. Connect a 600-Ω load between CH A AUD OUT terminals.		
	d. Set front-panel METER switch to CH A AF (+3FS).		
	e. Set audio oscillator to 1000 Hz at 10-mV rms output.		
(Cont)	f. Note front-panel meter reading.	≅ 0 dB mW.	Adjust per paragraph 4.3. Check U3B and associated circuit.

Table 1. Receive Audio, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
17. (Cont)	g. Decrease audio oscillator output by 10 dB.		
	h. Note front-panel meter reading.	≅ -10 dB mW.	Same as step e.
18. Channel B, receive meter	a. Set front-panel MODE switch to ISB.		
	b. Connect an audio oscillator to P1-50.		
	c. Connect a 600-Ω load between CH B AUD OUT terminals.		
	d. Set front-panel METER switch to CH B AF (+3FS).		
	e. Set audio oscillator to 1000 Hz at 10-mV rms output.		
	f. Note front-panel meter reading.	≅ 0 dB mW.	Adjust per paragraph 4.4. Check U6A and associated circuit.
	g. Decrease audio oscillator output by 10 dB.		
	h. Note front-panel meter reading.	≅ -10 dB mW.	Same as step e.
19. Rf transmit	a. Set front-panel MODE switch to AM.		
	b. Connect an audio oscillator to P1-35.		
	c. Set front-panel METER switch to CH A AF (+3FS).		
	d. Set audio oscillator to 1000 Hz at 10-mV rms output.		
	e. Reference front-panel meter reading.	Reference.	
	f. Apply a +5-V dc signal at P1-41.		
	g. Note front-panel meter reading.	No deflection.	Check Q3, CR2, U11D, and associated circuit.
	h. Remove +5 V dc from P1-41.		
	i. Note front-panel meter reading.	Step e reference.	
	j. Set front-panel MODE switch to SSB/CW (receiver) or USB (receiver-exciter).		
	k. Remove audio oscillator from P1-35 and connect it to P1-34 (same 10-mV output).		
(Cont)	l. Reference front-panel meter reading.	Reference.	

Table 1. Receive Audio, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
19. (Cont)	m. Apply a +5-V dc signal at P1-41.		
	n. Note front-panel meter reading.	No deflection.	Check CR4, U11A, and associated circuit.
	o. Remove +5 V dc from P1-41.		
	p. Note front-panel meter reading.	Step l reference.	
	q. Apply +5-V dc signal at P1-10.		
	r. Remove audio oscillator from P1-34 and connect it to P1-7 (same 10-mV output).		
	s. Reference front-panel meter reading.	Reference.	
	t. Apply a +5-V dc signal at P1-41.		
	u. Note front-panel meter reading.	No deflection.	Check CR6, U11B, and associated circuit.
	v. Remove +5 V dc from P1-41.		
	w. Note front-panel meter reading.	Step s reference.	
	x. Remove +5 V dc from P1-10.		
	y. Apply +5 V dc from P1-38.		
	z. Remove audio oscillator from P1-7 and connect it to P1-5 (same 10-mV output).		
	aa. Reference front-panel meter reading.	Reference.	
	ab. Apply a +5-V dc signal at P1-41.		
	ac. Note front-panel meter reading.	Step aa reference.	Check for shorts or unauthorized modification.
	ad. Remove +5 V dc from P1-41.		
	ae. Note front-panel meter reading.	Step aa reference.	
	af. Remove +5 V dc from P1-38.		
	ag. Set front-panel MODE switch to ISB.		
	ah. Remove audio oscillator from P1-5 and connect it to P1-50 (same 10-mV output).		
	ai. Reference front-panel meter reading.	Reference.	
(Cont)	aj. Apply a +5-V dc signal at P1-41.		

Table 1. Receive Audio, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
19. (Cont)	ak. Note front-panel meter reading.	No deflection.	Check CR12, U12B, and associated circuit.
	al. Remove +5 V dc from P1-41.		
	am. Note front-panel meter reading.	Step ai reference.	
	an. Apply +5-V dc signal to P1-38.		
	ao. Remove audio oscillator from P1-50 and connect it to P1-22 (same 10-mV output).		
	ap. Reference front-panel meter reading.	Reference.	
	aq. Apply a +5 V dc signal at P1-41.		
	ar. Note front-panel meter reading.	Step ap reference.	Same as step ac.
	as. Remove +5 V dc from P1-41.		
	at. Note front-panel meter reading.	Step ap reference.	
20. Mute	a. Set front-panel MODE switch to AM.		
	b. Connect an audio oscillator to P1-35.		
	c. Set front-panel METER switch to CH A AF (+3FS).		
	d. Set audio oscillator to 1000 Hz at 10-mV rms output.		
	e. Reference front-panel meter reading.	Reference.	
	f. Apply a ground signal at P1-13.		
	g. Note front-panel meter reading.	No deflection.	Check CR1 and associated circuit.
	h. Remove ground from P1-13.		
	i. Note front-panel meter reading.	Step e reference.	
	j. Set front-panel MODE switch to SSB/CW (receiver) or USB (receiver-exciter).		
	k. Remove audio oscillator from P1-35 and connect it to P1-34 (same 10-mV output).		
	l. Reference front-panel meter reading.	Reference.	
	m. Apply a ground signal at P1-13.		
(Cont)	n. Note front-panel meter reading.	No deflection.	Check CR3 and associated circuit.

Table 1. Receive Audio. Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
20. (Cont)	o. Remove ground from P1-13.		
	p. Note front-panel meter reading.	Step l reference.	
	q. Apply +5-V dc signal at P1-10.		
	r. Remove audio oscillator from P1-34 and connect it to P1-7 (same 10-mV output).		
	s. Reference front-panel meter reading.	Reference.	
	t. Apply a ground signal at P1-13.		
	u. Note front-panel meter reading.	No deflection.	Check CR5 and associated circuit.
	v. Remove ground from P1-13.		
	w. Note front-panel meter reading.	Step s reference.	
	x. Remove +5 V dc from P1-10.		
	y. Apply +5-V dc signal to P1-38.		
	z. Remove audio oscillator from P1-7 and connect it to P1-5 (same 10-mV output).		
	aa. Reference front panel meter reading.	Reference.	
	ab. Apply a ground signal at P1-13.		
	ac. Note front-panel meter reading.	Step aa reference.	Check for shorts or unauthorized modifications.
	ad. Remove ground from P1-13.		
	ae. Note front-panel meter reading.	Step aa reference.	
	af. Remove +5 V dc from P1-38.		
	ag. Set front-panel MODE switch to ISB.		
	ah. Remove audio oscillator from P1-5 and connect it to P1-50 (same 10-mV output).		
	ai. Reference front-panel meter reading.	Reference.	
	aj. Apply a ground signal to P1-13.		
	ak. Note front-panel meter reading.	No deflection.	Check CR11 and associated circuit.
	al. Remove ground from P1-13.		
	am. Note front-panel meter reading.	Step ai reference.	
(Cont)	an. Apply +5-V dc signal to P1-38.		

Table 1. Receive Audio, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
20. (Cont)	ao. Remove audio oscillator from P1-50 and connect it to P1-22 (same 10-mV output).		
	ap. Reference front-panel meter reading.	Reference.	
	aq. Apply a ground signal at P1-13.		
	ar. Note front-panel meter reading.	Step ap reference.	Check for shorts or unauthorized modifications.
	as. Remove ground from P1-13.		
	at. Note front-panel meter reading.	Step ap reference.	
21. Af transmit	a. Set front-panel MODE switch to AM.		
	b. Set front-panel SPKR switch to CH A.		
	c. Connect an audio oscillator to P1-35.		
	d. Connect an audio voltmeter between P1-19 and P1-17.		
	e. Adjust audio oscillator to 1000 Hz at 10-mV rms output.		
	f. Set SQUELCH control to off (fully ccw).		
	g. Adjust front-panel AF GAIN control until audio voltmeter indicates 0.5 V rms.		
	h. Apply +5-V dc signal to P1-4.		
	i. Note audio voltmeter reading.	0.0 V rms.	Check Q12, Q9, CR21, and associated circuit.
	j. Remove +5 V dc from P1-4.		
	k. Note audio voltmeter reading.	0.5 V rms.	Same as step i.

4.2 Channel B Receive Line Amplifier Adjustment

Adjustment of CH B RCV LINE ADJ (R65) is as follows:

a. Perform test setup of table 1, test 1.
b. Set front-panel MODE switch to ISB.
c. Connect an audio oscillator to P1-50.
d. Set the audio oscillator to 1000 Hz at 10-mV rms output.
e. Connect a 600-Ω load across CH B AUD OUT terminals.
f. Connect an audio voltmeter across 600-Ω load.
g. Adjust CH B LINE ADJ (R65) for a 0-dB mW (+775-mV rms) reading on audio voltmeter.

4.3 Channel A Meter Adjustment

Adjustment of METER ADJ (R43) is as follows:

a. Perform channel A line amplifier adjustment per paragraph 4.1.
b. Perform test setup of table 1, test 1.
c. Set front-panel MODE switch to AM.
d. Connect an audio oscillator to P1-35.
e. Set front-panel METER switch to RCV-CH A AF (+3FS).
f. Set the audio oscillator to 1000 Hz at 10-mV rms output.
g. Adjust METER ADJ (R43) for a 0-dB mW reading on the front-panel meter.

4.4 Channel B Meter Adjustment

Adjustment of METER ADJ (R80) is as follows:

a. Perform channel B line amplifier adjustment per paragraph 4.2.
b. Perform test setup of table 1, test 1.
c. Set front-panel MODE switch to ISB.
d. Connect an audio oscillator to P1-50.
e. Set the audio oscillator to 1000 Hz at 10-mV rms output.
f. Set front-panel METER switch to RCV-CH B AF (+3FS).
g. Adjust METER ADJ (R80) for a 0-dB mW reading on the front-panel meter.

4.5 Squelch Adjustment

Perform squelch high-channel adjust (R131) as follows:

a. Perform test setup of table 1, test 1.
b. Set front-panel MODE switch to AM.
c. Set front-panel SPKR switch to CH A.
d. Connect an audio oscillator to P1-35.
e. Connect audio voltmeter to TP5 (green), voltmeter common to TP1 (brown).
f. Adjust audio oscillator (10-mV rms output) from 0 through 10 000 Hz and note maximum indication on audio voltmeter (frequency should be 600 ±100 Hz). Note amplitude.
g. Connect audio voltmeter to TP4 (yellow), voltmeter common to TP1 (brown).
h. Adjust audio oscillator (10-mV rms output) from 0 through 10 000 Hz and note maximum indication on audio voltmeter (frequency should be 2400 ±400 Hz).
i. Set audio oscillator to frequency (10-mV rms output) that gave the maximum indication in step h.
j. Adjust R131 to produce a level at TP4 (yellow), 12 dB below the amplitude noted in step f.

5. REPAIR

Repair of the receive audio card is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figure 8). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on the schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points to the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Receive audio	635-0748-001	REV J

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	RECEIVE AUDIO 635-0748-001		
CR1-CR21	SEMICOND DEVICE, 1N4454	353-3644-010	
C1-C4	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	
C5	CAPACITOR, FXD, CER DIEL, 0.1μF, 10%, 100V	913-5019-440	
C6	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	
C7	CAPACITOR, FXD, CER DIEL, 56pF, 10%, 200V (A2)	913-4003-000	
C7	CAPACITOR, FXD, DER DIEL, 18pF, 10%, 200V	913-5019-040	
C8	CAPACITOR, FXD, ELCTLT, 47μF, 20%, 20V	184-9102-190	
C9	CAPACITOR, FXD, CER DIEL, 56pF, 10%, 200V (A2)	913-4003-000	
C9	CAPACITOR, FXD, CER DIEL, 47pF, 10%, 200V	913-4002-000	
C10	CAPACITOR, FXD, CER DIEL, 0.1μF, 10%, 100V	913-5019-440	
C11	CAPACITOR, FXD, CER DIEL, 1μF, 20%, 50V	913-3279-270	
C12	CAPACITOR, FXD, ELCTLT, 47μF, 20%, 20V	184-9102-190	
C13	CAPACITOR, FXD, CER DIEL, 0.1μF, 10%, 100V	913-5019-440	
C14, C15	CAPACITOR, FXD, ELCTLT, 47μF, 20%, 20V	184-9102-190	
C16-C18	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	
C19	CAPACITOR, FXD, CER DIEL, 56pF, 10%, 200V (A2)	913-4003-000	
C19	CAPACITOR, FXD, CER DIEL, 18pF, 10%, 200V	913-5019-040	
C20	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 20V	184-9102-170	
C21	CAPACITOR, FXD, CER DIEL, 0.1μF, 10%, 100V	913-5019-440	
C22	CAPACITOR, FXD, CER DIEL, 1μF, 20%, 50V	913-3279-270	
C23	CAPACITOR, FXD, ELCTLT, 47μF, 20%, 20V	184-9102-190	
C24	CAPACITOR, FXD, CER DIEL, 0.1μF, 10%, 100V	913-5019-440	
C25-C27	CAPACITOR, FXD, ELCTLT, 47μF, 20%, 20V	184-9102-190	
C28	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	
C29	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 20V	184-9102-170	
C30, C31	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	
C32	CAPACITOR, FXD, CER DIEL, 56pF, 10%, 200V (A2)	913-4003-000	
C32	CAPACITOR, FXD, CER DIEL, 47pF, 10%, 200V	913-4002-000	
C33	CAPACITOR, FXD, CER DIEL, 0.1μF, 10%, 100V	913-5019-440	
C34, C35	CAPACITOR, FXD, ELCTLT, 47μF, 20%, 20V	184-9102-190	
C36	CAPACITOR, FXD, CER DIEL, 0.1μF, 10%, 100V	913-5019-440	
C37	CAPACITOR, FXD, CER DIEL, 0.47μF, 20%, 50V	913-3279-250	
C38	CAPACITOR, FXD, ELCTLT, 33μF, 20%, 25V	183-9102-260	
C39, C40	CAPACITOR, FXD, CER DIEL, 0.1μF, 10%, 100V	913-5019-440	
C41	CAPACITOR, FXD, ELCTLT, 220μF, -10%+75%, 20V	183-1277-200	
C42	NOT USED		
C43	CAPACITOR, FXD, ELCTLT, 4.7μF, 20%, 10V	184-9102-070	
C44	CAPACITOR, FXD, CER DIEL, 0.022μF, 10%, 50V	913-5019-240	
C45, C46	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	
C47, C48	CAPACITOR, FXD, ELCTLT, 4.7μF, 20%, 10V	184-9102-070	
C49	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V (A2)	913-5019-200	
C50, C51	CAPACITOR, FXD, CER DIEL, 330pF, 10%, 200V	913-4012-000	
C52	CAPACITOR, FXD, CER DIEL, 680pF, 10%, 200V	913-4016-000	
C53	CAPACITOR, FXD, ELCTLT, 4.7μF, 20%, 10V	184-9102-070	
C54	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	
C55, C56	CAPACITOR, FXD, ELCTLT, 4.7μF, 20%, 10V	184-9102-070	
C57	CAPACITOR, FXD, ELCTLT, 33μF, 20%, 25V	183-9102-260	
C58	CAPACITOR, FXD, CER DIEL, 3300pF, 10%, 100V	913-5019-140	
C59, C60	CAPACITOR, FXD, ELCTLT, 47μF, 20%, 20V	184-9102-190	
C61	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 20V	184-9102-170	
C62	CAPACITOR, FXD, ELCTLT, 4.7μF, 20%, 10V	184-9102-070	
C63	NOT USED		
C64, C65	CAPACITOR, FXD, ELCTLT, 47μF, 20%, 20V	184-9102-190	
C66, C67	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 20V	184-9102-170	
C68	CAPACITOR, FXD, CER DIEL, 100pF, 10%, 200V	913-4006-000	
C69-C72	CAPACITOR, FXD, ELCTLT, 47μF, 20%, 20V	184-9102-190	
Q1	TRANSISTOR, 2N2222A	352-0661-020	
Q2	TRANSISTOR, 2N2907A	352-0551-010	
Q3, Q4	TRANSISTOR, 2N2222A	352-0661-020	
Q5	TRANSISTOR, 2N2907A	352-0551-010	
Q6, Q7	TRANSISTOR, 2N2222A	352-0661-020	
Q8	TRANSISTOR, 2N2907A	352-0551-010	
Q9	TRANSISTOR, 2N4092	352-0759-020	
Q10, Q11	TRANSISTOR, 2N2222A	352-0661-020	
Q12	TRANSISTOR, 2N2608	352-0605-010	
R1	RESISTOR, FXD, CMPSN, 680Ω, 10%, 1/4W	745-0743-000	
R2	RESISTOR, FXD, CMPSN, 0.22MΩ, 10%, 1/4W	745-0833-000	
R3	RESISTOR, FXD, CMPSN, 0.47MΩ, 10%, 1/4W	745-0845-000	

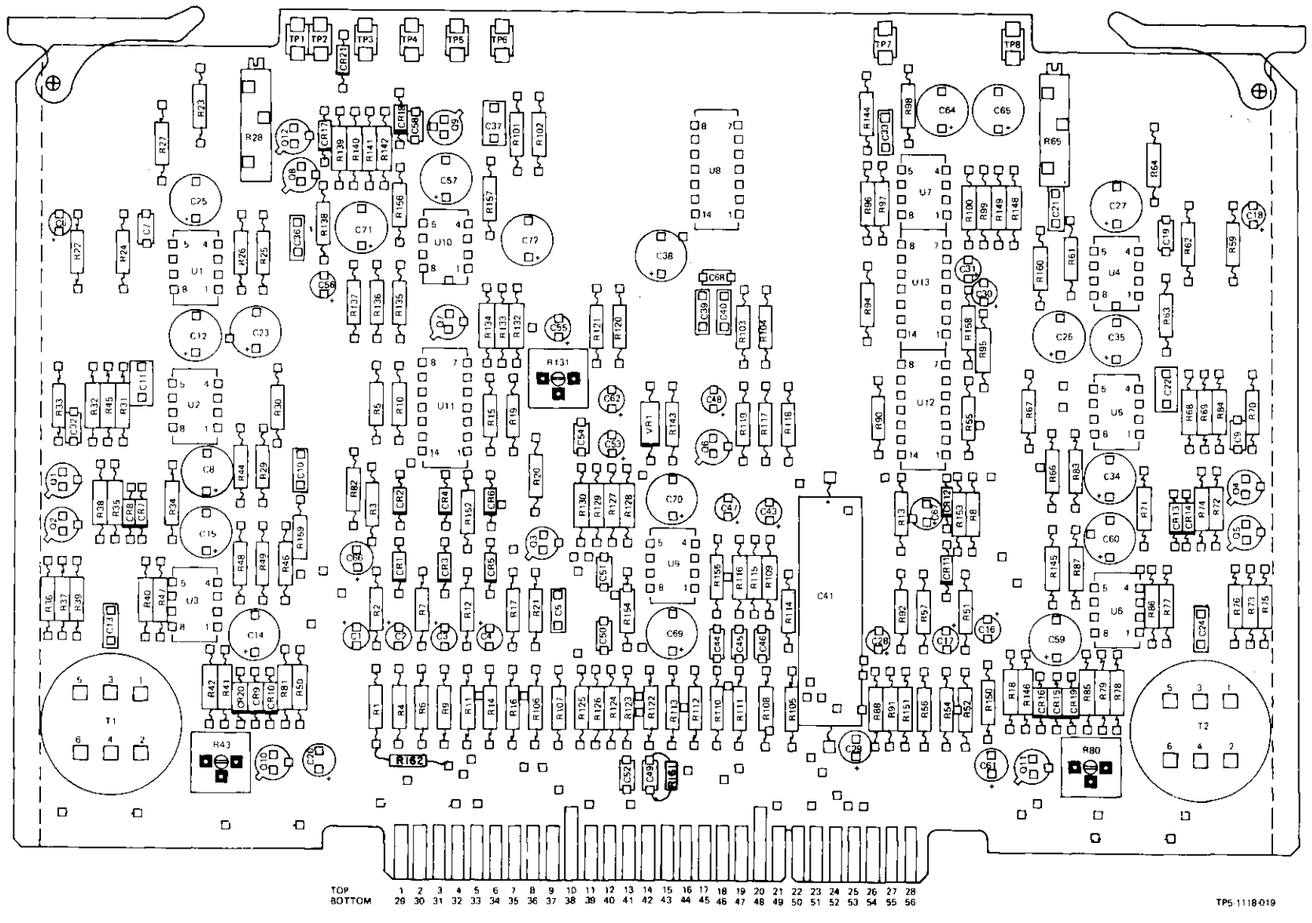
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
R4	RESISTOR, FXD, CMPSN, 0.01MΩ, 10%, 1/4W	745-0821-000	
R5	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R6	RESISTOR, FXD, CMPSN, 680Ω, 10%, 1/4W	745-0743-000	
R7	RESISTOR, FXD, CMPSN, 0.22MΩ, 10%, 1/4W	745-0833-000	
R8	RESISTOR, FXD, CMPSN, 0.47MΩ, 10%, 1/4W	745-0845-000	
R9	RESISTOR, FXD, CMPSN, 0.01MΩ, 10%, 1/4W	745-0821-000	
R10	RESISTOR, FXD, 1MΩ, 10%, 1/4W	745-0857-000	
R11	RESISTOR, FXD, CMPSN, 680Ω, 10%, 1/4W	745-0743-000	
R12	RESISTOR, FXD, CMPSN, 0.22MΩ, 10%, 1/4W	745-0833-000	
R13	RESISTOR, FXD, 1MΩ, 10%, 1/4W	745-0857-000	
R14	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R15	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R16	RESISTOR, FXD, CMPSN, 27kΩ, 10%, 1/4W	745-0800-000	
R17	RESISTOR, FXD, CMPSN, 0.22MΩ, 10%, 1/4W	745-0833-000	
R18	RESISTOR, FXD, CMPSN, 0.10Ω, 10%, 1/4W	745-0821-000	
R19	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R20	RESISTOR, FXD, CMPSN, 47kΩ, 10%, 1/4W	745-0809-000	
R21	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R22	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R23	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R24	RESISTOR, FXD, CMPSN, 0.15MΩ, 10%, 1/4W	745-0827-000	
R25	RESISTOR, FXD, CMPSN, 200Ω, 10%, 1/4W	745-0725-000	
R26	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R27	RESISTOR, FXD, CMPSN, 220Ω, 10%, 1/4W	745-0725-000	
R28	RESISTOR, VAR, 10kΩ, 10%, 3/4W	382-0012-290	
R29	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R30	RESISTOR, FXD, CMPSN, 68kΩ, 10%, 1/4W	745-0815-000	
R31, R32	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R33	RESISTOR, FXD, CMPSN, 68kΩ, 10%, 1/4W	745-0815-000	
R34	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R35	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R36, R37	RESISTOR, FXD, CMPSN, 47Ω, 10%, 1/4W	745-0701-000	
R38	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R39	RESISTOR, FXD, FILM, 140Ω, 1%, 1/8W	705-0955-000	
R40	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R41, R42	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R43	RESISTOR, VAR, 10kΩ, 20%, 1/2W	382-0038-070	
R44-R47	RESISTOR, FXD, CMPSN, 220Ω, 10%, 1/4W	745-0725-000	
R48	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R49	RESISTOR, FXD, CMPSN, 68kΩ, 10%, 1/4W	745-0815-000	
R50	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R51	RESISTOR, FXD, CMPSN, 0.22MΩ, 10%, 1/4W	745-0833-000	
R52	RESISTOR, FXD, CMPSN, 680Ω, 10%, 1/4W	745-0743-000	
R53	NOT USED		
R54	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R55	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R56	RESISTOR, FXD, CMPSN, 27kΩ, 10%, 1/4W	745-0800-000	
R57	RESISTOR, FXD, CMPSN, 0.22MΩ, 10%, 1/4W	745-0833-000	
R58	NOT USED		
R59	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R60	NOT USED		
R61	RESISTOR, FXD, CMPSN, 220Ω, 10%, 1/4W	745-0725-000	
R62	RESISTOR, FXD, CMPSN, 0.15MΩ, 10%, 1/4W	745-0827-000	
R63	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R64	RESISTOR, FXD, CMPSN, 220Ω, 10%, 1/4W	745-0725-000	
R65	RESISTOR, VAR, 10kΩ, 10%, 3/4W	382-0012-290	
R66	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R67	RESISTOR, FXD, CMPSN, 68kΩ, 10%, 1/4W	745-0815-000	
R68, R69	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R70	RESISTOR, FXD, CMPSN, 68kΩ, 10%, 1/4W	745-0815-000	
R71	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R72	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R73	RESISTOR, FXD, CMPSN, 47Ω, 10%, 1/4W	745-0701-000	
R74	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R75	RESISTOR, FXD, CMPSN, 47Ω, 10%, 1/4W	745-0701-000	
R76	RESISTOR, FXD, FILM, 140Ω, 1%, 1/8W	705-0955-000	
R77	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R78, R79	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R80	RESISTOR, VAR, 10kΩ, 20%, 1/2W	382-0038-070	
R81	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	

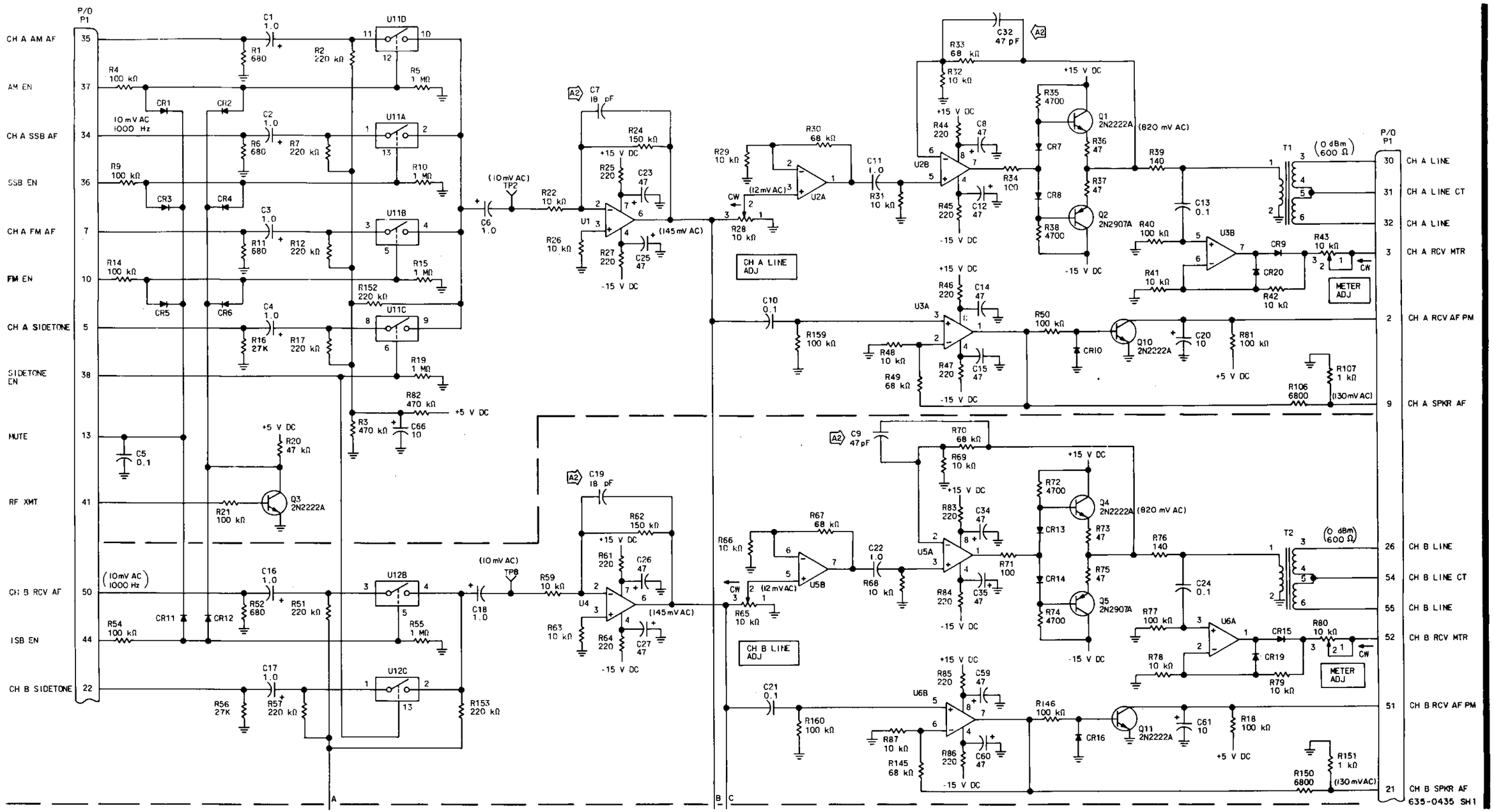
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
R82	RESISTOR, FXD, CMPSN, 0.47MΩ, 10%, 1/4W	745-0845-000	
R83-R86	RESISTOR, FXD, CMPSN, 220Ω, 10%, 1/4W	745-0725-000	
R87	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R88	RESISTOR, FXD, CMPSN, 0.22MΩ, 10%, 1/4W	745-0833-000	
R89	NOT USED		
R90	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R91	RESISTOR, FXD, CMPSN, 0.47MΩ, 10%, 1/4W	745-0845-000	
R92	RESISTOR, FXD, CMPSN, 0.22MΩ, 10%, 1/4W	745-0833-000	
R93	NOT USED		
R94	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R95, R96	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R97	RESISTOR, FXD, CMPSN, 68kΩ, 10%, 1/4W (A2)	745-0815-000	
R97	RESISTOR, FXD, FILM, 56.2kΩ, 1%, 1/8W	705-1080-000	
R98	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R99	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R100	RESISTOR, FXD, CMPSN, 0.15MΩ, 10%, 1/4W (A2)	745-0827-000	
R100	RESISTOR, FXD, FILM, 287kΩ, 1%, 1/8W	705-1114-000	
R101	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R102, R103	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R104	RESISTOR, FXD, CMPSN, 2.7Ω, 5%, 1/4W	745-4377-000	
R105	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R106	RESISTOR, FXD, CMPSN, 6.8kΩ, 10%, 1/4W	745-0779-000	
R107	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W	745-0749-000	
R108	RESISTOR, FXD, CMPSN, 6.8kΩ, 10%, 1/4W (A1)	745-0779-000	
R108	RESISTOR, FXD, CMPSN, 15kΩ, 10%, 1/4W	745-0791-000	
R109	RESISTOR, FXD, CMPSN, 510Ω, 5%, 1/4W	745-0738-000	
R110	RESISTOR, FXD, CMPSN, 27kΩ, 10%, 1/4W	745-0800-000	
R111	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W	745-0749-000	
R112	RESISTOR, FXD, CMPSN, 27kΩ, 10%, 1/4W	745-0800-000	
R113	RESISTOR, FXD, CMPSN, 510Ω, 5%, 1/4W	745-0738-000	
R114	RESISTOR, FXD, CMPSN, 13kΩ, 5%, 1/4W	745-0789-000	
R115	RESISTOR, FXD, CMPSN, 51kΩ, 5%, 1/4W (A2)	745-0810-000	
R115	RESISTOR, FXD, FILM, 51.1kΩ, 1%, 1/8W	705-1078-000	
R116	RESISTOR, FXD, CMPSN, 56kΩ, 10%, 1/4W (A2)	745-0812-000	
R116	RESISTOR, FXD, FILM, 56.2kΩ, 1%, 1/8W	705-1080-000	
R117	RESISTOR, FXD, FILM, 31.6kΩ, 1%, 1/8W	705-1068-000	
R118	RESISTOR, FXD, FILM, 5.76kΩ, 1%, 1/8W	705-3605-360	
R119	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R120	RESISTOR, FXD, CMPSN, 0.47MΩ, 10%, 1/4W	745-0845-000	
R121	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R122	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R123	RESISTOR, FXD, CMPSN, 75kΩ, 5%, 1/4W	745-0816-000	
R124	RESISTOR, FXD, CMPSN, 0.15MΩ, 10%, 1/4W	745-0827-000	
R125	RESISTOR, FXD, CMPSN, 510Ω, 5%, 1/4W	745-0738-000	
R126	RESISTOR, FXD, CMPSN, 0.15MΩ, 10%, 1/4W	745-0827-000	
R127	RESISTOR, FXD, CMPSN, 56kΩ, 10%, 1/4W (A2)	745-0812-000	
R127	RESISTOR, FXD, FILM, 56.2kΩ, 1%, 1/8W	705-1080-000	
R128	RESISTOR, FXD, CMPSN, 51kΩ, 5%, 1/4W (A2)	745-0810-000	
R128	RESISTOR, FXD, FILM, 51.1kΩ, 1%, 1/8W	745-1078-000	
R129	RESISTOR, FXD, CMPSN, 510Ω, 5%, 1/4W	745-0738-000	
R130	RESISTOR, FXD, CMPSN, 3.3kΩ, 10%, 1/4W	745-0767-000	
R131	RESISTOR, VAR, 10kΩ, 20%, 1/2W	382-0038-070	
R132	RESISTOR, FXD, FILM, 5.11kΩ, 1%, 1/8W	705-1030-000	
R133	RESISTOR, FXD, FILM, 31.6kΩ, 1%, 1/8W	705-1068-000	
R134	RESISTOR, FXD, FILM, 56.2kΩ, 1%, 1/8W (A1)	705-1080-000	
R134	RESISTOR, FXD, FILM, 24.9kΩ, 1%, 1/8W	705-1063-000	
R135	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R136	RESISTOR, FXD, CMPSN, 0.47MΩ, 10%, 1/4W	745-0845-000	
R137	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R138	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W	745-0749-000	
R139	RESISTOR, FXD, CMPSN, 47kΩ, 10%, 1/4W	745-0809-000	
R140	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R141	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R142	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R143	RESISTOR, FXD, CMPSN, 680Ω, 10%, 1/4W	745-0743-000	
R144	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W (A2)	745-0773-000	
R144	RESISTOR, FXD, CMPSN, 27kΩ, 10%, 1/4W	745-0800-000	
R145	RESISTOR, FXD, CMPSN, 68kΩ, 10%, 1/4W	745-0815-000	
R146	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R147	NOT USED		

Receive Audio, Schematic Diagram
Figure 8 (Sheet 2)



Receive Audio, Schematic Diagram
Figure 8 (Sheet 1 of 5)



Receive Audio, Schematic Diagram
Figure 8 (Sheet 3)

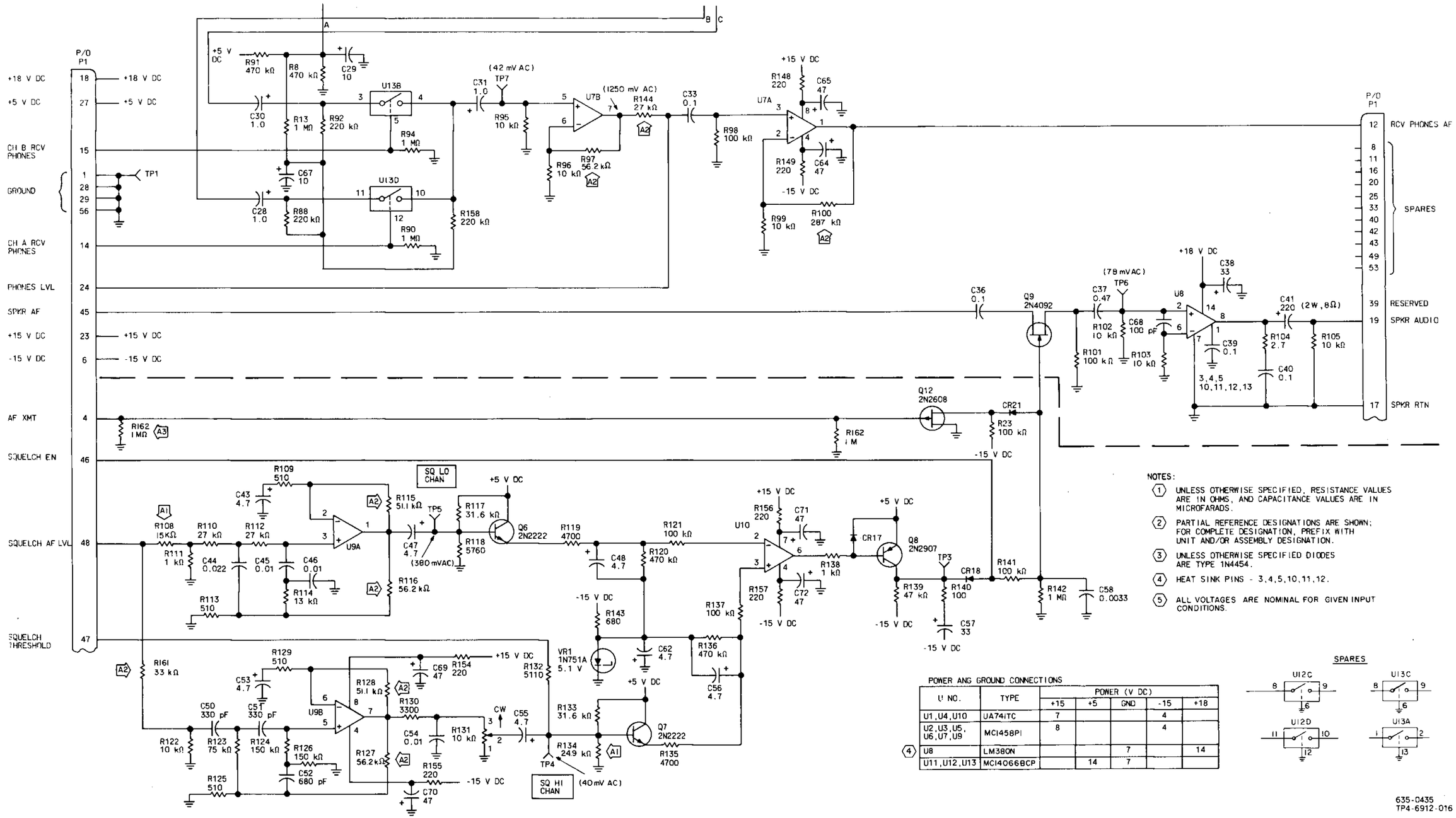
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
R148, R149	RESISTOR, FXD, CMPSN, 220Ω, 10%, 1/4W	745-0725-000	
R150	RESISTOR, FXD, CMPSN, 6.8kΩ, 10%, 1/4W	745-0779-000	
R151	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W	745-0749-000	
R152, R153	RESISTOR, FXD, CMPSN, 0.22MΩ, 10%, 1/4W	745-0833-000	
R154-R157	RESISTOR, FXD, CMPSN, 220Ω, 10%, 1/4W	745-0725-000	
R158	RESISTOR, FXD, CMPSN, 0.22MΩ, 10%, 1/4W	745-0833-000	
R159, R160	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R161	RESISTOR, FXD, CMPSN, 33kΩ, 10%, 1/4W (A2)	745-0803-000	
R162	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W (A3)	745-0857-000	
T1, T2	TRANSFORMER, AUD	677-0410-010	
TP1	JACK, TIP, BRN	360-0484-070	
TP2	JACK, TIP, RED	360-0484-020	
TP3	JACK, TIP, ORN	360-0484-050	
TP4	JACK, TIP, YEL	360-0484-060	
TP5	JACK, TIP, GRN	360-0484-040	
TP6	JACK, TIP, BLU	360-0484-080	
TP7	JACK, TIP, VIC	360-0484-090	
TP8	JACK, TIP, GRA	360-0484-100	
U1	INTEGRATED CKT, UA741TC	351-1110-020	
U2, U3	INTEGRATED CKT, MC1458P1	351-1071-070	
U4	INTEGRATED CKT, UA741TC	351-1110-020	
U5-U7	INTEGRATED CKT, MC1458P1	351-1071-070	
U8	INTEGRATED CKT, LM380N	351-1118-010	
U9	INTEGRATED CKT, MC1458P1	351-1071-070	
U10	INTEGRATED CKT, UA741TC	351-1110-020	
U11-U13	INTEGRATED CKT, MC14066BCP	351-8252-010	
VR1	SEMICOND DEVICE, 1N751A	353-2710-000	

MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Changed: R108 from 6800Ω to 15kΩ. R134 from 56.2kΩ to 24.9kΩ.	REV E and above
A2	Removed C49, 0.01 μF. Added R161, 33kΩ, in same location as C49 was removed. Changed: C7 from 56 pF to 18 pF C9 from 56 pF to 47 pF C19 from 56 pF to 18 pF C32 from 56 pF to 47 pF R97 from 68kΩ to 56.2kΩ R100 from 150kΩ to 287kΩ R115 from 51kΩ, 5% to 51.1kΩ, 1% R116 from 56kΩ, 10% to 56.2kΩ, 1% R127 from 56kΩ, 10%, to 56.2kΩ, 1% R128 from 51kΩ, 5% to 51.1kΩ, 1% R144 from 4700Ω to 27kΩ Added R161, 33kΩ	REV F and above
A3	Added R162, 1MΩ	REV H and above

Receive Audio, Schematic Diagram
Figure 8 (Sheet 4)



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, AND CAPACITANCE VALUES ARE IN MICROFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. UNLESS OTHERWISE SPECIFIED DIODES ARE TYPE 1N4454.
4. HEAT SINK PINS - 3,4,5,10,11,12.
5. ALL VOLTAGES ARE NOMINAL FOR GIVEN INPUT CONDITIONS.

POWER ANG GROUND CONNECTIONS

U NO.	TYPE	POWER (V DC)				
		+15	+5	GND	-15	+18
U1,U4,U10	UA741TC	7			4	
U2,U3,U5, U6,U7,U9	MC1458PI	8			4	
(4) U8	LM380N			7		14
U11,U12,U13	MC14066BCP		14	7		

SPARES

635-0435
TP4-6912-016

Receive Audio, Schematic Diagram
Figure 8 (Sheet 5)

Channel B IF (637-2647-( ))

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

523-0767965-003211
3rd Edition, 1 January 1979

1. DESCRIPTION

Channel B IF 637-2647-( ), shown in figure 1, is a 2-layer planar card with 56-pin, edge-on connector (2 layers, 28 pins each). The channel B if card has sub-miniax rf connectors for connecting to channel A if output (J1), channel A if input (J4), 450-kHz injection input (J5), and 450-kHz receive if input (J6).

The channel B if card consists of filter control, channel B if, channel B audio detector, and channel B AGC circuits.

The channel B if configuration differences are as follows:

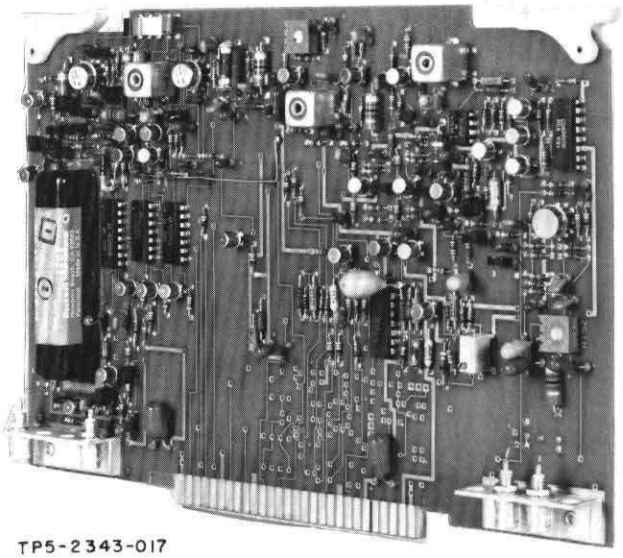
a. 637-2647 -001, FL2 has 2.75-kHz bandwidth (250 to 3000 Hz, LSB).
b. 637-2647-002, FL2 has 3.05-kHz bandwidth (250 to 3300 Hz, LSB).
c. 637-2647-003, FL2 has 3.10-kHz bandwidth (300 to 3400 Hz, LSB).

2. PRINCIPLES OF OPERATION

2.1 General

The channel B if receives the 450-kHz receive if input, filters the 450-kHz receive if signal, and provides the following:

a. 450-kHz receive if output
b. A product-detected channel B SSB audio output
c. AGC control signals



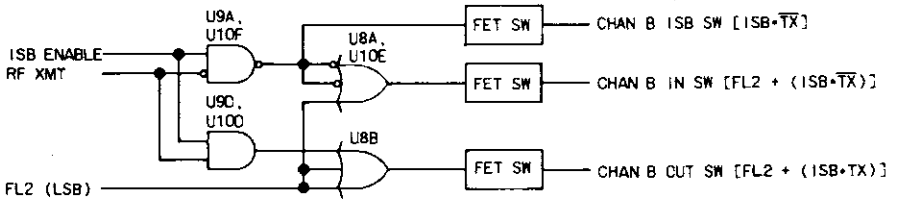
Channel B IF
Figure 1

2.2 Bandpass Filter Control Circuits (Refer to figure 2.)

The channel B if provides filter selection for receive if signals. Filter selection is initiated by the mode control signal, bandwidth control signal, and/or rf transmit signal. This means only that these signals are applied to the channel B if card to initiate filter selection; it does not reflect a mode of operation, selection of a bandwidth, or transmission of an rf signal.

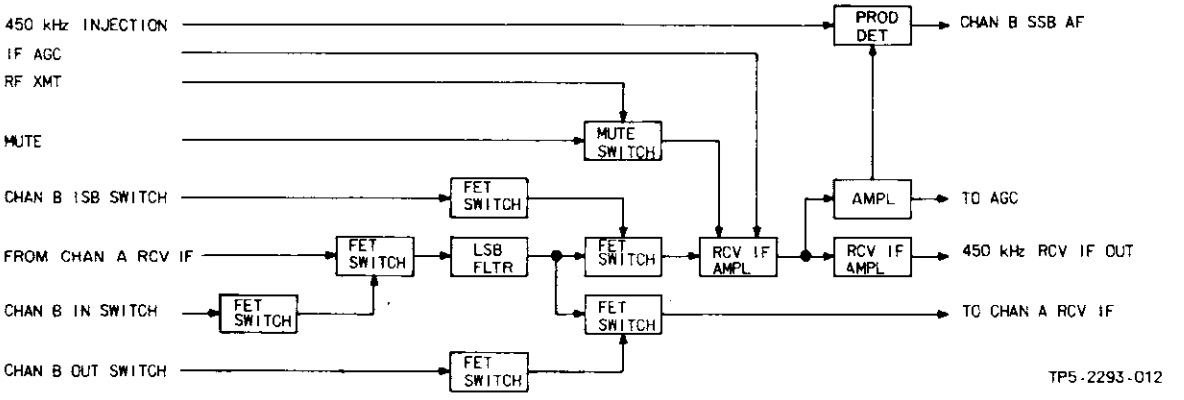
FL2 (LSB) is selected when an FL2 (LSB) enable signal or an ISB enable and rf transmit signals are applied to the channel B if card.

NOTICE: This section replaces second edition dated 1 June 1978.



TP5-2292-012

Channel B Filter and IF Control Circuits
Figure 2



TP5-2293-012

Channel B IF Circuits
Figure 3

2.3 Channel B IF Circuits (Refer to figure 3.)

The channel B if card receives 450-kHz receive if and supplies the 450-kHz if frequency to the LSB bandpass filter. After ISB mode or filter FL2 is selected, the 450-kHz if signal is supplied through the LSB bandpass filter. The output of the LSB bandpass filter is supplied as a channel B receive if output or is amplified and then applied as follows:

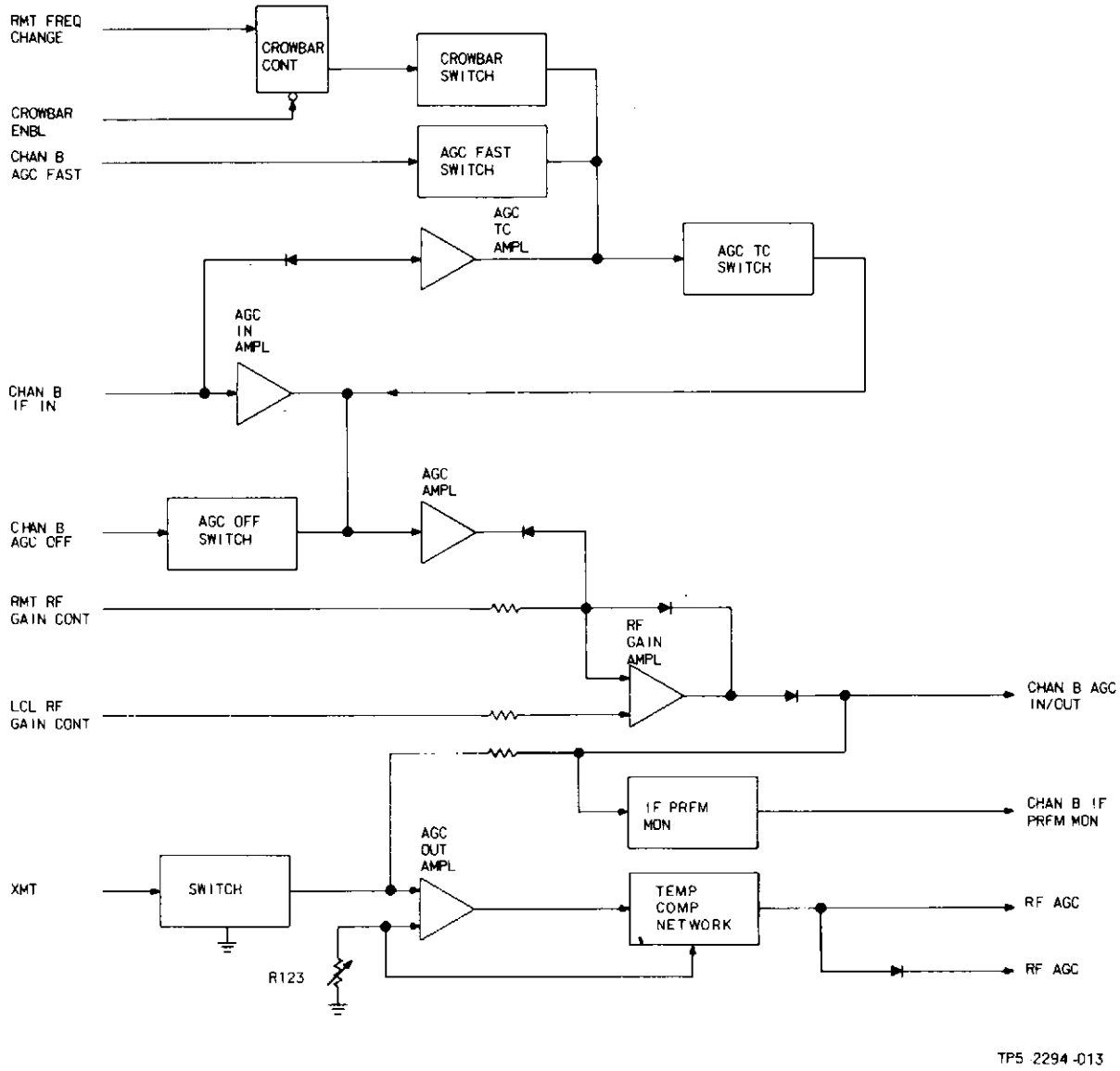
a. To AGC circuits
b. Through a receive if amplifier as an external 450-kHz receive if output
c. Through an amplifier to a channel B SSB audio product detector. The SSB product detector receives the receive if and a 450-kHz injection, and supplies a product-detected SSB audio output.

2.4 AGC Circuits (Refer to figure 4.)

Channel B if is received by the AGC input amplifier. The AGC input amplifier and associated AGC time constant switches develop the AGC level and decay time to be used by the receiver. The AGC level is amplified and applied through rf gain amplifier, and supplied to the if performance monitor and AGC output amplifier. The if AGC and rf AGC signals are developed and supplied to associated attenuator circuits.

With the AGC control in the SLOW position, only the AGC time constant amplifier and AGC time constant switch are enabled and establish a 1.0-second AGC decay time. (The AGC to amplifier and AGC to switch are enabled for all AGC functions.) With the AGC control in the FAST position, the AGC fast switch is enabled, reducing the time constant of the AGC circuits and establishing a 0.1-second AGC decay time. With the AGC control in the OFF position, the output of the AGC input amplifier is disabled and removed from the input of the AGC amplifier.

With the receiver in remote control and a crowbar enable applied, a remote frequency change enables the crowbar switch and reduces the AGC time constant, establishing the AGC decay time at about 2 milliseconds. The crowbar function is used for fast frequency hopping or scanning operation under processor control.
The gain of the rf gain amplifier is controlled by a local rf gain control signal. The dc voltage level



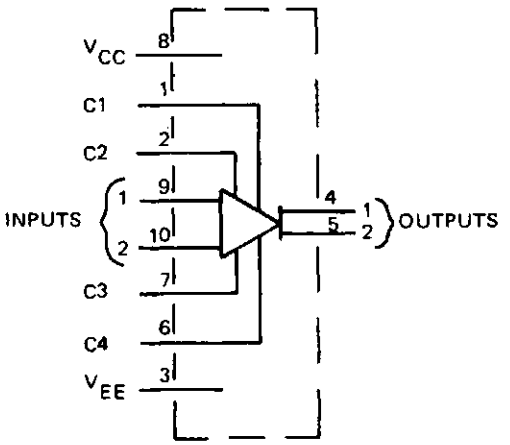
AGC Circuits
Figure 4

applied to the noninverting input of the rf gain amplifier establishes its gain. The remote rf gain control signal establishes the minimum gain output of the rf gain amplifier.

From the rf gain amplifier, the AGC output is supplied to channel B AGC out for use by other cards and to the channel B if performance monitor for channel B AGC indications. The rf gain amplifier output is supplied to AGC output amplifier and through AGC switch to the if/rf AGC outputs. R123 and temperature compensating network are used to keep the if/rf AGC outputs constant throughout the frequency/temperature range.

2.5 Differential Output Operational Amplifier 351-1050-030 (Refer to figure 5.)

The 351-1050-030 is a wide-band general-purpose operational amplifier which features both differential inputs and outputs. Open loop gain is adjustable with external feedback components.



CHARACTERISTICS

SUPPLY VOLTAGE: V_{CC} +8 V DC MAX., V_{EE} −8 V DC MAX.

INPUT DIFF VOLTAGE: ±8 V DC MAX.

INPUT COMMON MODE VOLTAGE: ±3.0 V PEAK

INPUT RESISTANCE: 2.0 M OHM TYPICAL

OUTPUT RESISTANCE: 50 OHM TYPICAL

OPEN LOOP GAIN: SINGLE ENDED– 750 V/V MIN, 1500 V/V TYPICAL; DIFFERENTIAL – 1500 V/V MIN,. 3000 V/V TYPICAL

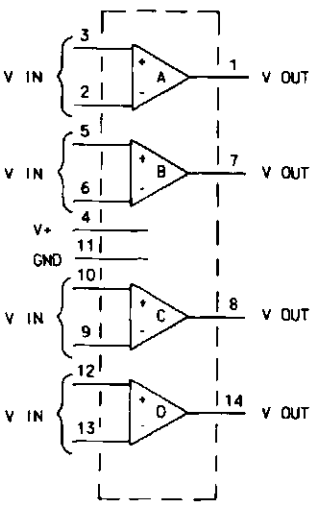
BANDWIDTH: OPEN LOOP–2.0 MHz TYPICAL; CLOSED LOOP –10.0 MHz TYPICAL

TP5-2282-011

Differential Output Operational Amplifier 351-1050-030
Figure 5

2.6 Quad Operational Amplifier 351-1141-030 (Refer to figure 6.)

The 351-1141-030 consists of four independent, high-gain, internally frequency-compensated operational amplifiers that are designed to operate from a single power supply over a wide range of voltages. Common applications include transducer amplifiers, dc gain blocks, and all conventional operational amplifier circuits.



CHARACTERISTICS

SUPPLY VOLTAGE (V+). 32 V DC MAX
INPUT DIFF VOLTAGE: 32 V DC MAX
INPUT COMMON MODE VOLTAGE: V+ (-1.5 V DC)
OUTPUT SHORT CIRCUIT DURATION:
CONTINUOUS (1)
VOLTAGE GAIN: 25 MIN

NOTE:
(1) SUPPLY VOLTAGE EQUAL TO OR LESS THAN 15 V.

TP5-2289-013

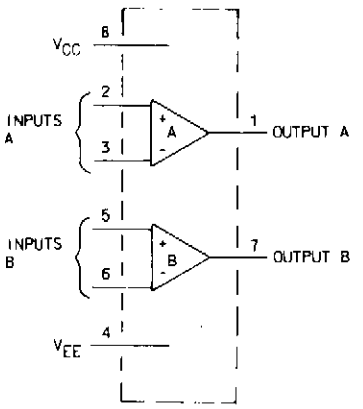
Quad Operational Amplifier 351-1141-030
Figure 6

2.7 Dual Operational Amplifier 351-1071-070 (Refer to figure 7.)

The 351-1071-070 consists of two operational amplifiers in one package, designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components.

2.8 Dual Monostable Multivibrator 351-8278-010 (Refer to figure 8.)

The 351-8278-010 is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X.

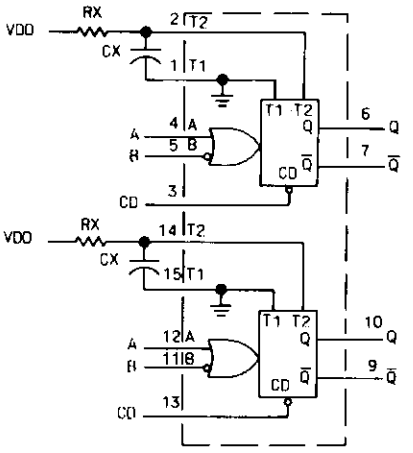


CHARACTERISTICS
SUPPLY VOLTAGE: V_{CC} +18 V DC MAX
V_{EE} -18 V DC MAX
INPUT DIFF VOLTAGE: ±30 V MAX
INPUT COMMON MODE VOLTAGE:
±15 V MAX (1)
OUTPUT SHORT CIRCUIT DURATION:
CONTINUOUS (2)
INPUT RESISTANCE: 300 kΩ MIN, 2.0 MΩ MAX
OUTPUT RESISTANCE: 75Ω TYPICAL
VOLTAGE GAIN: 15 MIN

NOTES:
(1) FOR SUPPLY VOLTAGE LESS THAN ±15.0 V, MAX INPUT VOLTAGE EQUAL TO SUPPLY VOLTAGE.
(2) SUPPLY VOLTAGE EQUAL TO OR LESS THAN 15 V.

TP5-2285-013

Dual Operational Amplifier 351-1071-070
Figure 7



NOTE:
RX AND CX ARE EXTERNAL COMPONENTS.

CHARACTERISTICS:
SUPPLY VOLTAGE (VDD): -0.5 TO +18 V DC.
INPUT VOLTAGE: EQUAL TO VDD, MAX.

CHARACTERISTIC		VDD		
		5.0 V DC	10.0 V DC	15.0 V DC
OUTPUT VOLTAGE	"0"	0.05 V DC MAX.	0.05 V DC MAX.	0.05 V DC MAX.
	"1"	4.95 V DC MIN.	9.95 V DC MIN.	14.95 V DC MIN
INPUT VOLTAGE	"0"	2.25 V DC MAX.	4.50 V DC MAX.	6.75 V DC MAX.
	"1"	2.75 V DC MIN.	5.50 V DC MIN.	8.25 V DC MIN.
EXTERNAL TIMING	RX	1000 Ω MIN	1000 Ω MIN.	1000 Ω MIN.
	CX	NO LIMITS	NO LIMITS	NO LIMITS

TP5-2290-013

Dual Monstable Multivibrator 351-8278-010
Figure 8

2.9 Balanced Modulator-Demodulator 351-0043-020 (Refer to figure 9.)

The 351-0043-020 is designed for use where the output voltage is a product of an input voltage (signal) and a switching function carrier. Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications.

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

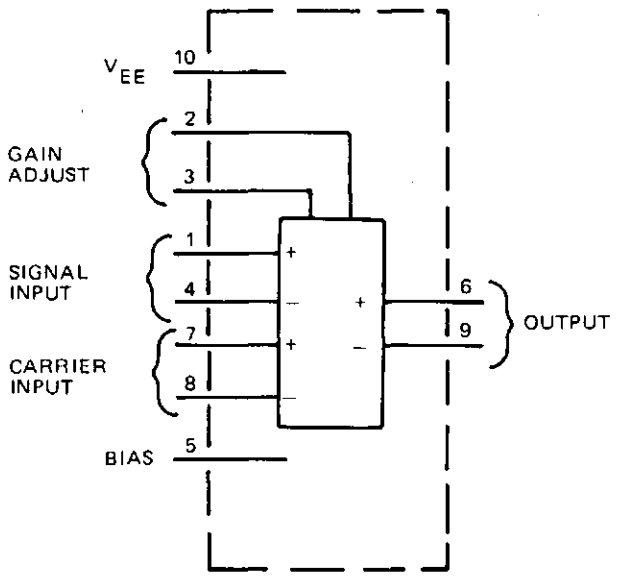
Test equipment and power sources required to test, troubleshoot, and repair the channel B if card are listed in the maintenance section of this instruction book.

3.2 Testing

Test procedures in table 1 check total performance of the channel B if card. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

Note

In emergencies, Channel B IF 637-2647-( ) can be replaced by Channel B IF 635-0902-( ). In this type of repair, use the test procedures given in table 1 to test Channel B IF 635-0902-( ).



CHARACTERISTICS

APPLIED VOLTAGE: 30 V DC MAX PIN–TO–IN.

DIFFERENTIAL INPUT VOLTAGE: ±5 V DC MAX

CARRIER SUPPRESSION: 65 dB TYPICAL AT 0.5 MHz; 50 dB TYPICAL AT 10 MHz.

TRANSADMITTANCE BANDWIDTH:
CARRIER INPUT–300 MHz TYPICAL;
SIGNAL INPUT–80 MHz TYPICAL

SINGLE-ENDED INPUT RESISTANCE (SIGNAL INPUT): 200 k OHM TYPICAL (AT 5.0 MHz)

SINGLE-ENDED INPUT RESISTANCE (SIGNAL INPUT): 40 k OHM TYPICAL (AT 10 MHz)

DIFFERENTIAL OUTPUT VOLTAGE SWING: 8.0 V P–P TYPICAL

TP5-2291-011

Balanced Modulator-Demodulator 351-0043-020
Figure 9

Table 1. Channel B IF, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of unit containing the channel B if that is to be tested.		
	b. Remove channel A or channel B if (as noted by particular test step). Install it on an extender card and place it in the unit.		
	c. Set unit LINE SELECTOR switch 115 V.		
	d. Connect unit to 115-V ac power source and set power on.		
	e. Measure dc voltages (on channel B if) between the following pins and ground (TP1, brown):		
	P1-23 and P1-51 P1-27 P1-6	+15 ±1.0 V dc +5 ±0.5 V dc -15 ±1.0 V dc	Check associated power supply.
	Note Unless otherwise specified, all rf signal levels applied at J2, receive if in, are referenced to 50 Ω.		
2. FL2 (LSB) filter and ISB enable	**Note** Channel B if card extended.		
	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to A.		
	b. Measure dc voltage at the following test points to ground (TP1, brown):		
	TP3 (orange) TP4 (yellow)	-9.5 ±1.0 V dc -9.5 ±1.0 V dc	Proceed to step m.
	c. Set front panel BANDWIDTH switch to LSB.		
	d. Measure dc voltage at the following test points to ground:		
	TP3 TP4	NMT 0.5 V dc NMT 0.5 V dc	Proceed to step n.
	e. Apply a +5.0-V dc signal at P1-41.		
	f. Measure dc voltage at the following test points to ground:		
	TP3 TP4	NMT 0.5 V dc -9.5 ±1.0 V dc.	Proceed to step n.
	g. Remove +5.0-V dc signal from P1-41.		
	h. Set front panel MODE switch to ISB.		
	i. Measure dc voltage at the following test points to ground:		
(Cont)	TP2 (red TP3 (orange)	NMT 0.5 V dc -9.5 ±1.0 V dc	Proceed to step o.

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	TP4 (yellow) TP5 (green)	NMT 0.5 V dc NMT 0.5 V dc	
	j. Apply a +5.0-V dc signal at P1-41.		
	k. Measure dc voltage at the following test points to ground.		
	TP2 TP3 TP4 TP5	-9.5 ±1.0 V dc NMT 0.5 V dc -9.5 ±1.0 V dc NLT +3.0 V dc	Proceed to step p.
	l. Remove P1-41 +5.0 V dc signal.		
	FL2 (LSB) ENABLE AND ISB ENABLE TESTING COMPLETE		
	TROUBLESHOOTING		
	m. Measure dc voltage at the following pins to ground:		
	P1-42	NMT 0.5 V dc	Check FL2 (LSB) enable input circuit.
	P1-44	NMT 0.5 V dc	Check ISB enable input circuit.
	P1-41	NMT 0.5 V dc	Check rf transmit input circuit.
		If all voltages in step m are normal, check U9, U10, U8, and Q28 (for TP3) or Q27 (for TP4).	
	n. Measure dc voltage at P1-42 to ground.	NLT +3.0 V dc. Check U8 and Q28 (for TP3) or Q27 (for TP4).	Check FL2 (LSB) enable input circuit.
	o. Measure dc voltage at the following pins to ground:		
	P1-42	NMT 0.5 V dc	Check FL2 (LSB) enable input circuit.
	P1-44	NLT +3.0 V dc	Check ISB enable input circuit.
	P1-41	NMT 0.5 V dc	Check rf transmit input circuit.
(Cont)		If all voltages in step o are normal, check U9 and Q30 (for TP2); U9, U10,	

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)		and U8 (for TP3 or TP4); and U10 (for TP5).	
	p. Measure dc voltage at the following pins to ground:		
	P1-42	NMT 0.5 V dc	Check FL2 (LSB) enable input circuit.
	P1-44	NLT +3.0 V dc	Check ISB enable input circuit.
	P1-41	NLT +3.0 V dc	Check rf transmit input circuit.
		If all voltages in step p are normal, check U9 and Q30 (for TP2); U9, U10, and U8 (for TP3 or TP4); and U10 (for TP5).	
3. 2.75-kHz LSB filter measurement	**Note** This test applies only to 2.75-kHz LSB filter (526-9956-010). Channel A if card extended.		
	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to LSB.		
	b. Set AGC switch to OFF.		
	c. Set receive input to channel A if (A8J2) at 9.4517 MHz.		
	d. Using an rf voltmeter, measure rf voltage at J1 (A8J4). Adjust receive input level and frequency for a 70-mV peak reading at J1 (A8J4).	Reference	
	e. Adjust input frequency up until rf voltage at J1 (A8J4) is 3 dB below level of step d. Note input frequency.	NLT 9.453 000 MHz	Check FL2, Q3, Q4, Q5, Q6, and associated circuits.
	f. Adjust input frequency down until rf voltage at J1 (A8J4) is 3 dB below level of step d. Note input frequency.	NMT 9.450 250 MHz	Check FL2, Q3, Q4, Q5, Q6, and associated circuits.
3A. 3.05-kHz LSB filter measurement (Cont)	**Note** This test applies only to 3.05-kHz LSB filter (526-9981-010). Channel A if card extended.		

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3A. (Cont)	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to LSB.		
	b. Set AGC switch to OFF.		
	c. Set receive input to channel A if (A8J2) at 9.4518 MHz.		
	d. Using an rf voltmeter, measure rf voltage at J1 (A8J4). Adjust receive input level and frequency for a 70-mV peak reading at J1 (A8J4).	Reference	
	e. Adjust input frequency up until rf voltage at J1 (A8J4) is 3 dB below level of step d. Note input frequency.	NLT 9.453 300 MHz	Check FL2, Q3, Q4, Q5, Q6, and associated circuits.
	f. Adjust input frequency down until rf voltage at J1 (A8J4) is 3 dB below level of step d. Note input frequency.	NMT 9.450 250 MHz	Check FL2, Q3, Q4, Q5, Q6, and associated circuits.
3B. 3.10-kHz LSB filter measurement	***Note***		
	This test applies only to 3.10-kHz LSB filter (526-9986-010).		
	Channel A if card extended.		
	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to LSB.		
	b. Set AGC switch to OFF.		
	c. Set receive input to channel A if (A8J2) at 9.4518 MHz.		
	d. Using an rf voltmeter, measure rf voltage at J1 (A8J4). Adjust receive input level and frequency for a 70-mV peak reading at J1 (A8J4).	Reference	
	e. Adjust input frequency up until rf voltage at J1 (A8J4) is 3 dB below level of step d. Note input frequency.	NLT 9.453 400 MHz	Check FL2, Q3, Q4, Q5, Q6, and associated circuits.
	f. Adjust input frequency down until rf voltage at J1 (A8J4) is 3 dB below level of step d. Note input frequency.	NMT 9.450 300 MHz	Check FL2, Q3, Q4, Q5, Q6, and associated circuits.
3C. 5.80-kHz LSB filter measurement	***Note***		
	This test applies only to 5.80-kHz LSB filter (526-9977-010).		
	Channel A if card extended.		
(Cont)	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to LSB.		

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3C. (Cont)	b. Set AGC switch to OFF.		
	c. Set receive input to channel A if (A8J2) at 9.4541 MHz.		
	d. Using an rf voltmeter, measure rf voltage at J1 (A8J4). Adjust receive input level and frequency for a 70-mV peak reading at J1 (A8J4).	Reference	
	e. Adjust input frequency up until rf voltage at J1 (A8J4) is 3 dB below level of step d. Note input frequency.	NLT 9.45 6 000 MHz	Check FL2, Q3, Q4, Q5, Q6, and associated circuits.
	f. Adjust input frequency down until rf voltage at J1 (A8J4) is 3 dB below level of step d. Note input frequency.	NMT 9.450 200 MHz	Check FL2, Q3, Q4, Q5, Q6, and associated circuits.
4. AGC attack and decay times	**Note** Channel A if card extended.		
	a. Set front panel MODE switch to ISB.		
	b. Set receive input to channel A if (A8J2) at 9.4517 MHz and 1 mV at output of switching device. Set the switching device for 0.25 s on and 2.5 s off. **Note** If a switching device is not available, one may be fabricated using figure 10.		
	c. Set front panel AGC switch to FAST.		
	d. Using an oscilloscope, measure AGC attack time at Q19-C (connect test lead to Q19-C and reinstall channel B if in unit). **Note** AGC attack time is the time interval from the first appearance of an rf burst to the point where the rf envelope stays within 6 dB of the final value.	NMT 5 ms	
	e. Set receive input to channel A if (A8J2) at 9.4517 MHz and 200 μV at output of switching device. Set the switching device to alternate between a 200-μV output and a 10-μV output.		

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
	f. Using an oscilloscope, measure AGC decay time at Q19-C. **Note** AGC decay time is the time interval from 200-μV to 10-μV transition and the point when the rf envelope reaches 70% of the final value.	75 to 200 ms	Check Q22, Q24, U4, and associated circuits.
	g. Repeat steps e and f with the front panel AGC switch at SLOW.	1 to 2 s	Check U4 and associated circuits.
5. 450-kHz injection frequency suppression	**Note** Channel A if card extended. a. Set receive input to channel A if (A8J2) at 9.4517 MHz and 1000 μV. b. Set AGC switch to FAST. c. Set front panel MODE switch to ISB.		
	d. Using a spectrum analyzer, measure the desired if out at J6 (CH B IF jack on rear panel).	Note level.	
	e. Measure the 450-kHz injection frequency leakage at the receive if out jack J6 (CH B IF jack on rear panel).	NLT 40 dB down from receive if above. **Note** It may be necessary to remove the receive input to locate the 450-kHz leakage. Measure it with the receive input applied.	Check U1, Q1, and associated circuits.
6. Receive audio distortion	**Note** Channel A if card extended. a. Set receive input to channel A if (A8J2) at 9.4517 MHz and 500 μV. b. Set front panel MODE switch to ISB.		
	c. Using an audio distortion analyzer, measure the audio distortion at RCV AF 600 Ω-B on rear panel (TB1-4, -6).	NMT 0.5%	Check U7, U2, U3, Q12, Q18, Q19, and associated circuits.

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
7. AGC range	**Note** Channel A if card extended.		
	a. Set front panel MODE switch to ISB.		
	b. Set AGC switch to FAST.		
	c. Set receive input to channel A if (A8J2) at 9.4517 MHz and 0 μV.		
	d. Connect dvm to P1-21 (TB1-9 on rear panel).		
	e. Increase receive input until dvm just begins to increase from 70 mV dc.	Note input level at this point. (Nominally 5μV rms)	
	f. Using an rf voltmeter, note rf level at J6 (CH B IF jack on rear panel).	Reference	
	g. Increase receive input 80 dB higher than the input level notes in step e.		
	h. Note the rf level at J6 (CH B IF jack on rear panel) and that no sign of an overload exists on Q19-C.	NMT 6 dB above that noted in step f. No overload on Q19-C.	Check U2, U3, and associated circuits.
8. Remote rf gain	**Note** This test applies only to unit with a remote control connected. Channel A if card extended.		
	a. Set receive input to channel A if (A8J2) at 9.4517 MHz and 5 μV.		
	b. Set front panel CONT switch to REM.		
	c. Set remote control MODE switch to ISB.	Reference if output level at J6 (CH B IF jack on rear panel).	
	d. Set remote control AGC switch off.		
	e. Adjust remote control RF GAIN control full counterclockwise. Increase receive input at A8J2 until if output level equals reference of step c.	Total attenuation over RF GAIN control range minimum 80 dB	Check U4 and associated circuits.
	f. Set receive input for 60 dB above 5-μV input. Adjust remote control RF GAIN control until if output level equals reference of step c.		
	g. Note the input at P1-11 (A8P1-11).	-5.0 ±0.1 V dc	Same as step e.
	h. Set front panel CONT switch to LCL.		

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont).

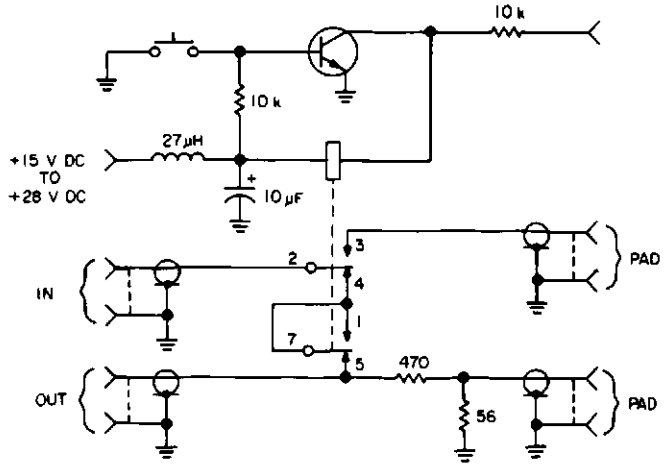
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
9. Local rf gain	**Note** Channel A if card extended.		
	a. Set receive input to channel A if (A8J2) at 9.4517 MHz and 5 μV.		
	b. Set front panel MODE switch to ISB.	Reference if output level at J6 (CH B IF jack on rear panel).	
	c. Set front panel AGC switch to OFF.		
	d. Adjust front panel RF GAIN control full counterclockwise. Increase receive input at A8J2 until if output level equals reference of step b.	Total attenuation over RF GAIN control range minimum 80 dB	Check U4 and associated circuits.
	e. Set receive input for 60 dB above 5-μV input. Adjust RF GAIN control until if output level equals reference of step b.		
	f. Note the input at P1-39 (A8P1-39).	+2.8 ±0.3 V dc	Same as step d.
10. AGC in/out	**Note** Channel A if card extended.		
	a. Set the front panel MODE switch to ISB.		
	b. Set front panel AGC switch to FAST.		
	c. Set receive input to channel A if (A8J2) at 9.4517 MHz and 5 μV.		
	d. Check the AGC in/out voltage at P1-21 (TB1-9 on rear panel) with this input applied.	≅70 mV dc	Check U4B and associated circuits.
	e. Increase the receive input to channel A if (A8J2) by 80 dB.		
	f. Check the AGC in/out voltage at P1-21 (TB1-9 on rear panel) with this input applied.	7.8 ±0.8 V dc	Same as step e.
11. Rf AGC	**Note** Channel A if card extended.		
	a. Set the front panel MODE switch to ISB.		
	b. Set front panel AGC switch to FAST.		
(Cont)	c. Set receive input to channel A if (A8J2) at 9.4517 MHz and 5 μV.	Reference	

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
11. (Cont)	d. Using a dvm, monitor the rf AGC voltage at P1-18 (A8P1-18).		
	e. Adjust front panel RF GAIN control for 0 V dc at P1-18 (A8P1-18).		
	f. Note the rf AGC voltage while slowly increasing the receive input to 80 dB above level in step c.	Rf AGC increases at a constant rate from 0 to 3 V dc. (60-dB point = NLT 3.0 V dc)	Check Q20, U4A, U4B, and associated circuits.
12. Mute	**Note** Channel A if card extended.		
	a. Set the front panel MODE switch to ISB.		
	b. Set receive input to channel A if (A8J2) at 9.4517 MHz and 50 μV.		
	c. Using an rf voltmeter, monitor the if output at J6 (CH B IF jack on rear panel).	Output signal is present.	Check U2, U3, and associated circuits.
	d. Apply a ground at P1-13 (A8P1-13).	Output signal is muted.	Check Q8 thru Q11 and associated circuits.
	e. Remove P1-13 (A8P1-13) ground.	Output signal is restored.	
13. Performance monitor	**Note** Channel A if card and parallel input card extended.		
	a. Set the front panel MODE switch to ISB.		
	b. Set receive input to channel A if (A8J2) at 9.4517 MHz and 50 μV.		
	c. Using a dvm, measure the dc voltage at P1-2 (A11P1-18).	0.5 ±0.5 V dc	Check Q25 and associated circuits.
	d. Remove receive input and measure the dc voltage at P1-2 (A11P1-18).	±4.5 ±0.5 V dc	Same as step c.
14. Crowbar enable	**Note** Channel B if card extended.		
	a. Set the front panel CONT switch to REM.		
	b. Apply +5 V dc to P1-37.		
(Cont)	c. Using an oscilloscope, monitor the waveform at U6-7.	NLT +3.0 V dc	Check U6 and associated circuits.

Table 1. Channel B IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
14. (Cont)	d. Note dc level and duration of U6-7 pulse while slowly changing the remote control frequency settings.	0.5±0.5 V dc for 20 ±10 ms between each frequency change.	Same as step b.
	e. Using an oscilloscope, monitor the waveform at P1-18.	During the logic 0 pulse, waveform at P1-18 shall be 0.5 ±0.5 V dc	Check Q24 and associated circuits.
	f. Remove +5 V dc from P1-37.		
	g. Set the front panel CONT switch to LCL.		
15. Sensitivity	**Note** Channel A if card extended.		
	a. Set the front panel MODE switch to ISB.		
	b. Set AGC switch to OFF.		
	c. Using an audio voltmeter, monitor the audio at P1-34 (A6TP8) (with no receive input).		
	d. Set receive input to channel A if (A8J2) at 9.4517 MHz.		
	e. Adjust receive input for +10 dB (s+n)/n at P1-34 (A6TP8).		
	f. Note the receive input level.	NMT 1 μV rms (into 50-Ω, 2-μV rms open circuit)	Check U2, U3, and associated circuits.
16. If output	**Note** Channel A if card extended.		
	a. Set the front panel MODE switch to ISB.		
	b. Set receive input to channel A if (A8J2) at 9.4517 MHz and 15 μV.		
	c. Set front panel AGC switch to FAST.		
	d. Using an rf voltmeter, measure the receive if output at J6 (CH B IF jack on rear panel).	27 ±10 mV rms.	Check U2, U3, and associated circuits.



TPA-1345-013

AGC Switching Device
Figure 10

4. ALIGNMENT/ADJUSTMENT

4.1 Filter Gain Adjustments (Selection of R29 and R41)

a. Set front panel MODE switch to ISB. Set AGC switch to FAST.
b. Connect receive input of 9.4517 MHz to channel A if J2.

Note

Select values of R29 and R41 only if Q3, Q5, and/or FL2 circuits have been repaired.

c. Set receive signal to 50 µV (9.4517 MHz). Find a passband reponse minimum between 9.4507 and 9.4511 MHz at J1. Measure voltage gain between J4 and J1. Should be 8.2 ±2.0 dB. Select values of R29 and R41 (200 thru 1000 Ω) to give a voltage gain of 8.2 ±2.0 dB.

4.2 Receive Gain Adjustment (Adjustment of L5, L7, R68, and R123)

a. Set front panel MODE switch to ISB. Adjust R68 for minimum gain (full ccw). Adjust receive input until channel B if output (measured at J6) indicates about 20 mV rms.
b. Adjust L5 and L7 for a peak channel B if output. Decrease the receive input as necessary to maintain channel B if output at 20 mV rms.
c. Repeat step b until no further increase in channel B if output is possible.
d. Set the receive input to 5 µV (9.4517 MHz) and adjust R68 for +70 ±5-mV dc AGC voltage (measured at P1-21).
e. Increase receive input to 5.0 mV (9.4517 MHz) and adjust R123 until AGC voltage (measured at P1-21) equals +5.0 ±0.1 V dc.
f. Repeat steps d and e until no further improvement is possible.

4.3 SSB Output Level Adjustment (Adjustment of R152)

a. Set front panel MODE switch to ISB.
b. Set receive input for 15.0 μV (9.4517 MHz) and adjust R152 for 10 ±0.5-mV rms audio output (measured at P1-34).

5. REPAIR

Repair of the channel B if card is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

This paragraph assists in identification, requisition, and issuance of parts and in maintenance of equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figures 11 and 12.) The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

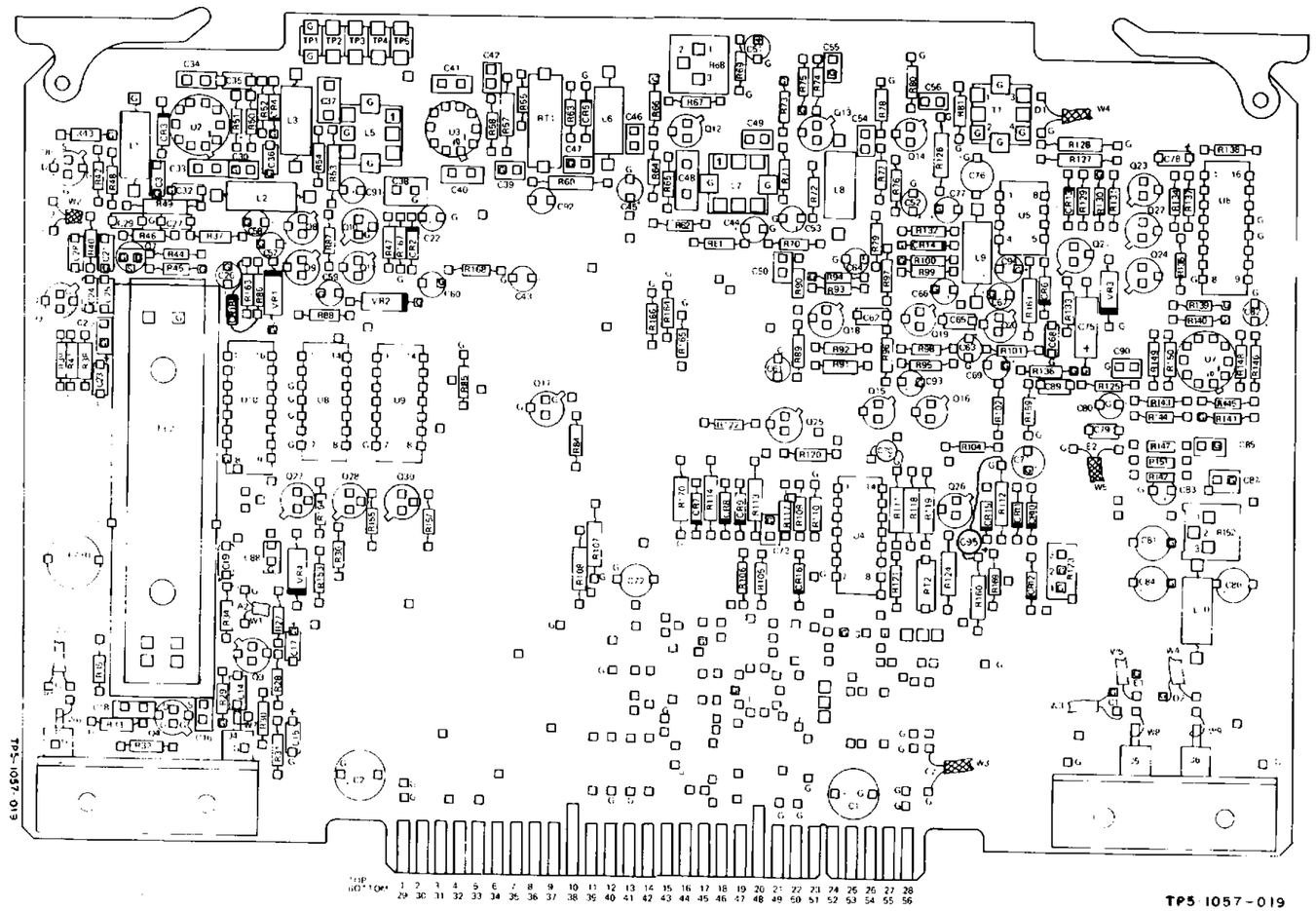
Use reference designator indicated on the schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description is listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Channel B if	637-2647-001	REV U
Channel B if	637-2647-002	REV U
Channel B if	637-2647-003	REV U
Channel B if	637-2647-004	*

* Not covered in this printing.



Channel B IF, Through REV T, Schematic Diagram
Figure 11 (Sheet 1 of 5)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
	CHANNEL B IF A7	637-2647-001	A
	CHANNEL B IF A7	637-2647-002	B
	CHANNEL B IF A7	637-2647-003	C
CR1	NOT USED		
CR2	SEMICOND DEVICE 1N4454	353-3644-010	
CR3-CR5	SEMICOND DEVICE 1N5767	922-6119-010	
CR6-CR14	SEMICOND DEVICE 1N4454	353-3644-010	
CR15	SEMICOND DEVICE 1N816 (A2)	353-2564-000	
CR15	SEMICOND DEVICE 1N5767	922-6119-010	
CR16	SEMICOND DEVICE 1N4454	353-3644-010	
CR17	NOT USED		
CR18	SEMICOND DEVICE 1N4454 (A2)	353-3644-010	
C1,C2	CAPACITOR,FXD ELCTLT, 47UF, 20%, 20V	184-9102-630	
C3-C13	NOT USED		
C14	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C15	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V (A1)	913-5019-200	
C15	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C16	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C17	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V (A4)	913-5019-200	
C17	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C18	CAPACITOR,FXD MICA DIEL, 15PF, PORM 0.5PF, 300V (A4)	912-4141-130	
C18	CAPACITOR,FXD MICA DIEL, 22PF, PORM 0.5PF, 300V	912-4141-030	
C19	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V (A2)	913-5019-200	
C19	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C20	CAPACITOR,FXD MICA DIEL, 20PF, PORM 0.5PF, 100V	912-4141-150	
C21	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C22	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C23	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V (A2)	913-5019-200	
C23	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C24,C25	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C26	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C27-C29	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C30	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C31,C32	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C33,C34	CAPACITOR,FXD MICA DIEL, 4PF, PORM 0.5PF, 300V	912-4141-080	
C35,C36	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C37	CAPACITOR,FXD CER DIEL, 1200PF, 5%, 100V	913-3281-290	
C38	CAPACITOR,FXD MICA DIEL, 400PF, 5%, 50V	912-4141-520	
C39	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C40,C41	CAPACITOR,FXD MICA DIEL, 4PF, PORM 0.5PF, 300V	912-4141-080	
C42	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C43-C45	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A7)	184-9102-290	
C43-C45	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C46,C47	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C48	CAPACITOR,FXD CER DIEL, 5600PF, 5%, 100V	913-3281-380	
C49,C50	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C51	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A7)	184-9102-290	
C51	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C52	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V (A4)	184-9102-350	
C52	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C53	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A4)	184-9102-290	
C53	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C54-C56	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C57-C61	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A7)	184-9102-290	
C57-C61	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C62	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C63	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V (A4)	184-9102-350	
C63	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C64	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A7)	184-9102-290	
C64	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C65	CAPACITOR,FXD CER DIEL, 470PF, 10%, 200V	913-4014-000	
C66	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A7)	184-9102-290	
C66	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C67	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A7)	184-9102-290	
C67	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C68	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C69	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A7)	184-9102-290	
C69	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C70	CAPACITOR,FXD ELCTLT, 47UF, 20%, 20V	184-9102-630	
C71	CAPACITOR,FXD ELCTLT, 22UF, 20%, 15V	184-9102-140	
C72	CAPACITOR,FXD ELCTLT, 47UF, 20%, 6V	184-9102-470	
C73	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C74	NOT USED		
C75	CAPACITOR,FXD ELCTLT, 4.7UF, 10%, 10V (A1)	184-9086-140	
C75	CAPACITOR,FXD ELCTLT, 2.2UF, 10%, 20V	184-9086-430	
C76	CAPACITOR,FXD ELCTLT, 6.8UF, 20%, 6V	184-9102-450	
C77	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A7)	184-9102-290	
C77	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C78	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A7)	184-9102-290	
C78	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C79	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C80	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A7)	184-9102-290	
C80	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C81	CAPACITOR,FXD ELCTLT, 22UF, 20%, 10V	184-9102-520	
C82,C83	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A7)	184-9102-290	
C82,C83	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C84	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-610	
C85	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V (A4)	913-3279-110	

PARTS LIST (CONT)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
C85	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C86	CAPACITOR,FXD ELCTLT, 6.8UF, 20%, 25V	184-9102-670	
C87	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V (A4)	913-3279-110	
C87	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C88	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-180	
C89	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C90	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C91	CAPACITOR,FXD ELCTLT, 0.47UF, 20%, 35V	184-9102-330	
C92	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C93	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V (A4)	184-9102-350	
C93	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C94	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C95	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V (A6)	184-9102-660	
C95	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
FL1	NOT USED		
FL2	FILTER,LSB,2.75 KHZ	526-9956-010	A
FL2	FILTER,LSB,3.05 KHZ	526-9981-010	B
FL2	FILTER,LSB,3.10 KHZ	526-9986-010	C
J1	CONNECTOR,RCPT ELEC	357-7207-100	
J2,J3	NOT USED		
J4-J6	CONNECTOR,RCPT ELEC	357-7207-100	
L1	COIL,RF 2700UH	240-2715-540	
L2,L3	COIL,RF 1000UH	240-2715-490	
L4	NOT USED		
L5	INDUCTOR,RF	242-0441-010	
L6	COIL,RF 1000UH	240-2715-490	
L7	INDUCTOR,RF	242-0441-020	
L8	COIL,RF 1000UH	240-2715-490	
L9	COIL,RF 8200UH	240-2715-600	
L10	COIL,RF 1000UH	240-2715-490	
Q1,Q2	NOT USED		
Q3-Q6	TRANSISTOR 2N4416	352-0756-010	
Q7	TRANSISTOR SPF557	352-1068-010	
Q8	TRANSISTOR 2N2222A	352-0661-020	
Q9	TRANSISTOR 2N2907A	352-0551-010	
Q10	TRANSISTOR 2N2222A	352-0661-020	
Q11	TRANSISTOR 2N2907A	352-0551-010	
Q12-Q14	TRANSISTOR 2N2222A	352-0661-020	
Q15	TRANSISTOR 2N2907A	352-0551-010	
Q16	TRANSISTOR 2N2222A	352-0661-020	
Q17	TRANSISTOR 2N2608	352-0605-010	
Q18,Q19	TRANSISTOR 2N2222A	352-0661-020	
Q20	TRANSISTOR 2N2907A	352-0551-010	
Q21	TRANSISTOR 2N2222A	352-0661-020	
Q22,Q23	TRANSISTOR 2N2907A	352-0551-010	
Q24	TRANSISTOR 2N2608	352-0605-010	
Q25,Q26	TRANSISTOR 2N2222A	352-0661-020	
Q27,Q28	TRANSISTOR 2N2608	352-0605-010	
Q29	NOT USED		
Q30	TRANSISTOR 2N2608	352-0605-010	
RT1	RESISTOR,THRM 3K, 10%, 1W	714-1715-000	
RT2	RESISTOR,THRM 100K, 10%, 0.5W	714-1736-000	
R1-R26	NOT USED		
R27	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R28	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R29	RESISTOR,FXD CMPSN, 560 OHMS, 10%, 1/8W (A4)	745-2332-000	
R29	RESISTOR,FXD CMPSN, 470 OHMS, 10%, 1/8W	745-2329-000	
R30	RESISTOR,FXD CMPSN, 560 OHMS, 10%, 1/8W (A2)	745-2332-000	
R30	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R31	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W (A1)	745-2304-000	
R31	RESISTOR,FXD CMPSN, 470 OHMS, 10%, 1/8W	745-2329-000	
R32	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R33	RESISTOR,FXD CMPSN, 560 OHMS, 10%, 1/8W	745-2332-000	
R34	RESISTOR,FXD FILM, 5.11K, 1%, 1/8W	705-1030-000	
R35	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W (A2)	745-2304-000	
R35	RESISTOR,FXD CMPSN, 470 OHMS, 10%, 1/8W	745-2329-000	
R36,R37	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R38	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R39	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R40	RESISTOR,FXD FILM, 5.11K, 1%, 1/8W	705-1030-000	
R41	RESISTOR,FXD,CMPSN, 200 THRU 680 OHMS,5%,1/8W (A4)	637-2529-001	
R41	RESISTOR,FXD CMPSN, 470 OHMS, 10%, 1/8W	745-2329-000	
R42	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R43	RESISTOR,FXD,CMPSN, 200 THRU 680 OHMS,5%,1/8W (A2)	637-2529-001	
R43	RESISTOR,FXD CMPSN, 390 OHMS, 10%, 1/8W	745-2326-000	
R44	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R45	RESISTOR,FXD CMPSN, 680 OHMS, 10%, 1/8W (A1)	745-2335-000	
R45	RESISTOR,FXD CMPSN, 330 OHMS, 10%, 1/8W	745-2323-000	
R46	RESISTOR,FXD CMPSN, 470K, 10%, 1/8W	745-2437-000	
R47	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R48	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/8W	745-2353-000	
R49	RESISTOR,FXD FILM, 20.5K, 1%, 1/8W	705-1059-000	
R50	RESISTOR,FXD CMPSN, 390 OHMS, 10%, 1/8W	745-2326-000	
R51	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R52	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/8W	745-2353-000	
R53	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R54	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R55	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/8W	745-2347-000	
R56	RESISTOR,FXD CMPSN, 470 OHMS, 10%, 1/8W (B2)	745-2329-000	

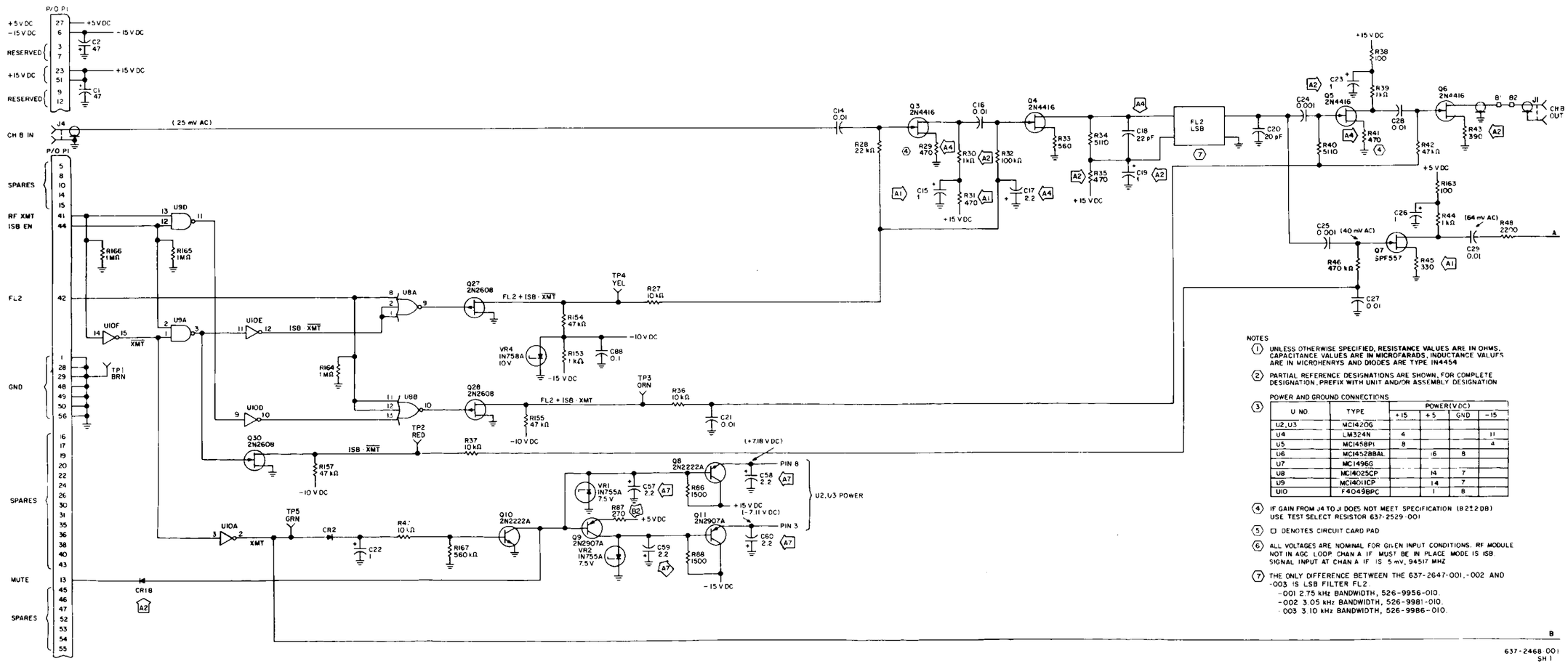
PARTS LIST (CONT)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
R57	RESISTOR,FXD CMPSN, 270 OHMS, 10%, 1/8W	745-2320-000	
R58	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/8W	745-2347-000	
R59	RESISTOR,FXD CMPSN, 15K, 10%, 1/8W	745-2383-000	
R60	NOT USED		
R61	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/8W	745-2292-000	
R62	RESISTOR,FXD CMPSN, 470 OHMS, 10%, 1/8W	745-2329-000	
R63	RESISTOR,FXD CMPSN, 220 OHMS, 10%, 1/8W	745-2317-000	
R64	RESISTOR,FXD CMPSN, 1.2K, 10%, 1/8W	745-2344-000	
R65	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R65	RESISTOR,FXD CMPSN, 15K, 10%, 1/8W (B1)	745-2383-000	
R66	RESISTOR,FXD CMPSN, 560 OHMS, 10%, 1/8W	745-2332-000	
R67	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R68	RESISTOR,FXD CMPSN, 220 OHMS, 10%, 1/8W	745-2317-000	
R100	RESISTOR,FXD CMPSN, 36 OHMS, 5%, 1/8W	745-1863-340	
R101	RESISTOR,FXD CMPSN, 270 OHMS, 10%, 1/8W	745-2320-000	
R102	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/8W	745-2292-000	
R103	RESISTOR,FXD CMPSN, 330 OHMS, 10%, 1/8W	745-2323-000	
R72	NOT USED		
R104	RESISTOR,FXD CMPSN, 330 OHMS, 10%, 1/8W	745-2323-000	
R105,	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R106	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R107			
R108	RESISTOR,FXD FILM, 1.40K, 1%, 1/8W	705-1003-000	
R109	RESISTOR,FXD FILM, 18.7K, 1%, 1/8W	705-1057-000	
R110	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/8W	745-2356-000	
R111	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R112	RESISTOR,FXD FILM, 10K, 1%, 1/8W	705-1044-000	
R113,	RESISTOR,FXD FILM, 12.4K, 1%, 1/8W	705-3605-520	
R114	RESISTOR,FXD FILM, 47.5K, 1%, 1/8W	705-3605-800	
R115,	NOT USED		
R116			
R117	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R118	RESISTOR,FXD FILM, 37.4K, 1%, 1/8W	705-3605-750	
R119	RESISTOR,FXD FILM, 30.1K, 1%, 1/8W	705-1067-000	
R120,	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R121			
R122	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R123	RESISTOR,VAR NON-WW,20K, 10%	382-0052-470	
R124	RESISTOR,FXD FILM, 22.6K, 1%, 1/8W (A3)	705-1061-000	
R124	RESISTOR,FXD FILM, 15.4K, 1%, 1/8W	705-1053-000	
R125	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W (A5)	745-2377-000	
R125	RESISTOR,FXD CMPSN, 6.8K, 10%, 1/8W	745-2371-000	
R126	RESISTOR,FXD FILM, 100K, 1%, 1/8W	705-1092-000	
R127	RESISTOR,FXD FILM, 38.3K, 1%, 1/8W	705-1072-000	
R128	RESISTOR,FXD FILM, 13K, 1%, 1/8W	705-3605-530	
R129	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/8W	745-2356-000	
R130	RESISTOR,FXD CMPSN, 270K, 10%, 1/8W (A1)	745-2428-000	
R130	RESISTOR,FXD CMPSN, 470K, 10%, 1/8W	745-2437-000	
R131	RESISTOR,FXD CMPSN, 18K, 10%, 1/8W	745-2386-000	
R132	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R133	RESISTOR,FXD CMPSN, 680 OHMS, 10%, 1/8W	745-2335-000	
R134	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R135	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R136	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R137	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R138	RESISTOR,FXD CMPSN, 560K, 10%, 1/8W	745-2440-000	
R139,	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R140			
R141	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R142	RESISTOR,FXD CMPSN, 820 OHMS, 10%, 1/8W	745-2338-000	
R143	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/8W	745-2292-000	
R144	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R145,	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R146			
R147	RESISTOR,FXD CMPSN, 1.3K, 5%, 1/8W	745-1863-520	
R148	RESISTOR,FXD CMPSN, 180 OHMS, 10%, 1/8W	745-2314-000	
R149	RESISTOR,FXD CMPSN, 3K, 5%, 1/8W	745-1863-600	
R150	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R151	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R152	RESISTOR,VAR 2K, 20%, 1/2W	382-0038-050	
R153	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R154,	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R155			
R156	NOT USED		
R157	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R158	NOT USED		
R159	RESISTOR,FXD CMPSN, 8.2MEGO, 5%, 1/8W	745-1864-470	
R160	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/4W	745-0713-000	
R161	RESISTOR,FXD FILM, 221K, 1%, 1/8W	705-3604-170	
R162	NOT USED		
R163	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R164-	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R166			
R167	RESISTOR,FXD CMPSN, 560K, 10%, 1/8W	745-2440-000	
R168	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R169	RESISTOR,FXD CMPSN, 330K, 5%, 1/8W (A2)	745-1864-130	
R169	RESISTOR,FXD CMPSN, 430K, 5%, 1/8W	745-1864-160	
R170	RESISTOR,FXD FILM, 10K, 1%, 1/8W	705-1044-000	
TP1	JACK,TIP BRN	360-0484-070	
TP2	JACK,TIP RED	360-0484-020	

PARTS LIST (CONT)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
TP3	JACK,TIP ORN	360-0484-050	
TP4	JACK,TIP YEL	360-0484-060	
TP5	JACK,TIP GRN	360-0484-040	
T1	TRANSFORMER,RF	278-0432-030	
U1	NOT USED		
U2,U3	INTEGRATED CIRCUIT MC1420G	351-1050-030	
U4	INTEGRATED CIRCUIT LM324N	351-1141-030	
U5	INTEGRATED CIRCUIT MC1458P1	351-1071-070	
U6	INTEGRATED CIRCUIT CD4098BE	351-8278-010	
U7	INTEGRATED CIRCUIT MC14966	351-0043-020	
U8	INTEGRATED CIRCUIT MC14025CP	351-8159-150	
U9	INTEGRATED CIRCUIT MC14011CP	351-8159-040	
U10	INTEGRATED CIRCUIT F40498PC	351-8159-210	
VR1,VR2	SEMICOND DEVICE 1N755A	353-2716-000	
VR3	SEMICOND DEVICE 1N751A	353-2710-000	
VR4	SEMICOND DEVICE 1N758A	353-2724-000	
R29,R41	RESISTOR,FXD,CMPSN, 200 THRU 1K, 5%,1/8W (TEST SELECT)	637-2529-001	

Channel B IF, Through REV T, Schematic Diagram
Figure 11 (Sheet 2)



NOTES

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, INDUCTANCE VALUES ARE IN MICROHENRYS AND DIODES ARE TYPE IN4454
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION
3. POWER AND GROUND CONNECTIONS

U NO.	TYPE	POWER (V DC) +15	+5	GND	-15
U2,U3	MC1420G				
U4	LM324N	4			11
U5	MC1458PI	8			4
U6	MC14528BAL		16	8	
U7	MC1496G				
U8	MC14025CP		14	7	
U9	MC14011CP		14	7	
U10	F4049BPC		1	8	

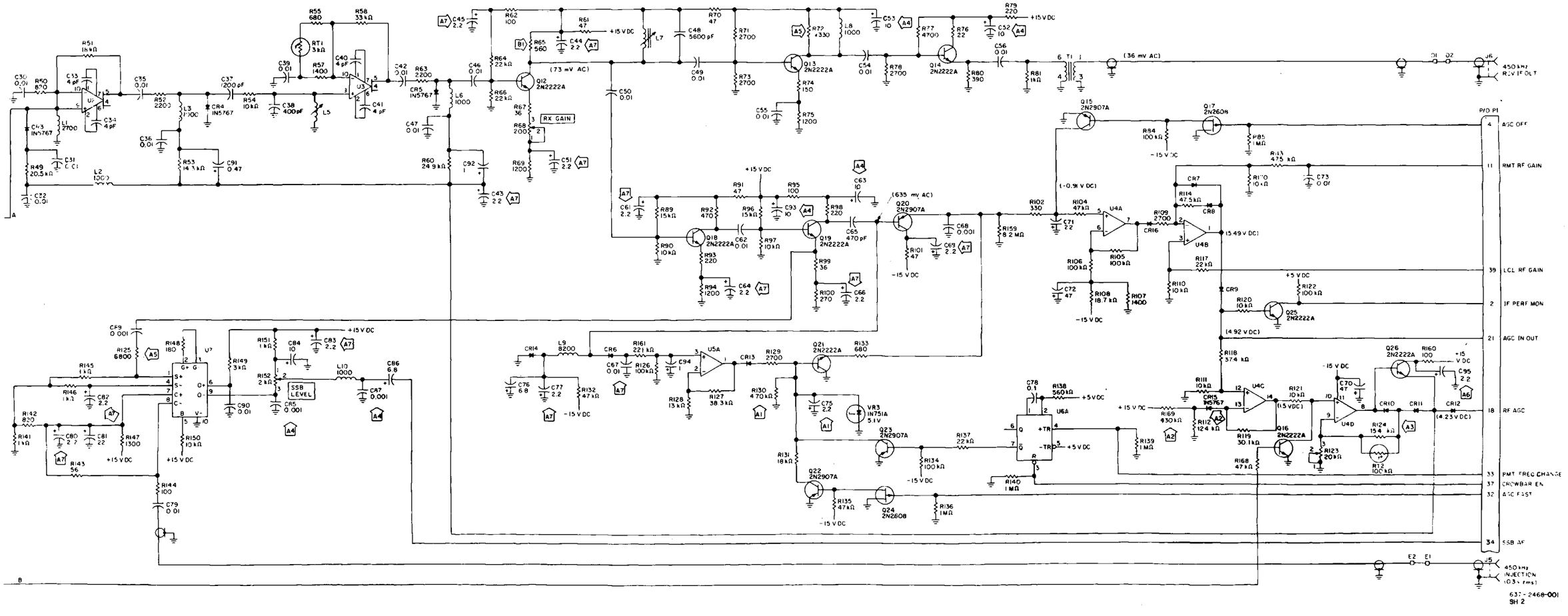
4. IF GAIN FROM J4 TO J1 DOES NOT MEET SPECIFICATION (8 ± 2 DB) USE TEST SELECT RESISTOR 637-2529-001
5. ☐ DENOTES CIRCUIT CARD PAD
6. ALL VOLTAGES ARE NOMINAL FOR GIVEN INPUT CONDITIONS. RF MODULE NOT IN AGC LOOP. CHAN A IF MUST BE IN PLACE. MODE IS ISB. SIGNAL INPUT AT CHAN A IF IS 5 mV, 94517 MHZ
7. THE ONLY DIFFERENCE BETWEEN THE 637-2647-001, -002 AND -003 IS LSB FILTER FL2.
   - -001 2.75 kHz BANDWIDTH, 526-9956-010.
   - -002 3.05 kHz BANDWIDTH, 526-9981-010.
   - -003 3.10 kHz BANDWIDTH, 526-9986-010.

Channel B IF, Through REV T, Schematic Diagram
Figure 11 (Sheet 3)

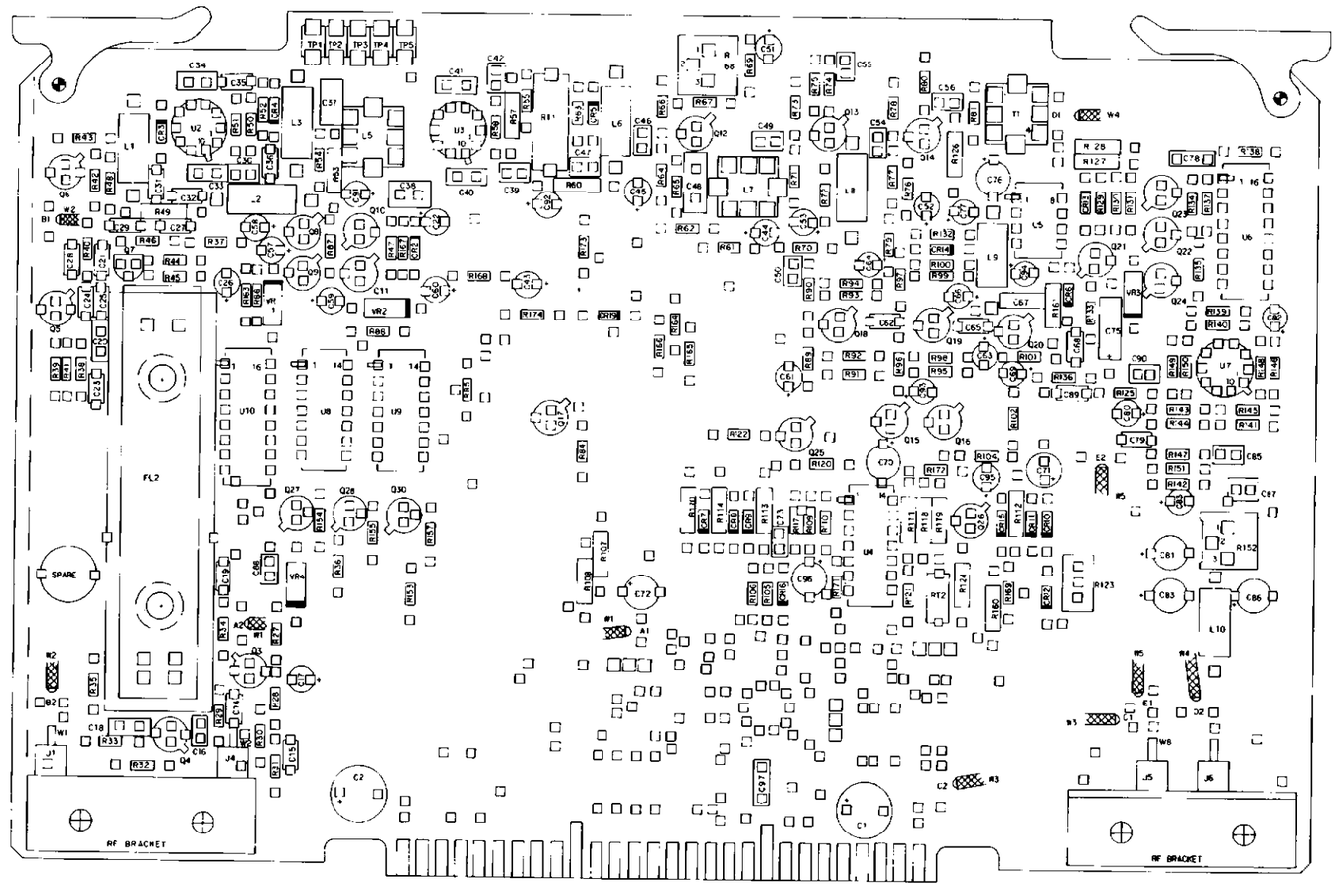
MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Changed: C15 from 0.01μF to 1μF. C75 from 4.7μF to 2.2μF. R31from 100Ω to 470Ω. R45 from 680Ω to 330Ω. R130 from 270kΩ to 470kΩ.	REV C and above
A2	Added CR18, 1N4454. Changed: CR15 from 1N8116 to 1N5767. C19 from 0.01μF to 1μF. C23 from 0.01μF to 1μF. R30 from 560Ω to 1kΩ. R35 from 100Ω to 470Ω. R43 from test select of 200Ω thru 680Ω to fixed 390Ω. R169 from 330kΩ to 430kΩ.	REV D and above
A3	Changed R124 from 22.6kΩ to 13.4kΩ.	REV E and above
A4	Changed: C17 from 0.01μF to 2.2μF. C18 from 15pF to 22pF. C52 from 1μF to 10μF. C53 from 1μF to 10μF. C63 from 1μF to 10μF. C85 from 0.01μF to 1000pF. C87 from 0.01μF to 1000pF. C93 from 1μF to 10μF. R29 from 560Ω to 470Ω. R41 from test select of 200Ω thru 680Ω to fixed 470Ω.	REV F and above
A5	Changed: R72 from 470Ω to 330Ω. R125 from 10kΩ to 6800Ω.	REV J and above.
A6	Added C95, 2.2μF.	REV K and above
A7	Changed: C43 from 0.1μF to 2.2μF. C44 from 0.1μF to 2.2μF. C57 from 0.1μF to 2.2μF. C58 from 0.1μF to 2.2μF. C59 from 0.1μF to 2.2μF. C60 from 0.1μF to 2.2μF. C61 from 0.1μF to 2.2μF. C64 from 0.1μF to 2.2μF. C66 from 0.1μF to 2.2μF. C67 from 0.1μF to 0.01μF. C69 from 0.1μF to 2.2μF. C77 from 0.1μF to 2.2μF. C78 from 0.1μF to 0.01μF. C80 from 0.1μF to 2.2μF. C82 from 0.1μF to 2.2μF. C83 from 0.1μF to 2.2μF.	REV L and above
B1	Changed R65 from 1200Ω to 560Ω.	REV N and above.
B2	Changed R87 from 470Ω to 270Ω.	REV T and above.

Channel B IF, Through REV T, Schematic Diagram
Figure 11 (Sheet 4)



Channel B IF, Through REV T, Schematic Diagram
Figure 11 (Sheet 5)



Channel B IF, REV U and Above,
Schematic Diagram
Figure 12 (Sheet 1 of 5)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
	CHANNEL B IF A7	637-2647-001	A
	CHANNEL B IF A7	637-2647-002	B
	CHANNEL B IF A7	637-2647-003	C
CR1	NOT USED		
CR2	SEMICOND DEVICE 1N4454	353-3644-010	
CR3-CR5	SEMICOND DEVICE 1N5767	922-6119-010	
CR6-CR14	SEMICOND DEVICE 1N4454	353-3644-010	
CR15	SEMICOND DEVICE 1N5767	922-6119-010	
CR16	SEMICOND DEVICE 1N4454	353-3644-010	
CR17,	NOT USED		
CR18			
CR19	SEMICOND DEVICE 1N4454	353-3644-010	
C1,C2	CAPACITOR,FXD ELCTLT, 47UF, 20%, 20V	184-9102-630	
C3-C13	NOT USED		
C14	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C15	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C16	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C17	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C18	CAPACITOR,FXD MICA DIEL, 22PF, PORM 0.5PF, 300V	912-4141-030	
C19	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C20	CAPACITOR,FXD MICA DIEL, 20PF, PORM 0.5PF, 100V	912-4141-150	
C21	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C22,C23	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C24,C25	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C26	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C27-C29	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C30	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C31,C32	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C33,C34	CAPACITOR,FXD MICA DIEL, 4PF, PORM 0.5PF, 300V	912-4141-080	
C35,C36	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C37	CAPACITOR,FXD CER DIEL, 1200PF, 5%, 100V	913-3281-290	
C38	CAPACITOR,FXD MICA DIEL, 400PF, 5%, 50V	912-4141-520	
C39	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C40,C41	CAPACITOR,FXD MICA DIEL, 4PF, PORM 0.5PF, 300V	912-4141-080	
C42	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C43-C45	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C46,C47	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C48	CAPACITOR,FXD CER DIEL, 5600PF, 5%, 100V	913-3281-380	
C49,C50	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C51	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C52,C53	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C54-C56	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C57-C61	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C62	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C63	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C64	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C65	CAPACITOR,FXD CER DIEL, 470PF, 10%, 200V	913-4014-000	
C66	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C67	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C68	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C69	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C70	CAPACITOR,FXD ELCTLT, 15UF, 20%, 20V	184-9102-620	
C71	CAPACITOR,FXD ELCTLT, 22UF, 20%, 15V	184-9102-140	
C72	CAPACITOR,FXD ELCTLT, 47UF, 20%, 6V	184-9102-470	
C73	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C74	NOT USED		
C75	CAPACITOR,FXD ELCTLT, 2.2UF, 10%, 20V	184-9086-430	
C76	CAPACITOR,FXD ELCTLT, 6.8UF, 20%, 6V	184-9102-450	
C77	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C78	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C79	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C80	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C81	CAPACITOR,FXD ELCTLT, 22UF, 20%, 10V	184-9102-520	
C82,C83	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C84	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-610	
C85	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C86	CAPACITOR,FXD ELCTLT, 6.8UF, 20%, 25V	184-9102-670	
C87	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C88	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-180	
C89	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C90	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C91	CAPACITOR,FXD ELCTLT, 0.47UF, 20%, 35V	184-9102-330	
C92	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C93	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C94	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C95	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C96	CAPACITOR,FXD ELCTLT, 15UF, 20%, 20V	184-9102-620	
C97	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
FL1	NOT USED		
FL2	FILTER,LSB,2.75 KHZ	526-9956-010	A
FL2	FILTER,LSB,3.05 KHZ	526-9981-010	B
FL2	FILTER,LSB,3.10 KHZ	526-9986-010	C
L1	COIL,RF 2700UH	240-2715-540	
L2,L3	COIL,RF 1000UH	240-2715-490	
L4	NOT USED		
L5	INDUCTOR,RF	242-0441-010	
L6	COIL,RF 1000UH	240-2715-490	
L7	INDUCTOR,RF	242-0441-020	
L8	COIL,RF 1000UH	240-2715-490	
L9	COIL,RF 8200UH	240-2715-600	

PARTS LIST (CONT)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
L10	COIL,RF 1000UH	240-2715-490	
Q1,Q2	NOT USED		
Q3-Q6	TRANSISTOR 2N4416	352-0756-010	
Q7	TRANSISTOR SPF557	352-1068-010	
Q8	TRANSISTOR 2N2222A	352-0661-020	
Q9	TRANSISTOR 2N2907A	352-0551-010	
Q10	TRANSISTOR 2N2222A	352-0661-020	
Q11	TRANSISTOR 2N2907A	352-0551-010	
Q12-Q14	TRANSISTOR 2N2222A	352-0661-020	
Q15	TRANSISTOR 2N2907A	352-0551-010	
Q16	TRANSISTOR 2N2222A	352-0661-020	
Q17	TRANSISTOR 2N2608	352-0605-010	
Q18,Q19	TRANSISTOR 2N2222A	352-0661-020	
Q20	TRANSISTOR 2N2907A	352-0551-010	
Q21	TRANSISTOR 2N2222A	352-0661-020	
Q22,Q23	TRANSISTOR 2N2907A	352-0551-010	
Q24	TRANSISTOR 2N2608	352-0605-010	
Q25,Q26	TRANSISTOR 2N2222A	352-0661-020	
Q27,Q28	TRANSISTOR 2N2608	352-0605-010	
Q29	NOT USED		
Q30	TRANSISTOR 2N2608	352-0605-010	
RT1	RESISTOR,THRM 3K, 10%, 1W	714-1715-000	
RT2	RESISTOR,THRM 100K, 10%, 0.5W	714-1736-000	
R1-R26	NOT USED		
R27	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R28	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R29	RESISTOR,FXD CMPSN, 470 OHMS, 10%, 1/8W	745-2329-000	
R30	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R31	RESISTOR,FXD CMPSN, 470 OHMS, 10%, 1/8W	745-2329-000	
R32	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R33	RESISTOR,FXD CMPSN, 560 OHMS, 10%, 1/8W	745-2332-000	
R34	RESISTOR,FXD FILM, 5.11K, 1%, 1/8W	705-1030-000	
R35	RESISTOR,FXD CMPSN, 470 OHMS, 10%, 1/8W	745-2329-000	
R36,R37	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R38	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R39	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R40	RESISTOR,FXD FILM, 5.11K, 1%, 1/8W	705-1030-000	
R41	RESISTOR,FXD CMPSN, 470 OHMS, 10%, 1/8W	745-2329-000	
R42	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R43	RESISTOR,FXD CMPSN, 390 OHMS, 10%, 1/8W	745-2326-000	
R44	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R45	RESISTOR,FXD CMPSN, 330 OHMS, 10%, 1/8W	745-2323-000	
R46	RESISTOR,FXD CMPSN, 470K, 10%, 1/8W	745-2437-000	
R47	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R48	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/8W	745-2353-000	
R49	RESISTOR,FXD FILM, 20.5K, 1%, 1/8W	705-1059-000	
R50	RESISTOR,FXD CMPSN, 820 OHMS, 10%, 1/8W	745-2338-000	
R51	RESISTOR,FXD CMPSN, 18K, 10%, 1/8W	745-2386-000	
R52	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/8W	745-2353-000	
R53	RESISTOR,FXD FILM, 14.3K, 1%, 1/8W	705-3605-550	
R54	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R55	RESISTOR,FXD CMPSN, 680 OHMS, 10%, 1/8W	745-2335-000	
R56	NOT USED		
R57	RESISTOR,FXD FILM, 1.40K, 1%, 1/8W	705-1003-000	
R58	RESISTOR,FXD CMPSN, 33K, 10%, 1/8W	745-2395-000	
R59	NOT USED		
R60	RESISTOR,FXD FILM, 24.9K, 1%, 1/8W	705-1063-000	
R61	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/8W	745-2292-000	
R62	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R63	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/8W	745-2353-000	
R64	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R65	RESISTOR,FXD CMPSN, 1.2K, 10%, 1/8W	745-2344-000	A,B
R65	RESISTOR,FXD CMPSN, 560 OHMS, 10%, 1/8W	745-2332-000	C
R66	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R67	RESISTOR,FXD CMPSN, 36 OHMS, 5%, 1/8W	745-1863-140	
R68	RESISTOR,VAR 200 OHMS, 20%, 1/2W	382-0038-020	
R69	RESISTOR,FXD CMPSN, 1.2K, 10%, 1/8W	745-2344-000	
R70	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/8W	745-2292-000	
R71	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/8W	745-2356-000	
R72	RESISTOR,FXD CMPSN, 330 OHMS, 10%, 1/8W	745-2323-000	
R73	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/8W	745-2356-000	
R74	RESISTOR,FXD CMPSN, 150 OHMS, 10%, 1/8W	745-2311-000	
R75	RESISTOR,FXD CMPSN, 1.2K, 10%, 1/8W	745-2344-000	
R76	RESISTOR,FXD CMPSN, 22 OHMS, 10%, 1/8W	745-2280-000	
R77	RESISTOR,FXD CMPSN, 4.7K, 10%, 1/8W	745-2365-000	
R78	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/8W	745-2356-000	
R79	RESISTOR,FXD CMPSN, 220 OHMS, 10%, 1/8W	745-2317-000	
R80	RESISTOR,FXD CMPSN, 390 OHMS, 10%, 1/8W	745-2326-000	
R81	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R82,R83	NOT USED		
R84	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R85	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R86	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/8W	745-2347-000	
R87	RESISTOR,FXD CMPSN, 270 OHMS, 10%, 1/8W	745-2320-000	
R88	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/8W	745-2347-000	
R89	RESISTOR,FXD CMPSN, 15K, 10%, 1/8W	745-2383-000	
R90	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R91	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/8W	745-2292-000	
R92	RESISTOR,FXD CMPSN, 470 OHMS, 10%, 1/8W	745-2329-000	
R93	RESISTOR,FXD CMPSN, 220 OHMS, 10%, 1/8W	745-2317-000	
R94	RESISTOR,FXD CMPSN, 1.2K, 10%, 1/8W	745-2344-000	
R95	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	

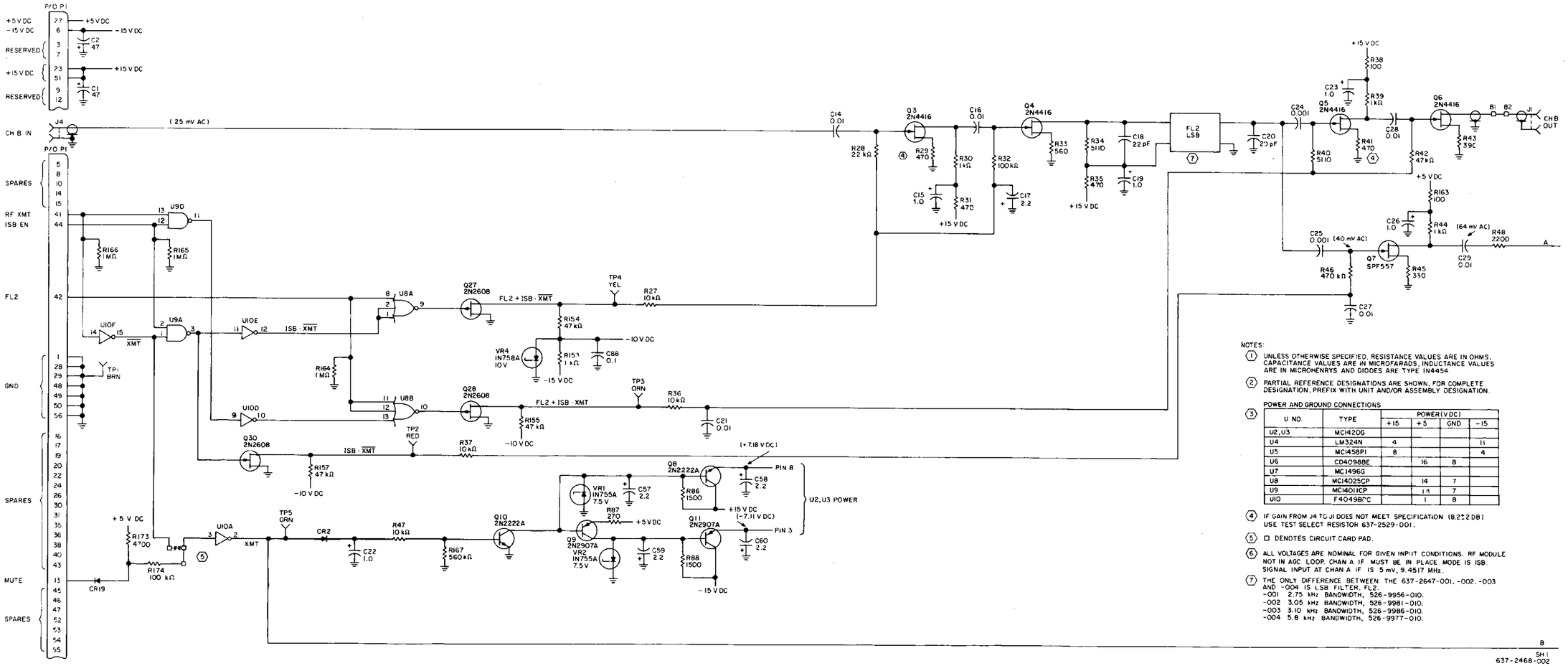
PARTS LIST (CONT)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
R96	RESISTOR,FXD CMPSN, 15K, 10%, 1/8W	745-2383-000	
R97	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R98	RESISTOR,FXD CMPSN, 220 OHMS, 10%, 1/8W	745-2317-000	
R99	RESISTOR,FXD CMPSN, 36 OHMS, 5%, 1/8W	745-1863-140	
R100	RESISTOR,FXD CMPSN, 270 OHMS, 10%, 1/8W	745-2320-000	
R101	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/8W	745-2292-000	
R102	RESISTOR,FXD CMPSN, 330 OHMS, 10%, 1/8W	745-2323-000	
R103	NOT USED		
R104	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R105,	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R106			
R107	RESISTOR,FXD FILM, 1.40K, 1%, 1/8W	705-1003-000	
R108	RESISTOR,FXD FILM, 18.7K, 1%, 1/8W	705-1057-000	
R109	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/8W	745-2356-000	
R110	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R111	RESISTOR,FXD FILM, 10K, 1%, 1/8W	705-1044-000	
R112	RESISTOR,FXD FILM, 12.4K, 1%, 1/8W	705-3605-520	
R113,	RESISTOR,FXD FILM, 47.5K, 1%, 1/8W	705-3605-800	
R114			
R115,	NOT USED		
R116			
R117	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R118	RESISTOR,FXD FILM, 37.4K, 1%, 1/8W	705-3605-750	
R119	RESISTOR,FXD FILM, 30.1K, 1%, 1/8W	705-1067-000	
R120,	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R121			
R122	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R123	RESISTOR,VAR NON-WW,20K, 10%	382-0052-470	
R124	RESISTOR,FXD FILM, 15.4K, 1%, 1/8W	705-1053-000	
R125	RESISTOR,FXD CMPSN, 6.8K, 10%, 1/8W	745-2371-000	
R126	RESISTOR,FXD FILM, 100K, 1%, 1/8W	705-1092-000	
R127	RESISTOR,FXD FILM, 38.3K, 1%, 1/8W	705-1072-000	
R128	RESISTOR,FXD FILM, 13K, 1%, 1/8W	705-3605-530	
R129	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/8W	745-2356-000	
R130	RESISTOR,FXD CMPSN, 470K, 10%, 1/8W	745-2437-000	
R131	RESISTOR,FXD CMPSN, 18K, 10%, 1/8W	745-2386-000	
R132	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R133	RESISTOR,FXD CMPSN, 680 OHMS, 10%, 1/8W	745-2335-000	
R134	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R135	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R136	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R137	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R138	RESISTOR,FXD CMPSN, 560K, 10%, 1/8W	745-2440-000	
R139,	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R140			
R141	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R142	RESISTOR,FXD CMPSN, 820 OHMS, 10%, 1/8W	745-2338-000	
R143	RESISTOR,FXD CMPSN, 56 OHMS, 10%, 1/8W	745-2295-000	
R144	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R145,	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R146			
R147	RESISTOR,FXD CMPSN, 1.3K, 5%, 1/8W	745-1863-520	
R148	RESISTOR,FXD CMPSN, 180 OHMS, 10%, 1/8W	745-2314-000	
R149	RESISTOR,FXD CMPSN, 3K, 5%, 1/8W	745-1863-600	
R150	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R151	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R152	RESISTOR,VAR 2K, 20%, 1/2W	382-0038-050	
R153	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R154,	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R155			
R156	NOT USED		
R157	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R158,	NOT USED		
R159			
R160	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/4W	745-0713-000	
R161	RESISTOR,FXD FILM, 221K, 1%, 1/8W	705-3604-170	
R162	NOT USED		
R163	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R164-	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R166			
R167	RESISTOR,FXD CMPSN, 560K, 10%, 1/8W	745-2440-000	
R168	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R169	RESISTOR,FXD CMPSN, 430K, 5%, 1/8W	745-1864-160	
R170	RESISTOR,FXD FILM, 10K, 1%, 1/8W	705-1044-000	
R171,	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R172			
R173	RESISTOR,FXD CMPSN, 4.7K, 10%, 1/8W	745-2365-000	
R174	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
TP1	JACK,TIP BRN	360-0484-070	
TP2	JACK,TIP RED	360-0484-020	
TP3	JACK,TIP ORN	360-0484-050	
TP4	JACK,TIP YEL	360-0484-060	
TP5	JACK,TIP GRN	360-0484-040	
T1	TRANSFORMER,RF	278-0432-030	
U1	NOT USED		
U2,U3	INTEGRATED CIRCUIT MC1420G	351-1050-030	
U4	INTEGRATED CKT LM324N	351-1141-030	
U5	INTEGRATED CIRCUIT MC1458P1	351-1071-070	
U6	INTEGRATED CIRCUIT CD4098BE	351-8278-010	
U7	INTEGRATED CIRCUIT MC1496G	351-0043-020	
U8	INTEGRATED CIRCUIT MC14025CP	351-8159-150	
U9	INTEGRATED CIRCUIT MC14011CP	351-8159-040	

PARTS LIST (CONT)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
U10	INTEGRATED CIRCUIT F4049BPC	351-8159-210	
VR1,VR2	SEMICOND DEVICE 1N755A	353-2718-000	
VR3	SEMICOND DEVICE 1N751A	353-2710-000	
VR4	SEMICOND DEVICE 1N758A	353-2724-000	
R29,R41	RESISTOR,FXD,CMPSN, 200 THRU 1K, 5%,1/8W (TEST SELECT)	637-2529-001	

Channel B IF, REV U and Above, Schematic Diagram
Figure 12 (Sheet 2)



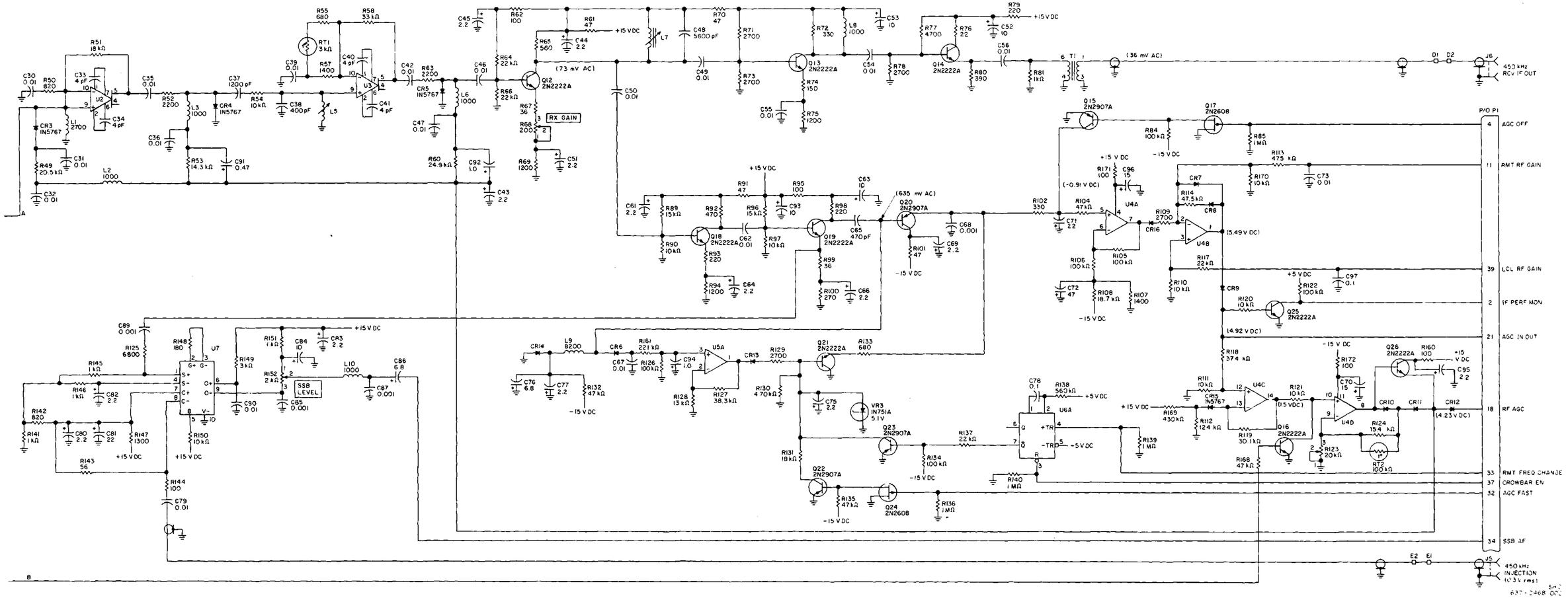
NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, INDUCTANCE VALUES ARE IN MICROHENRYS AND DIODES ARE TYPE 1N4454.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. POWER AND GROUND CONNECTIONS

U NO.	TYPE	POWER (VDC) +15	+5	GND	-15
U2,U3	MC1420G				
U4	LM324N	4			11
U5	MC1458P1	8			4
U6	CD4098BE		16	8	
U7	MC1496G				
U8	MC14025CP		14	7	
U9	MC14011CP		14	7	
U10	F40498PC		1	8	

4. IF GAIN FROM J4 TO J1 DOES NOT MEET SPECIFICATION (8.2±2 DB) USE TEST SELECT RESISTOR 637-2529-001.
5. □ DENOTES CIRCUIT CARD PAD.
6. ALL VOLTAGES ARE NOMINAL FOR GIVEN INPUT CONDITIONS. RF MODULE NOT IN AGC LOOP. CHAN A IF MUST BE IN PLACE. MODE IS ISB. SIGNAL INPUT AT CHAN A IF IS 5 mV, 9.4517 MHz.
7. THE ONLY DIFFERENCE BETWEEN THE 637-2647-001, -002, -003 AND -004 IS LSB FILTER, FL2.
   -001 2.75 kHz BANDWIDTH, 526-9956-010.
   -002 3.05 kHz BANDWIDTH, 526-9981-010.
   -003 3.10 kHz BANDWIDTH, 526-9986-010.
   -004 5.8 kHz BANDWIDTH, 526-9977-010.

Channel B IF, REV U and Above, Schematic Diagram
Figure 12 (Sheet 3)



Channel B IF, REV U and Above, Schematic Diagram
Figure 12 (Sheet 4)

Channel A IF (637-2650-( ))

Rockwell International

instructions

Collins Telecommunications Products Division

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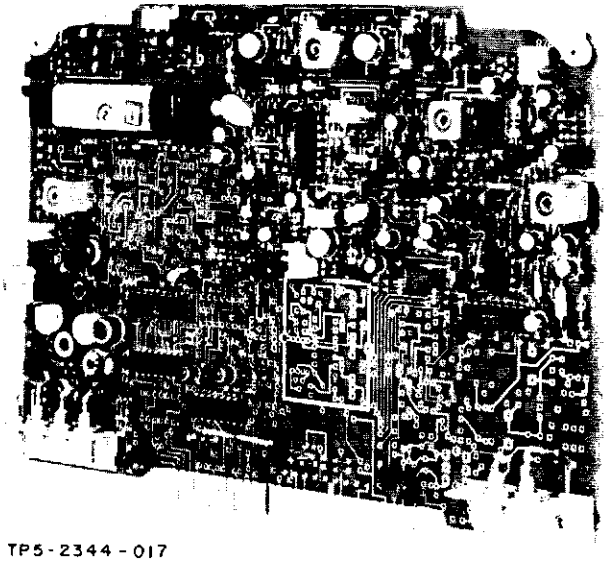
3rd Edition, 1 January 1979

1. DESCRIPTION

Channel A IF 637-2650-( ), shown in figure 1, is a 2-layer planar card with 56-pin edge-on connector (2 layers, 28 pins each). The channel A if card has subminiax rf connectors for connecting to channel B if input (J1), 9.45-MHz receive input (J2), 9.9-MHz injection input (J3), channel B if output (J4), 450-kHz injection input (J5), and 450-kHz receive if input (J6).

The channel A if card consists of filter control, channel A if, channel A audio detector, and channel A AGC circuits.



TP5-2344-017

Channel A IF
Figure 1

The channel A if configuration differences are as follows:

a. 637-2650-001, FL1 has 2.75-kHz bandwidth (250 to 3000 Hz, USB).
b. 637-2650-002, FL1 has 3.05-kHz bandwidth (250 to 3300 Hz, USB).
c. 637-2650-003, FL1 has 3.10-kHz bandwidth (300 to 3400 Hz, USB).
d. 637-2650-004, reserved.
e. 637-2650-005, FL1 has 5.80-kHz bandwidth (200 to 6000 Hz, USB).

2. PRINCIPLES OF OPERATION

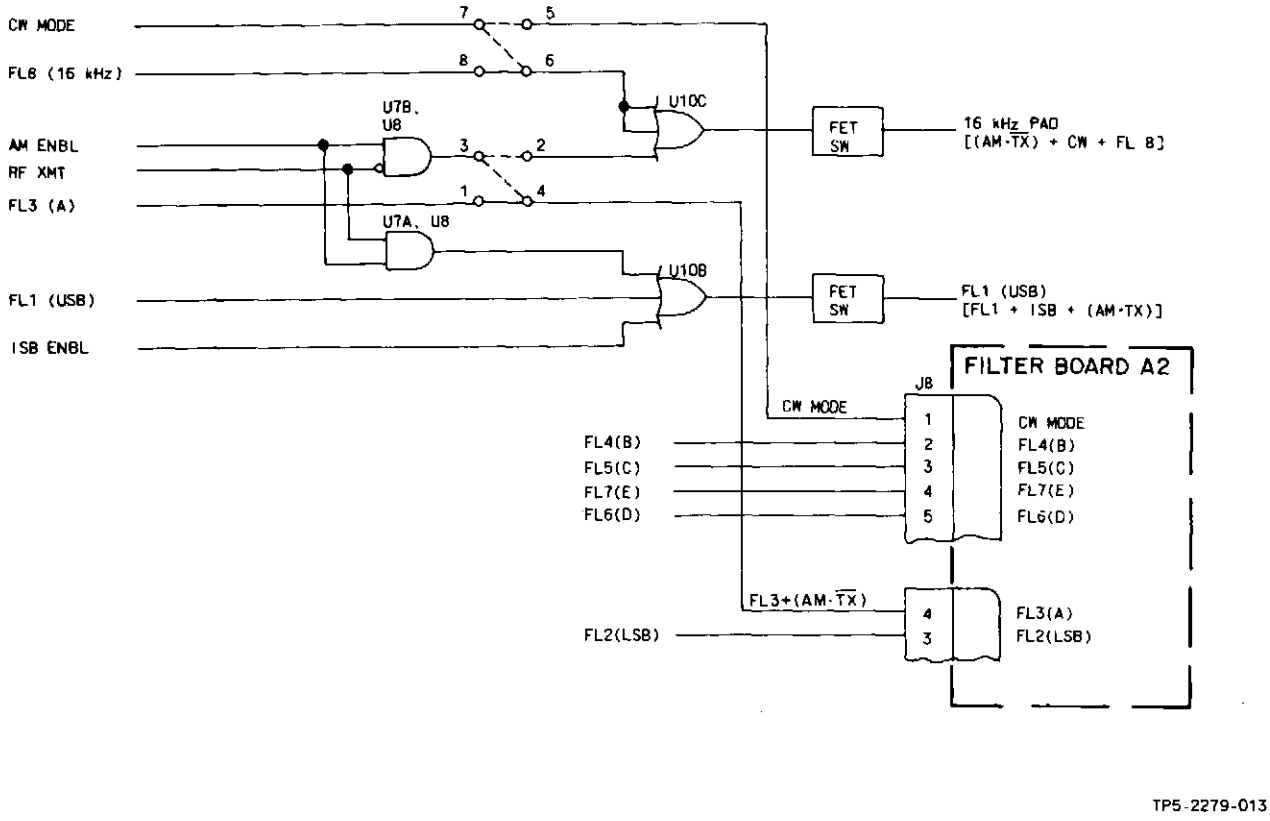
2.1 General

The channel A if receives the 9.45-MHz receive if input; mixes it with a 9.9-MHz fixed injection signal; filters the resulting 450-kHz receive if signal; and provides (1) 450-kHz receive if output, (2) AM audio output, (3) a product detected channel A SSB audio output, and (4) AGC control signals.

2.2 Bandpass Filter Control Circuits (Refer to figure 2.)

The channel A if provides filter selection for receive if signals. Filter selection is initiated by the mode control signal, bandwidth control signal, and/or rf transmit signal. This means only that these signals are applied to the channel A if card to initiate filter selection and does not reflect a mode of operation, selection of a bandwidth, or transmission of an rf signal.

NOTICE: This section replaces second edition dated 1 June 1978.



Bandpass Filter Control Circuits
Figure 2

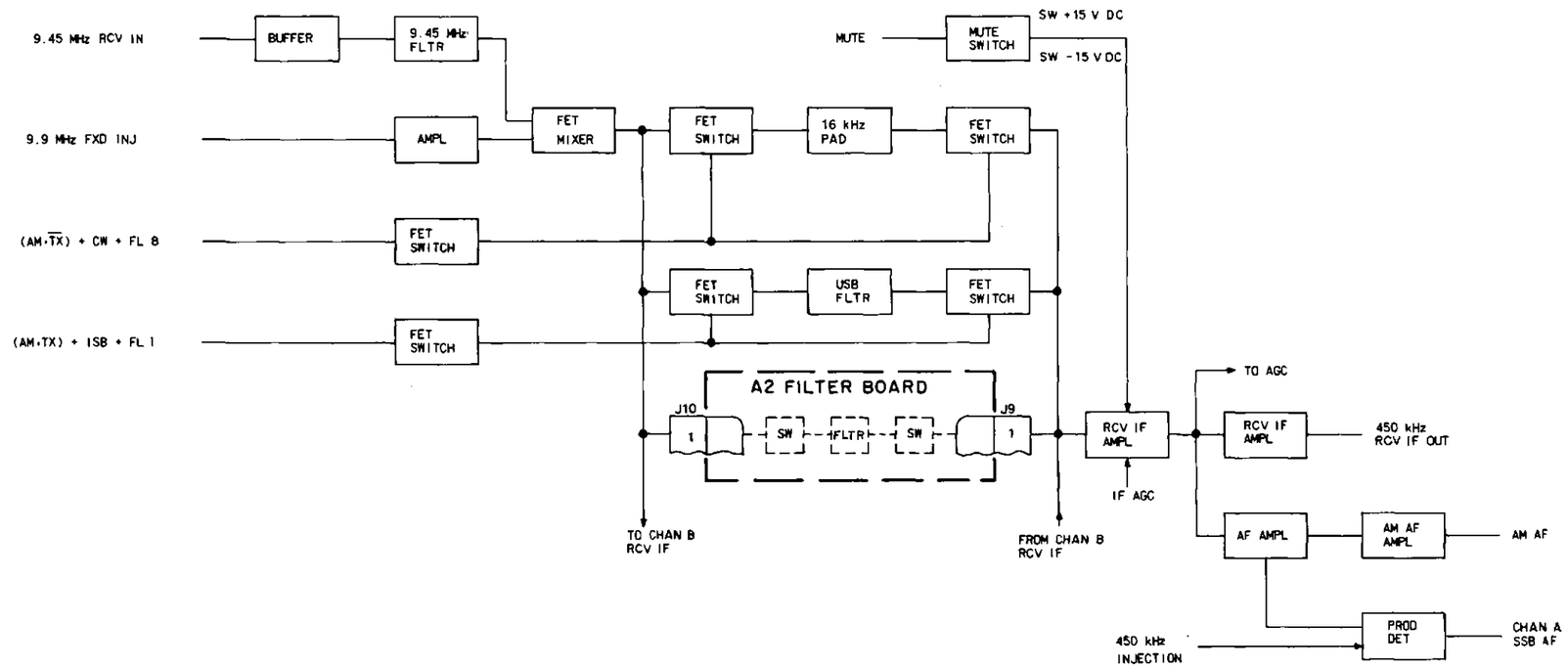
FL1 (USB) is selected when an FL1 (USB) enable signal, an ISB enable signal, and/or AM enable and rf transmit signals are applied to the channel A if card.

When strapped, 8-6 and 1-4: FL8 (16-kHz pad) is selected when an FL8 (16 kHz) enable signal is applied to the channel A if card. FL3 (A) is selected on A2 filter board when an FL3 (A) enable signal is applied to channel A if card (A2 is optional board).

FL2 (LSB), FL4 (B), FL5 (C), FL6 (D), and FL7 (E) are selected when the associated enable signal is applied to the channel A if card. These filters are mounted (if used) on the optional A2 filter board.

2.3 Channel A IF Circuits (Refer to figure 3.)

The channel A if card receives 9.45-MHz receive if through a buffer and a 9.45-MHz filter. The 9.45-MHz receive if is mixed in an FET mixer with a 9.9-MHz fixed injection signal and supplies a 450-kHz if frequency to the bandpass filter networks. Bandpass filters are located on the channel A if card, the A2 filter board, and/or an associated channel B if card. After mode/bandwidth selection, the 450-kHz if signal is supplied through the associated bandpass filter and amplified. The amplified 450 kHz is then



TP5-2280-014

Channel A IF Circuits
Figure 3

applied to AGC circuits, a receive if amplifier as an external 450-kHz receive if output, an audio amplifier to an AM audio detector, and/or the SSB audio product detector. The AM audio amplifier detects the audio and provides an AM audio output. The SSB product detector receives the receive if and a 450-kHz injection and supplies a product detected SSB audio output.

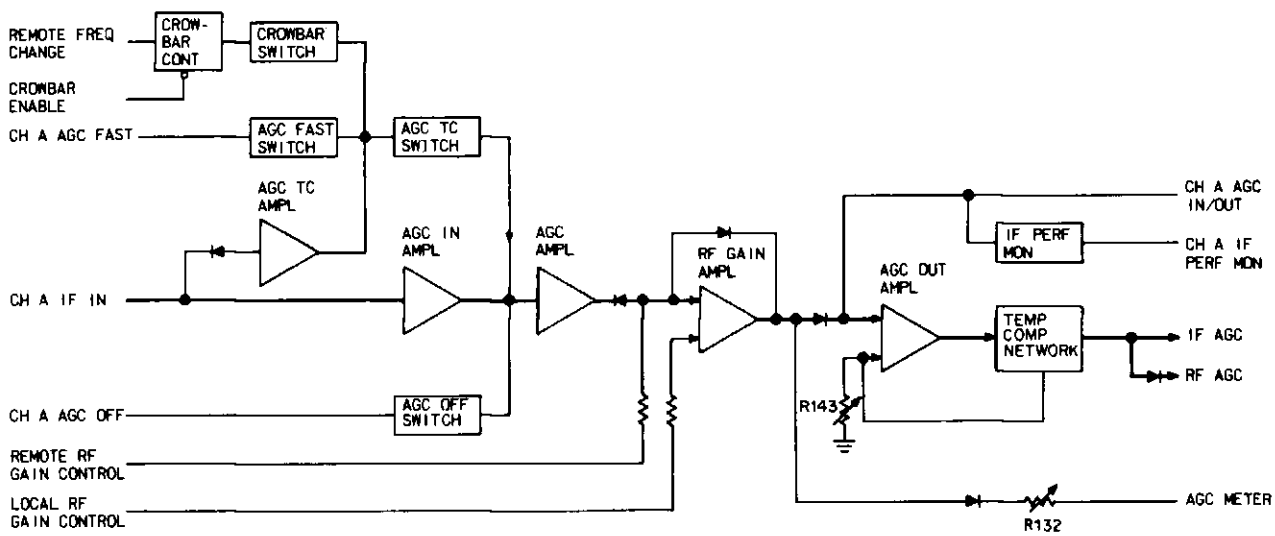
2.4 AGC Circuits (Refer to figure 4.)

Channel A if is received by the AGC input amplifier. The AGC input amplifier and associated AGC time constant switches develop the AGC level and decay time to be used by the receiver. The AGC level is amplified and applied through rf gain amplifier and supplied to the if performance monitor and AGC output amplifier. The if AGC and rf AGC signals are developed and supplied to the associated attenuator circuits. With the AGC control in the SLOW position, only the AGC time constant amplifier and AGC time constant switch are enabled and establish a 1.0-second AGC decay time. (The AGC to amplifier and AGC to switch are enabled for all AGC functions.) With the AGC control in the FAST position, the AGC fast switch is enabled reducing the time constant of the AGC circuits and establishing a 0.1-second AGC decay time. With the AGC control in the OFF position, the output of the AGC input amplifier is disabled and removed from the input of the AGC amplifier.

With the receiver in remote control and a crowbar enable applied, a remote frequency change enables the crowbar switch and reduces the AGC time constant and establishes the AGC decay time at about 2 milliseconds. The crowbar function is used for fast frequency hopping or scanning operation under processor control.

The gain of the rf gain amplifier is controlled by a local rf gain control signal. The dc voltage level applied to the noninverting input of the rf gain amplifier establishes its gain. The remote rf gain control signal establishes the minimum gain output of the rf gain amplifier.

R132 sets the level for the correct reading of the AGC meter (0 dB at 1-μV input to 100 dB above the 1-μV input).



AGC Circuits
Figure 4

From the rf gain amplifier, the AGC output is supplied to channel A AGC output for use by other cards and to the channel A if performance monitor for channel A AGC indications. The rf gain amplifier output is supplied to AGC output amplifier that develops the if/rf AGC outputs. R143 and temperature compensating network are used to keep the if/rf AGC outputs constant throughout the temperature range.

2.5 Differential Output Operational Amplifier 351-1050-030 (Refer to figure 5.)

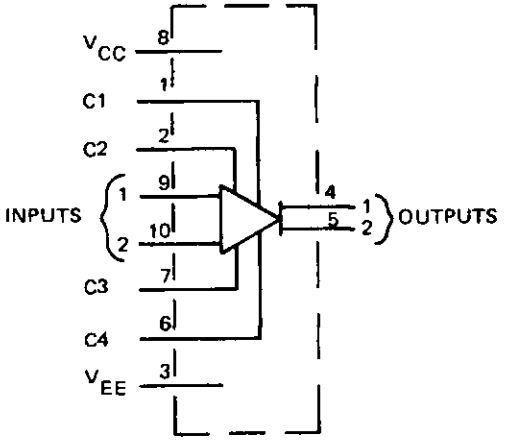
The 351-1050-030 is a wide-band general-purpose operational amplifier that features both differential inputs and outputs. Open loop gain is adjustable with external feedback components.

2.6 Quad Operational Amplifier 351-1141-030 (Refer to figure 6.)

The 351-1141-030 consists of four independent, high gain, internally frequency-compensated operational amplifiers that are designed to operate from a single power supply over a wide range of voltages. Common applications include transducer amplifiers, dc gain blocks, and all conventional operational amplifier circuits.

2.7 Dual Operational Amplifier 351-1071-070 (Refer to figure 7.)

The 351-1071-070 consists of two operational amplifiers in one package designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components.



CHARACTERISTICS

SUPPLY VOLTAGE: V_{CC} +8 V DC MAX., V_{EE} −8 V DC MAX.

INPUT DIFF VOLTAGE: ±8 V DC MAX.

INPUT COMMON MODE VOLTAGE: ±3.0 V PEAK

INPUT RESISTANCE: 2.0 M OHM TYPICAL

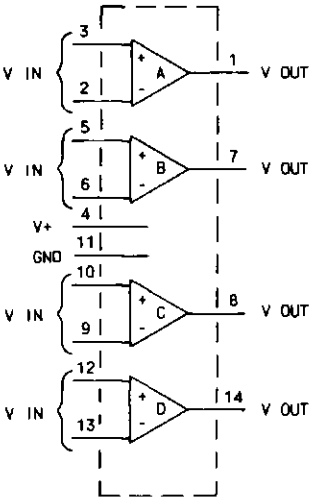
OUTPUT RESISTANCE: 50 OHM TYPICAL

OPEN LOOP GAIN: SINGLE ENDED– 750 V/V MIN, 1500 V/V TYPICAL; DIFFERENTIAL – 1500 V/V MIN,. 3000 V/V TYPICAL

BANDWIDTH: OPEN LOOP–2.0 MHz TYPICAL; CLOSED LOOP –10.0 MHz TYPICAL

TP5-2282-011

Differential Output Operational Amplifier 351-1050-030
Figure 5



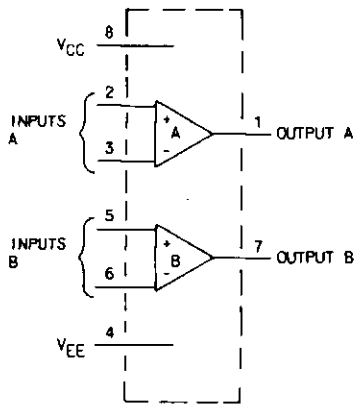
CHARACTERISTICS

SUPPLY VOLTAGE (V+): 32 V DC MAX
INPUT DIFF VOLTAGE: 32 V DC MAX
INPUT COMMON MODE VOLTAGE: V+ (-1.5 V DC)
OUTPUT SHORT CIRCUIT DURATION:
CONTINUOUS (1)
VOLTAGE GAIN: 25 MIN

NOTE:
(1) SUPPLY VOLTAGE EQUAL TO OR LESS THAN 15 V.

TP5-2289-013

Quad Operational Amplifier 351-1141-030
Figure 6



CHARACTERISTICS
SUPPLY VOLTAGE: V_{CC} +18 V DC MAX
V_{EE} -18 V DC MAX
INPUT DIFF VOLTAGE: ±30 V MAX
INPUT COMMON MODE VOLTAGE:
±15 V MAX (1)
OUTPUT SHORT CIRCUIT DURATION:
CONTINUOUS (2)
INPUT RESISTANCE: 300 kΩ MIN, 2.0 MΩ MAX
OUTPUT RESISTANCE: 75Ω TYPICAL
VOLTAGE GAIN: 15 MIN

NOTES:
(1) FOR SUPPLY VOLTAGE LESS THAN ±15.0 V, MAX INPUT VOLTAGE EQUAL TO SUPPLY VOLTAGE.
(2) SUPPLY VOLTAGE EQUAL TO OR LESS THAN 15 V.

TP5-2285-013

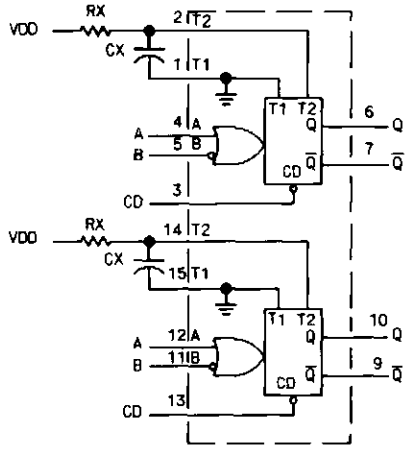
Dual Operatiumal Amplifier 351-1070-070
Figure 7

2.8 Dual Monostable Multivibrator 351-8278-010 (Refer to figure 8.)

The 351-8278-010 is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X.

2.9 Balanced Modulator-Demodulator 351-0043-020 (Refer to figure 9.)

The 351-0043-020 is designed for use where the output voltage is a product of an input voltage (signal) and a switching function carrier. Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications.



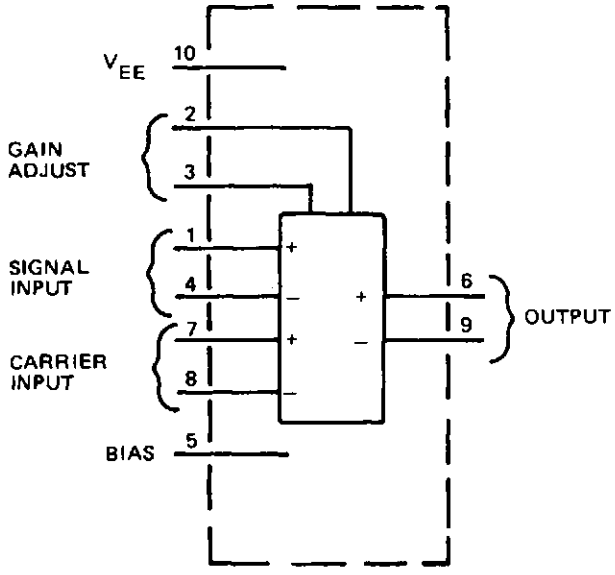
NOTE:
RX AND CX ARE EXTERNAL COMPONENTS.

CHARACTERISTICS:
SUPPLY VOLTAGE (VDD): -0.5 TO +18 V DC.
INPUT VOLTAGE: EQUAL TO VDD, MAX.

CHARACTERISTIC		VDD 5.0 V DC	10.0 V DC	15.0 V DC
OUTPUT VOLTAGE	"0"	0.05 V DC MAX.	0.05 V DC MAX.	0.05 V DC MAX.
	"1"	4.95 V DC MIN.	9.95 V DC MIN.	14.95 V DC MIN.
INPUT VOLTAGE	"0"	2.25 V DC MAX.	4.50 V DC MAX.	6.75 V DC MAX.
	"1"	2.75 V DC MIN.	5.50 V DC MIN.	8.25 V DC MIN.
EXTERNAL TIMING	RX	1000 Ω MIN.	1000 Ω MIN.	1000 Ω MIN.
	CX	NO LIMITS	NO LIMITS	NO LIMITS

TP5-2290-013

Dual Monostable Multivibrator 351-8278-010
Figure 8



CHARACTERISTICS

APPLIED VOLTAGE: 30 V DC MAX PIN–TO–IN.

DIFFERENTIAL INPUT VOLTAGE: ±5 V DC MAX

CARRIER SUPPRESSION: 65 dB TYPICAL AT 0.5 MHz; 50 dB TYPICAL AT 10 MHz.

TRANSADMITTANCE BANDWIDTH:
CARRIER INPUT–300 MHz TYPICAL;
SIGNAL INPUT–80 MHz TYPICAL

SINGLE-ENDED INPUT RESISTANCE (SIGNAL INPUT): 200 k OHM TYPICAL (AT 5.0 MHz)

SINGLE-ENDED INPUT RESISTANCE (SIGNAL INPUT): 40 k OHM TYPICAL (AT 10 MHz)

DIFFERENTIAL OUTPUT VOLTAGE SWING:
8.0 V P–P TYPICAL

TP5-2291-011

Balanced Modulator-Demodulator 351-0043-020
Figure 9

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the channel A if card are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 1 check total performance of the channel A if card. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

Note

In emergencies, Channel A IF 637-2650-( ) can be replaced by Channel A IF 635-0819-( ). In this type of repair, use the test procedures given in table 1 to test Channel A IF 635-0819-( ).

Table 1. Channel A IF, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of unit containing the channel A if that is to be tested.		
	b. Remove channel A if. Install it on an extender card and place it in the unit.		
	c. Set unit LINE SELECTOR switch to 115 V.		
	d. Connect unit to 115-V ac power source and set power on.		
	e. Measure dc voltages between the following pins and ground (TP1, brown):		
	P1-23 and P1-51	+15 ±1.0 V dc	Check associated power supply.
	P1-27	+5 ±0.5 V dc	
	P1-6	-15 ±1.0 V dc	
2. FL1 (USB) filter enable	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to A.		
	b. Measure dc voltage at TP2 to ground.	-9.5 ±1.0 V dc	Proceed to step n.
	c. Set front panel BANDWIDTH switch to USB.		
	d. Measure dc voltage at TP2 to ground.	NMT 0.5 V dc	Proceed to step o.
	e. Set front panel MODE switch to ISB.		
	f. Measure dc voltage at TP2 to ground.	NMT 0.5 V dc	Proceed to step p.
	g. Set front panel MODE switch to AM and BANDWIDTH switch to A.		
	h. Measure dc voltage at TP2 to ground.	-9.5 ±1.0 V dc	Proceed to step q.
	i. Connect a 4700-Ω resistor between P1-41 and +5 V dc.		
	j. Measure dc voltage at TP2 to ground.	NMT 0.5 V dc	Proceed to step r.
	k. Set front panel MODE switch to SSB/CW.		
	l. Measure dc voltage at TP2 to ground.	-9.5 ±1.0 V dc	Proceed to step s.
	m. Remove 4700-Ω resistor from P1-41 and +5 V dc.		
(Cont)	FL1 (USB) FILTER ENABLE TESTING COMPLETE		

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	TROUBLESHOOTING		
	n. Measure dc voltages at the following pins:		
	P1-14	NMT 0.5 V dc	Check FL1 (USB) input circuit.
	P1-35	NMT 0.5 V dc	Check AM enable input circuit.
	P1-41	NMT 0.5 V dc	Check rf transmit input circuit.
	P1-44	NMT 0.5 V dc	Check ISB enable input circuit.
		If voltages in step n are all normal, check U7, U8, U10, Q32, and associated circuit.	
	o. Measure dc voltage at P1-14.	NLT +3.0 V dc. Check U10, Q32, and associated circuit.	Check FL1 (USB) input circuit.
	p. Measure dc voltage at P1-44.	NLT +3.0 V dc. Check U10, Q32, and associated circuit.	Check ISB enable input circuit.
	q. Measure dc voltages at the following pins:		
	P1-14	NMT 0.5 V dc	Check FL1 (USB) input circuit.
	P1-35	NLT +3.0 V dc	Check AM enable input circuit.
	P1-41	NMT 0.5 V dc	Check rf transmit input circuit.
	P1-45	NMT 0.5 V dc	Check ISB enable input circuit.
		If voltages in step q are all normal, check U7, U8, U10, Q32, and associated circuit.	
	r. Measure dc voltage at P1-35.	NLT +3.0 V dc. If voltage is normal, check U7, U8, U10, Q32, and associated circuit.	Check AM enable input circuit.
(Cont)			

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	s. Measure dc voltages at the following pins:		
	P1-14	NMT 0.5 V dc	Check FL1 (USB) input circuit.
	P1-35	NMT 0.5 V dc	Check AM enable input circuit.
	P1-41	NLT +3.0 V dc	Check rf transmit input circuit.
	P1-45	NMT 0.5 V dc	Check ISB enable input circuit.
		If voltages in step s are all normal, check U7, U8, U10, Q32 and associated circuit.	
3. FL3 (A) filter enable	***Note***		
	With channel A if strapped 1-4, perform steps a thru d.		
	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to 16.		
	b. Measure dc voltage at J10-4.	NMT 0.5 V dc	Proceed to step k.
	c. Set BANDWIDTH switch to A.		
	d. Measure dc voltage at J10-4.	NLT +3.0 V dc	Proceed to step l.
	Note		
	With channel A if strapped 3-4, perform steps e thru j.		
	e. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to 16.		
	f. Measure dc voltage at J10-4.	NMT 0.5 V dc	Proceed to step m.
	g. Set MODE switch to AM.		
	h. Measure dc voltage at J10-4.	NLT +3.0 V dc	Proceed to step n.
	i. Apply +4.0-V dc signal to P1-41.		
	j. Measure dc voltage at J10-4.	NMT 0.5 V dc	Check U8, U7, and associated circuit.
(Cont)	FL3 (A) FILTER ENABLE TESTING COMPLETE		

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	TROUBLESHOOTING		
	k. Measure dc voltage at P1-15.	NMT 0.5 V dc. Check that a strap is installed from 1 to 4, and that no other strap is attached to 4.	Check FL3 (A) input circuit.
	l. Measure dc voltage at P1-15.	NLT +3.0 V dc. Check that a strap is installed from 1 to 4.	Check FL3 (A) input circuit.
	m. Measure dc voltage at P1-35.	NMT 0.5 V dc. Check U7, U8, and associated circuit. Check that a strap is installed from 3 to 4.	Check AM enable input circuit.
	n. Measure dc voltage at P1-35.	NLT +3.0 V dc. Proceed to step o.	Check AM enable input circuit.
	o. Measure dc voltage at P1-41.	NMT 0.5 V dc. Check U7, U8, and associated circuit. Check that a strap is installed from 3 to 4, and that no other strap is attached to 4.	Check rf transmit input circuit.
4. FL4 (B), FL5 (C), FL6 (D), and filter enable FL (E)	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to 16.		
	b. Measure dc voltage at each of the following pins:		
	J8-2	NMT 0.5 V dc	Proceed to step k.
	J8-3	NMT 0.5 V dc	
	J8-5	NMT 0.5 V dc	
	J8-4	NMT 0.5 V dc	
	c. Set BANDWIDTH switch to B.		
	d. Measure dc voltage at J8-2.	NLT +3.0 V dc	Proceed to step l.
	e. Set BANDWIDTH switch to C.		
	f. Measure dc voltage at J8-3.	NLT +3.0 V dc	Proceed to step m.
	g. Set BANDWIDTH switch to D.		
(Cont)	h. Measure dc voltage at J8-5.	NLT +3.0 V dc	Proceed to step n.

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	i. Set BANDWIDTH switch to E.		
	j. Measure dc voltage at J8-4.	NLT +3.0 V dc	Proceed to step o.
	FL4 (B), FL5 (C), FL6 (D), AND FL7 (E) FILTER ENABLE TESTING COMPLETE		
	TROUBLESHOOTING		
	k. Measure dc voltage at each of the following pins:		
	P1-43	NMT 0.5 V dc	Check FL4 (B) input circuit.
	P1-16	NMT 0.5 V dc	Check FL5 (C) input circuit.
	P1-45	NMT 0.5 V dc	Check FL6 (D) input circuit.
	P1-17	NMT 0.5 V dc	Check FL7 (E) input circuit.
		If the above voltages are normal and those in step b are not, check card for shorts.	
	l. Measure dc voltage at P1-43.	NLT +3.0 V dc. Check card for open circuit between P1-43 and J8-2.	Check FL4 (B) input circuit.
	m. Measure dc voltage at P1-16.	NLT +3.0 V dc. Check card for open circuit between P1-16 and J8-3.	Check FL5 (C) input circuit.
	n. Measure dc voltage at P1-45.	NLT +3.0 V dc. Check card for open circuit between P1-45 and J8-5.	Check FL6 (D) input circuit.
	o. Measure dc voltage at P1-17.	NLT +3.0 V dc. Check card for open circuit between P1-17 and J8-4.	Check FL7 (E) input circuit.
5. FL8 (16 kHz) filter enable	***Note*** With channel A if strapped 6-8, perform steps a thru d.		
	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to B.		
	b. Measure dc voltage at TP4 to ground.	-9.5 ±1.0 V dc	Proceed to step q.
(Cont)	c. Set BANDWIDTH switch to 16.		

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	d. Measure dc voltage at TP4 to ground.	NMT 0.5 V dc	Proceed to step r.
	Note With channel A if strapped 6-7, perform steps e thru i.		
	e. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to B.		
	f. Measure dc voltage at TP4 to ground.	-9.5 ±1.0 V dc	Proceed to step s.
	g. Apply +5.0 V dc at P1-38.		
	h. Measure dc voltage at TP4 to ground.	NMT 0.5 V dc	Check U10, Q33, and associated circuit. Check that a strap is installed from 6 to 7.
	i. Remove +5.0 V dc from P1-38.		
	Note With channel A if strapped 2-3, perform steps j thru p.		
	j. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to B.		
	k. Measure dc voltage at TP4 to ground.	-9.5 ±1.0 V dc	Proceed to step t.
	l. Set front panel MODE switch to AM.		
	m. Measure dc voltage at TP4 to ground.	NMT 0.5 V dc	Proceed to step u.
	n. Apply +5.0 V dc at P1-41.		
	o. Measure dc voltage at TP4 to ground.	-9.5 ±1.0 V dc.	Check U7, U8, U10, Q33, and associated circuit.
	p. Remove +5.0 V dc from P1-41.		
	FL8 (16 kHz) FILTER ENABLE TESTING COMPLETE		
	TROUBLESHOOTING		
	q. Measure dc voltage at P1-46.	NMT 0.5 V dc. Check U10, Q33, and associated circuit. Check that a strap is installed from 6 to 8 and that no other strap is attached to 6.	Check FL8 (16 kHz) input circuit.
(Cont)			

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	r. Measure dc voltage at P1-46.	NLT +3.0 V dc. Check U10, Q33, and associated circuit. Check that a strap is installed from 6 to 8.	Check FL8 (16 kHz) input circuit.
	s. Measure dc voltage at P1-38.	NMT 0.5 V dc. Check U10, Q33, and associated circuit. Check that a strap is installed from 6 to 7 and that no other strap is attached to 6.	Check CW mode input circuit.
	t. Measure dc voltage at P1-35.	NMT 0.5 V dc. Check U7, U8, U10, Q33, and associated circuit. Check that a strap is installed from 2 to 3 and that no other strap is attached to 2.	Check AM enable input circuit.
	u. Measure dc voltage at P1-35.	NLT +3.0 V dc. Proceed to step v.	Check AM enable input circuit.
	v. Measure dc voltage at P1-41.	NMT 0.5 V dc. Check U7, U8, U10, Q33, and associated circuit. Check that a strap is installed from 2 to 3.	Check rf transmit input circuit.
6. CW mode enable	***Note*** With channel A if strapped 5-7, perform steps a thru d.		
	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to 16.		
	b. Measure dc voltage at J8-1.	NMT 0.5 V dc	Proceed to step e.
	c. Apply +5.0 V dc to P1-38.		
	d. Measure dc voltage at J8-1.	NLT +3.0 V dc	Check CW mode circuit. Check that strap is installed from 5 to 7 and that no other strap is attached to 5.
(Cont)	CW MODE ENABLE TESTING COMPLETE		

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
6. (Cont)	TROUBLESHOOTING		
	e. Measure dc voltage at P1-38.	NMT 0.5 V dc. Check CW mode circuit. Check that strap is installed from 5 to 7 and that no other strap is attached to 5.	Check CW mode input circuit.
7. Filter card interface	a. Set power off.		
	b. Measure resistance between each of the following pins and ground (TP1, brown): J8-6 J8-7 J9-5 J9-6 J10-2 J10-5	NMT 3 Ω each pin	Repair circuit connections.
	c. Measure resistance between the following pins: J10-1 to J1 J9-1 to J4	NMT 3 Ω each pin	
	d. Set power on.		
	e. Measure dc voltage between each of the following pins and ground (TP1, brown):		
	J9-2	-9.5 ±0.5 V dc	Check VR5 and associated circuit.
	J9-4	+14.5 ±0.5 V dc	Check R157 and associated circuits.
	f. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.		
	g. Apply a 9.4483-MHz, 20-mV signal (measured) to J2.		
	h. Using an rf voltmeter (with high impedance probe), measure gain from J2 to J1.	≅ 3 to 1	Check J10-1 and associated input circuit.
	i. Using an rf voltmeter, measure voltage gain from J1 to J4.	8.2 ±2.0 dB	Check J9-1 and associated filter circuit.
8. 2.75-kHz USB filter measurement (Cont)	*Note* This test applies only to 2.75-kHz USB filter (526-9955-010).		

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
8. (Cont)	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.		
	b. Set AGC switch to OFF.		
	c. Set receive input at J2 for 9.4483 MHz.		
	d. Using an rf voltmeter (with high impedance probe), measure rf voltage at J4. Adjust receive input level and frequency for a 70-mV peak reading at J4.	Reference	
	e. Adjust input frequency down until rf voltage at J4 is 3 dB below level of step d. Note input frequency.	NMT 9.447 000 MHz	Check FL1, Q4, Q8, and associated circuit.
	f. Adjust input frequency up until rf voltage at J4 is 3 dB below level of step d. Note input frequency.	NLT 9.449 750 MHz	Check FL1, Q4, Q8, and associated circuit.
8A. 3.05-kHz USB filter measurement	**Note** This test applies only to 3.05-kHz USB filter (526-9980-010).		
	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.		
	b. Set AGC switch to OFF.		
	c. Set receive input at J2 for 9.4482 MHz.		
	d. Using an rf voltmeter (with high impedance probe), measure rf voltage at J4. Adjust receive input level and frequency for a 70-mV peak reading at J4.	Reference	
	e. Adjust input frequency down until rf voltage at J4 is 3 dB below level of step d. Note input frequency.	NMT 9.446 700 MHz	Check FL1, Q4, Q8, and associated circuit.
	f. Adjust input frequency up until rf voltage at J4 is 3 dB below level of step d. Note input frequency.	NLT 9.449 750 MHz	Check FL1, Q4, Q8, and associated circuit.
8B. 3.10-kHz USB filter measurement	**Note** This test applies only to 3.10-kHz USB filter (526-9985-010).		
	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.		
	b. Set AGC switch to OFF.		
(Cont)	c. Set receive input at J2 for 9.4482 MHz.		

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
8B. (Cont)	d. Using an rf voltmeter (with high impedance probe), measure rf voltage at J4. Adjust receive input level and frequency for a 70-mV peak reading at J4.	Reference	
	e. Adjust input frequency down until rf voltage at J4 is 3 dB below level of step d. Note input frequency.	NMT 9.446 600 MHz	Check FL1, Q4, Q8, and associated circuit.
	f. Adjust input frequency up until rf voltage at J4 is 3 dB below level of step d. Note input frequency.	NLT 9.449 700 MHz	Check FL1, Q4, Q8, and associated circuit.
8C. 5.80-kHz USB filter measurement	**Note** This test applies only to 5.80-kHz USB filter (526-9976-010).		
	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.		
	b. Set AGC switch to OFF.		
	c. Set receive input at J2 for 9.4459 MHz.		
	d. Using an rf voltmeter (with high impedance probe), measure rf voltage at J4. Adjust receive input level and frequency for a 70-mV peak reading at J4.	Reference	
	e. Adjust input frequency down until rf voltage at J4 is 3 dB below level of step d. Note input frequency.	NMT 9.444 000 MHz	Check FL1, Q4, Q8, and associated circuit.
	f. Adjust input frequency up until rf voltage at J4 is 3 dB below level of step d. Note input frequency.	NLT 9.449 800 MHz	Check FL1, Q4, Q8, and associated circuit.
9. AGC attack and decay times	a. Set receive input at J2 to 9.4483 MHz at 1 mV at output of switching device. Set the switching device for 0.25 s on and 2.5 s off.		
	Note If a switching device is not available, one may be fabricated using figure 10.		
	b. Set front panel AGC switch to FAST.		
(Cont)	c. Using an oscilloscope, measure AGC attack time at Q18-C.	NMT 5 ms	

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
9. (Cont)	**Note** AGC attack time is the time interval from the first appearance of an rf burst to the point where the rf envelope stays within 6 dB of the final value.		
	d. Set receive input at J2 to 9.4483 MHz at 200 μV at output of switching device. Set the switching device to alternate between a 200- and a 10-μV output.		
	e. Using an oscilloscope, measure AGC decay time at Q18-C.	75 to 200 ms	Check Q29, Q30, U3, and associated circuits.
(Cont)	**Note** AGC decay time is the time interval from the 200- to 10-μV transition		

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
9. (Cont)	and the point when the rf envelope reaches 70% of the final value.		
	f. Repeat steps d and e with the front panel AGC switch at SLOW.	1 to 2 s	Check U3 and associated circuits.
10. 450-kHz injection frequency suppression	a. Set receive input at J2 to 9.4483 MHz at 1000 μV.		
	b. Set AGC switch to FAST.		
	c. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.		
	d. Using a spectrum analyzer, measure the desired if out at J6 (CH A IF jack on rear panel).	Note level.	
	e. Measure the 450-kHz injection frequency leakage at the receive if out jack J6 (CH A IF jack on rear panel).	NLT 40 dB down from receive if above **Note** It may be necessary to remove the receive input to locate the 450-kHz leakage. Measure if with the receiver input applied.	Check U6, Q2, and associated circuit.
11. Receive audio distortion	a. Set receive input at J2 to 9.4483 MHz at 500 μV.		
	b. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.		
	c. Using an audio distortion analyzer, measure the audio distortion at RCV AF 600 Ω - A on rear panel (TB1-1, -3).	NMT 0.5%	Check U14, U1, U2, Q14, Q17, Q18, and associated circuits.
12. AGC range	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.		
	b. Set AGC switch to FAST.		
	c. Set receive input at J2 to 9.4483 MHz at 0 μV.		
	d. Connect dvm to P1-21.		
	e. Increase receive input until dvm just begins to increase from 70 mV dc.	Note input level at this point. (Nominally 5 μV rms)	
(Cont)	f. Using an rf voltmeter, note rf level at J6 (CH A IF jack on rear panel).	Reference	

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
12. (Cont)	g. Increase receive input 80 dB higher than the input level noted in step e.		
	h. Note the rf level at J6 (CH A IF jack on rear panel) and that no sign of an overload exists on Q18-C.	NMT 6 dB above that noted in step f. No overload on Q18-C.	Check U1, U2, and associated circuits.
13. Remote rf gain	**Note** This test applies only to unit with a remote control connected.		
	a. Set receive input at J2 to 9.4483 MHz at 5 μV.		
	b. Set front panel CONT switch to REM.		
	c. Set remote control MODE switch to SSB/CW and BANDWIDTH switch to USB.	Reference if output level at J6 (CH A IF jack on rear panel).	
	d. Set remote control AGC switch off.		
	e. Adjust remote control RF GAIN control full counterclockwise. Increase receive input at J2 until if output level equals reference of step c.	Total attenuation over RF GAIN control range 80 dB minimum.	Check U3 and associated circuits.
	f. Set receive input for 60 dB above 5-μV input. Adjust remote control RF GAIN control until if output level equals reference of step c.		
	g. Note the input at P1-11.	-5.0 ±0.1 V dc	Same as step c.
	h. Set front panel CONT switch to LCL.		
14. Local rf gain	a. Set receive input at J2 to 9.4483 MHz at 5 μV.		
	b. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.	Reference if output level at J6 (CH A IF jack on rear panel).	
	c. Set front panel AGC switch to OFF.		
	d. Adjust front panel RF GAIN control full counterclockwise. Increase receive input at J2 until if output level equals reference of step b.	Total attenuation over RF GAIN control range 80 dB minimum.	Check U3 and associated circuits.
	e. Set receive input for 60 dB above 5-μV input. Adjust RF GAIN control until if output level equals reference of step b.		
	f. Note the input at P1-39.	+2.8 ±0.3 V dc	Same as step d.

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

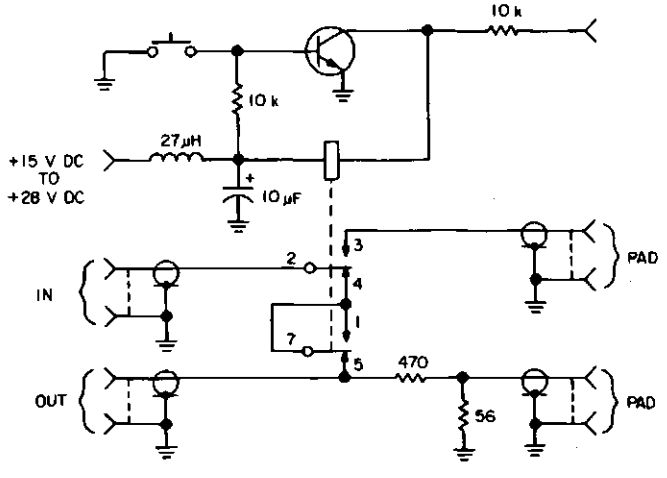
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
15. AGC in/out	a. Set the front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.		
	b. Set front panel AGC switch to FAST.		
	c. Set receive input at J2 to 9.4483 MHz at 5 μV.		
	d. Check the AGC in/out voltage at P1-21 with this input applied.	≃ 70 mV dc	Check U3B and associated circuits.
	e. Increase the receive input at J2 by 80 dB.		
	f. Check the AGC in/out voltage at P1-21 with this input applied.	7.8 ±0.8 V dc	Same as step d
16. RF AGC	a. Set the front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.		
	b. Set front panel AGC switch to FAST.		
	c. Set receive input at J2 to 9.4483 MHz at 5 μV.	Reference	
	d. Using a dvm, monitor the rf AGC voltage at P1-18.		
	e. Adjust front panel RF GAIN control for 0 V dc at P1-18.		
	f. Note the rf AGC voltage while slowly increasing the receive input to 80 dB above level in step c.	Rf AGC increases at a constant rate from 0 to 3 V dc. (60-dB point = NLT 3.0 V dc)	Check Q19, U3A, U3B, and associated circuits.
17. Mute	a. Set the front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.		
	b. Set receive input at J2 to 9.4483 MHz at 50 μV.		
	c. Using an rf voltmeter, monitor the if output at J6 (CH A IF jack on rear panel).	Output signal is present.	Check U1, U2, and associated circuits.
	d. Apply a ground at P1-13.	Output signal is muted.	Check Q10 thru Q13 and associated circuits.
	e. Remove P1-13 ground.	Output signal is restored.	

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
18. Performance monitor	a. Set the front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.		
	b. Set receive input at J2 to 9.4483 MHz at 50 μV.		
	c. Using a dvm, measure the dc voltage at P1-2.	0.5 ±0.5 V dc	Check Q25 and associated circuit.
	d. Remove receive input and measure the dc voltage at P1-2.	+4.5 ±0.5 V dc	Same as step c.
19. AGC meter voltage	a. Set the front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.		
	b. Set receive input at J2 to 9.4483 MHz at 5 μV.		
	c. Using a dvm, measure the dc voltage at P1-12.	0.5 ±0.5 V dc (with front panel METER switch at any position other than RCV SIG)	Check U3A, U3B, and associated circuits.
	d. Increase the receive input voltage and verify that the dc voltage at P1-12 increases.	Increased voltage	
20. Crowbar enable	a. Set the front panel CONT switch to REM.		
	b. Apply +5 V dc to P1-37.		
	c. Using an oscilloscope, monitor the waveform at U5-7.	NLT +3.0 V dc	Check U5 and associated circuits.
	d. Note dc level and duration of U5-7 pulse while slowly changing the remote control frequency settings.	0.5 ±0.5 V dc for 20 ±10 ms between each frequency change	Same as step b.
	e. Using an oscilloscope, monitor the waveform at P1-18.	During the logic 0 pulse, waveform at P1-18 shall be 0.5 ±0.5 V dc.	Check Q29 and associated circuit.
	f. Remove +5 V dc from P1-37.		
	g. Set the front panel CONT switch to LCL.		
21. AM audio	a. Set front panel MODE switch to AM and BANDWIDTH switch to 16.		
	b. Set receive input at J2 to 9.4500 MHz at 500 μV, AM modulated at 1000 Hz and 50%.		
	c. Using an audio distortion analyzer, measure the audio signal level at P1-8 (A6TP2) and the audio distortion at RCV AF 600 Ω-A on rear panel (TB1-1, -3).	Output: 10 ±2 mV. Distortion NMT 3.0%.	Check Q21 and associated circuits.

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
22. Sensitivity	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.		
	b. Set AGC switch to OFF.		
	c. Using an audio voltmeter, monitor the audio at P1-34 (A6TP2) (with no receive input).	Reference	
	d. Set receive input at J2 to 9.4483 MHz.		
	e. Adjust receive input for +10 dB (s+n)/n at P1-34 (A6TP2).		
	f. Note the receive input level.	NMT 1 μV rms (into 50-Ω, 2-μV rms open circuit)	Check U1, U2, and associated circuits.
23. If output	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.		
	b. Set receive input at J2 to 9.4483 MHz at 15 μV.		
	c. Set front panel AGC switch to FAST.		
	d. Using an rf voltmeter, measure the receive if output at J6 (CH A IF jack on rear panel).	27 ±10 mV rms	Check Q15, Q16, and associated circuits.



TPA-1345-013

AGC Switching Device
Figure 10

4. ALIGNMENT/ADJUSTMENT

4.1 Input Strapping

Inputs to FL3 and FL8 are strapped as required for special applications. FL3(A) through FL7(E) bandpass filters are located on piggyback filter board A8A2 if used. Refer to table 2 for input-strap-filter relationships.

Table 2. Input Strapping.

INPUT	STRAP	FILTER
FL3 (A) (P1-15)	1-4	FL3 (A) (J10-4)
FL8 (P1-46)	8-6	FL8 (16 kHz)

4.2 Filter Amplifier Gain Adjustments (Adjustment of R6 and Selection of R49, R56, R94, and R97)

a. Set front panel MODE switch to SSB/CW and the BANDWIDTH switch to USB. Set AGC switch to FAST.
b. Measure signal level at J1 with no receive input signal (9.9 MHz from Q5 mixer). Adjust R6 for a signal null at J1.
c. Connect receive input of 9.4483 MHz to J2. Measure gain from J2 to J1. Should be ≅3 to 1. (Receive input must be set higher than 9.9-MHz leakage.)

Note

Perform step d only if FL1, Q8, and/or Q9 circuits have been repaired.

d. Set receive signal to 50 μV (9.4483 MHz). Find a passband response minimum between 9.4493 and 9.4489 MHz at J4. Measure voltage gain between J1 and J4. Should be 8.2 ±2.0 dB. Select values of R94 and R97 (200 through 1000 Ω) to give a voltage gain of 8.2 ±2.0 dB.
e. Set front panel MODE switch to AM and the BANDWIDTH switch to 16.

Note

Perform step f only if Q6 and/or Q7 circuits have been repaired.

f. Find a passband response minimum between 9.4493 and 9.4489 MHz at J4. Measure voltage gain between J1 and J4. Should be 8.2 ±2.0 dB. Select values of R49 and R56 (200 through 1000 Ω) to give a voltage gain of 8.2 ±2.0 dB.

4.3 Receive Gain Adjustment (Adjustment of C5, C8, L10, L13, R78, and R143)

a. Set front panel MODE switch to SSB/CW and the BANDWIDTH switch to USB. Adjust R78 for minimum gain (full ccw). Increase receive input until AGC voltage (measured at P1-21) increases to about +1.0 V dc.
b. Adjust C5, C8, L10, and L13 for a peak AGC voltage. Decrease the receive input as necessary to maintain AGC voltage at about +1.0 V dc.
c. Repeat step b until no further increase in peak AGC voltage is possible.
d. Set the receive input to 5.0 μV (9.4483 MHz) and adjust R78 for +70 ±5 mV dc AGC voltage (measured at P1-21).
e. Increase receive input to 5.0 mV (9.4483 MHz) and adjust R143 until AGC voltage (measured at P1-21) equals +5.0 ±0.1 V dc.
f. Repeat steps d and e until no further improvement is possible.

4.4 SSB Output Level Adjustment (Adjustment of R262)

a. Set front panel MODE switch to SSB/CW and the BANDWIDTH switch to USB.
b. Set receive input for 15.0 μV (9.4483 MHz) and adjust R262 for 10 ±0.5-mV rms audio output (measured at P1-34).

4.5 AGC Meter Level Adjustment (Adjustment of R132)

AGC meter level adjustment is made at the unit level for the level required by the associated meter circuit.

5. REPAIR

Repair of the channel A if card is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

This paragraph assists in identification, requisition, and issuance of parts and in maintenance of equipment. A parts location illustration, schematic

diagram, parts list tabulation, and modification history are included in the schematic diagram (figures 11 and 12). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

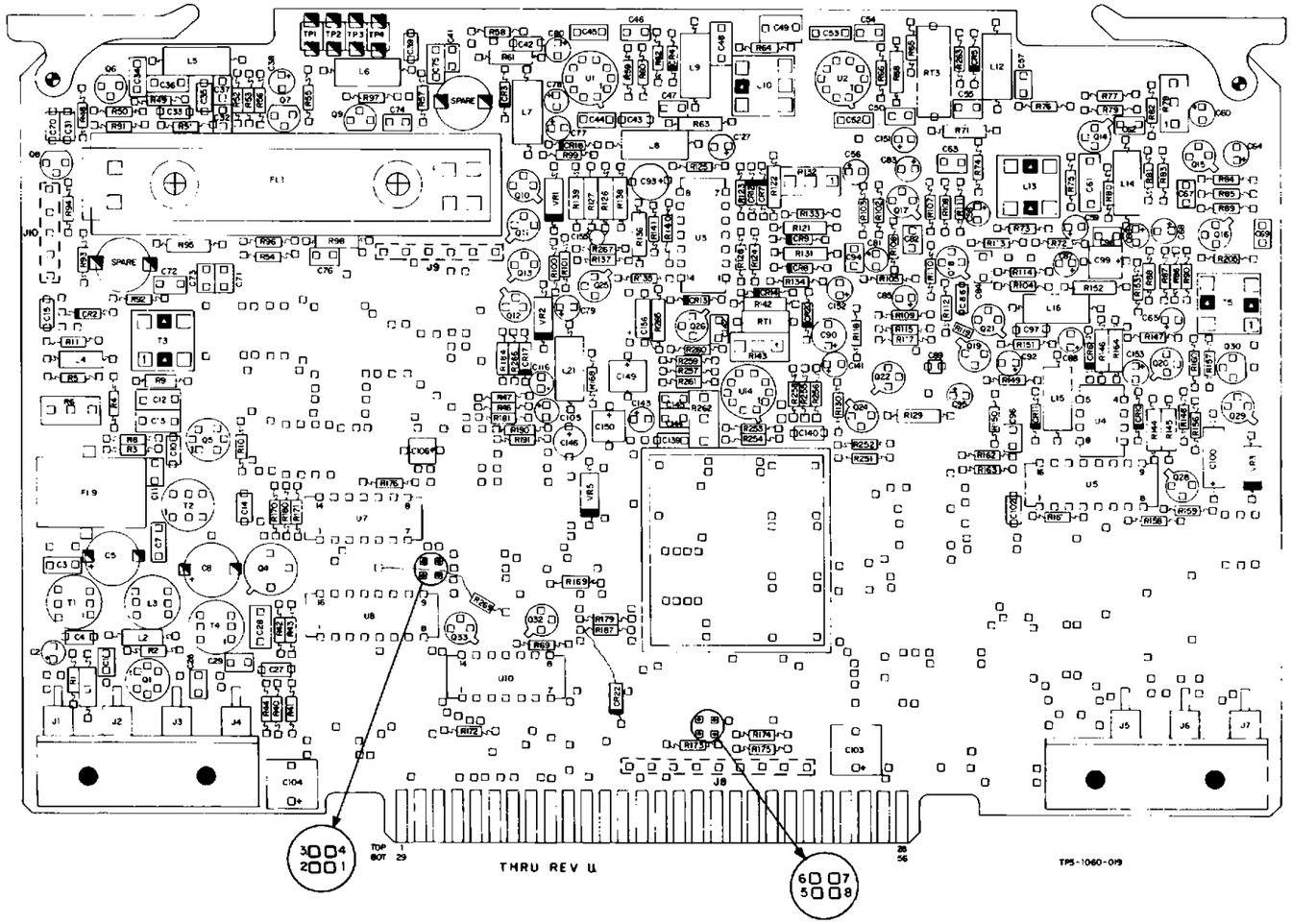
Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Channel A if	637-2650-001	REV AD
Channel A if	637-2650-002	REV AD
Channel A if	637-2650-003	REV AC
Channel A if	637-2650-004	*
Channel A if	637-2650-005	*

*Not covered in this printing.



Channel A IF, Through REV AC, Schematic Diagram
Figure 11 (Sheet 1 of 5)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
	CHANNEL A IF A8	637-2650-001	A
	CHANNEL A IF A8	637-2650-002	B
	CHANNEL A IF A6	637-2650-003	C
CR1	NOT USED		
CR2	SEMICOND DEVICE 1N4454	353-3644-010	
CR3-CR5	SEMICOND DEVICE 1N5767	922-6119-010	
CR6-CR8	SEMICOND DEVICE 1N4454	353-3644-010	
CR9	SEMICOND DEVICE 1N4454 (A1)	353-3644-010	
CR10-	SEMICOND DEVICE 1N4454	353-3644-010	
CR14			
CR15,	NOT USED		
CR16			
CR17	SEMICOND DEVICE 1N4454 (A7)	353-3644-010	
CR18	SEMICOND DEVICE 1N816 (A2)	353-2564-000	
CR18	SEMICOND DEVICE 1N5767	922-6119-010	
CR19	NOT USED		
CR20	SEMICOND DEVICE 1N4454	353-3644-010	
CR21	NOT USED		
CR22	SEMICOND DEVICE 1N4454 (A2)	353-3644-010	
C1	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C2	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A12)	184-9102-290	
C2	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C3	CAPACITOR,FXD MICA DIEL, 20PF, PORM 0.5PF, 100V	912-4141-150	
C4	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C5	CAPACITOR,VAR CER DIEL, 9 TO 35PF, 200V	917-1225-000	
C6	NOT USED		
C7	CAPACITOR,FXD MICA DIEL, 47PF, 5%, 50V (A5)	912-4141-280	
C7	CAPACITOR,FXD MICA DIEL, 68PF, 5%, 50V	912-4141-330	
C8	CAPACITOR,VAR CER DIEL, 9 TO 35PF, 200V	917-1225-000	
C9	NOT USED		
C10	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C11	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-180	
C12,C13	CAPACITOR,FXD CER DIEL, 2200PF, 5%, 100V	913-3281-300	
C14	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V (B1)	913-5019-200	
C14	CAPACITOR,FXD CER DIEL, 470PF, 10%, 200V	913-4014-000	
C15	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V (A5)	913-5019-200	
C15	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V (A8)	184-9102-350	
C15	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C16-C25	NOT USED		
C26	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C27	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C28	CAPACITOR,FXD CER DIEL, 120PF, 10%, 100V	913-3281-310	
C29	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V (A5)	913-3279-110	
C29	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C30	NOT USED		
C31	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C32	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C33	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V (A2)	913-5019-200	
C33	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C34	CAPACITOR,FXD MICA DIEL, 24PF, PORM 0.5PF, 50V	912-4141-160	
C35	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C36	CAPACITOR,FXD MICA DIEL, 24PF, PORM 0.5PF, 50V	912-4141-160	
C37	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C38	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C39	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C40	NOT USED		
C41-C43	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C44,C45	CAPACITOR,FXD MICA DIEL, 4PF, PORM 0.5PF, 300V	912-4141-080	
C46,C47	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C48	CAPACITOR,FXD CER DIEL, 1200PF, 5%, 100V	913-3281-290	
C49	CAPACITOR,FXD MICA DIEL, 400PF, 5%, 50V	912-4141-520	
C50	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C51	NOT USED		
C52,C53	CAPACITOR,FXD MICA DIEL, 4PF, PORM 0.5PF, 300V	912-4141-080	
C54,C55	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C56	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A12)	184-9102-290	
C56	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C57	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C58,C59	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A12)	184-9102-290	
C58,C59	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C60	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C61	CAPACITOR,FXD CER DIEL, 5600PF, 5%, 100V	913-3281-380	
C62,C63	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C64	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C65	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V (A8)	184-9102-350	
C65	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C66	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A8)	184-9102-290	
C66	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C67	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C68	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V (A8)	184-9102-350	
C68	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C69	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C70	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C71	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C72	CAPACITOR,FXD MICA DIEL, 15PF, PORM 0.5PF, 300V (A4)	912-4141-130	
C72	CAPACITOR,FXD MICA DIEL, 18PF, PORM 0.5PF, 100V	912-4141-140	
C73	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V (A2)	913-3279-110	
C73	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C74	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
C75	CAPACITOR,FXD MICA DIEL, 20PF, PORM 0.5PF, 100V (A6)	912-4141-150	
C75	CAPACITOR,FXD MICA DIEL, 6PF, PORM 0.5PF, 300V	912-4141-090	
C76	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C77-C81	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A12)	184-9102-290	
C77-C81	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C82	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C83	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A12)	184-9102-290	
C83	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C84	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-180	
C85	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V (A8)	184-9102-350	
C85	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C86	CAPACITOR,FXD CER DIEL, 470PF, 10%, 200V	913-4014-000	
C87	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A12)	184-9102-290	
C87	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C88	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A12)	184-9102-290	
C88	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C89	CAPACITOR,FXD CER DIEL, 1000PF, 20%, 50V	913-3279-030	
C90	CAPACITOR,FXD ELCTLT, 22UF, 20%, 15V	184-9102-140	
C91	NOT USED		
C92	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C93	CAPACITOR,FXD ELCTLT, 47UF, 20%, 6V	184-9102-470	
C94	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C95	CAPACITOR,FXD ELCTLT, 6.8UF, 20%, 6V	184-9102-450	
C96	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-180	
C97	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C98	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C99	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-610	
C100	CAPACITOR,FXD ELCTLT, 4.7UF, 10%, 10V (A2)	184-9086-140	
C100	CAPACITOR,FXD ELCTLT, 2.2UF, 10%, 20V	184-9086-430	
C101	NOT USED		
C102	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A12)	184-9102-290	
C102	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C103,	CAPACITOR,FXD ELCTLT, 47UF, 20%, 20V	184-9102-630	
C104			
C105	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A12)	184-9102-290	
C105	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C106	CAPACITOR,FXD ELCTLT, 6.8UF, 20%, 6V (A9)	184-9102-450	
C107-	NOT USED		
C115			
C116	CAPACITOR,FXD ELCTLT, 1.5UF, 20%, 25V (A7)	184-9102-210	
C117-	NOT USED		
C126			
C127	CAPACITOR,FXD ELCTLT, 0.47UF, 20%, 35V	184-9102-330	
C128-	NOT USED		
C138			
C139,	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C140			
C141	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A12)	184-9102-290	
C141	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C142	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C143	CAPACITOR,FXD ELCTLT, 0.1UF, 20%, 35V (A12)	184-9102-290	
C143	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C144,	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V (A8)	913-3279-110	
C145			
C144,	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C145			
C146	CAPACITOR,FXD ELCTLT, 6.8UF, 20%, 25V	184-9102-670	
C147,	NOT USED		
C148			
C149	CAPACITOR,FXD ELCTLT, 22UF, 20%, 10V	184-9102-520	
C150	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-610	
C151	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C152	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V (A8)	184-9102-350	
C152	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C153	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C154	NOT USED		
C155	CAPACITOR,FXD ELCTLT, 47UF, 20%, 20V (A5)	184-9102-630	
C156	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V (A11)	184-9102-220	
FL1	FILTER,USB,2.75 KHZ	526-9955-010	A
FL1	FILTER,USB,3.05 KHZ	526-9980-010	B
FL1	FILTER,USB,3.10 KHZ	526-9985-010	C
FL2-FL8	NOT USED		
FL9	FILTER,XTAL,BP 9.45 MHZ	293-1319-010	
J1-J6	CONNECTOR,RCPT ELEC	357-7207-100	
J7	NOT USED		
J8	HOUSING,CONN	372-2625-018	
J9	HOUSING,CONN	372-2625-015	
J10	HOUSING,CONN	372-2625-014	
L1,L2	COIL,RF 100UH	240-2047-000	
L3	TRANSFORMER,RF	278-0430-040	
L4	COIL,RF 100UH	240-2047-000	
L5,L6	COIL,RF 1000UH	240-2715-490	
L7	COIL,RF 2700UH (B2)	240-2715-540	
L7	COIL,RF,5600UH	637-3767-001	
L8,L9	COIL,RF 1000UH	240-2715-490	
L10	INDUCTOR,RF VAR	242-0441-010	
L11	NOT USED		
L12	COIL,RF 1000UH	240-2715-490	
L13	INDUCTOR,RF VAR	242-0441-020	
L14	COIL,RF 1000UH	240-2715-490	
L15,L16	COIL,RF 8200UH	240-2715-600	

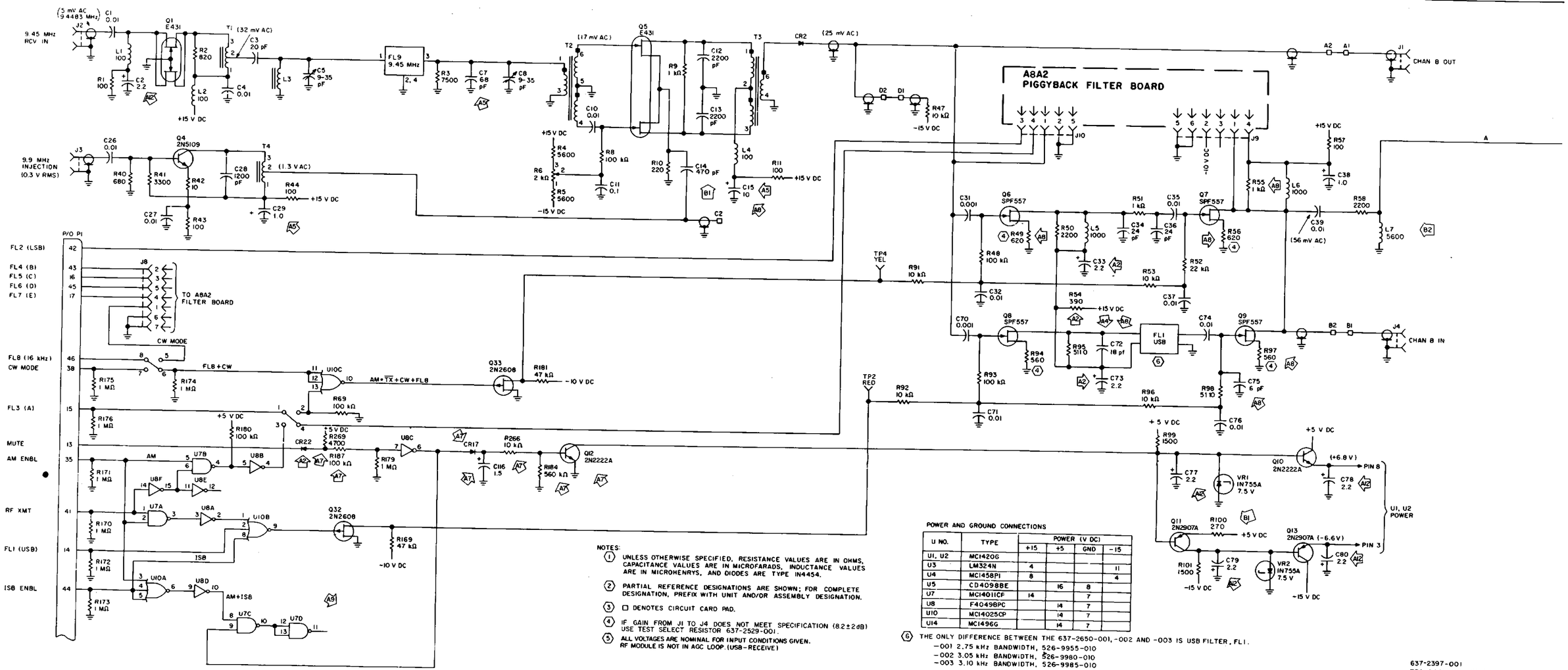
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
L17-L20	NOT USED		
L21	COIL,RF 1000UH	240-2715-490	
Q1	TRANSISTOR,FET E431	351-0194-010	
Q2,Q3	NOT USED		
Q4	TRANSISTOR 2N5109	352-0766-010	
Q5	TRANSISTOR,FET E431	351-0194-010	
Q6-Q9	TRANSISTOR SPF557	352-1068-010	
Q10	TRANSISTOR 2N2222A	352-0661-020	
Q11	TRANSISTOR 2N2907A	352-0551-010	
Q12	TRANSISTOR 2N2222A (A7)	352-0661-020	
Q13	TRANSISTOR 2N2907A	352-0551-010	
Q14-Q18	TRANSISTOR 2N2222A	352-0661-020	
Q19	TRANSISTOR 2N2907A	352-0551-010	
Q20	TRANSISTOR 2N2222A	352-0661-020	
Q21	TRANSISTOR 2N2222A (A6)	352-0661-020	
Q21	TRANSISTOR 2N2907A	352-0551-010	
Q22	TRANSISTOR 2N2907A	352-0551-010	
Q23	NOT USED		
Q24	TRANSISTOR 2N2608	352-0605-010	
Q25,Q26	TRANSISTOR 2N2222A	352-0661-020	
Q27	NOT USED		
Q28,Q29	TRANSISTOR 2N2907A	352-0551-010	
Q30	TRANSISTOR 2N2608	352-0605-010	
Q31	NOT USED		
Q32,Q33	TRANSISTOR 2N2608	352-0605-010	
RT1	RESISTOR,THRM 100K, 10%, 0.5W	714-1736-000	
RT2	NOT USED		
RT3	RESISTOR,THRM 3K, 10%, 1W	714-1715-000	
R1	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R2	RESISTOR,FXD CMPSN, 820 OHMS, 10%, 1/8W	745-2338-000	
R3	RESISTOR,FXD CMPSN, 7.5K, 5%, 1/8W	745-1863-700	
R4,R5	RESISTOR,FXD CMPSN, 5.6K, 10%, 1/8W	745-2368-000	
R6	RESISTOR,VAR NON-WW,2K, 10%	382-0052-440	
R7	NOT USED		
R8	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R9	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R10	RESISTOR,FXD CMPSN, 220 OHMS, 10%, 1/8W	745-2317-000	
R11	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R12-R39	NOT USED		
R40	RESISTOR,FXD CMPSN, 680 OHMS, 10%, 1/8W	745-2335-000	
R41	RESISTOR,FXD CMPSN, 3.3K, 10%, 1/8W	745-2359-000	
R42	RESISTOR,FXD CMPSN, 10 OHMS, 10%, 1/8W	745-2268-000	
R43,R44	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R45,R46	NOT USED		
R47	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R48	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R49	RESISTOR,FXD,CMPSN, 2000OHM THRU 7500HM,5%,1/8W (A8)	637-2529-000	
R49	RESISTOR,FXD CMPSN, 620 OHMS, 5%, 1/8W	745-1863-440	
R50	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/8W	745-2353-000	
R51	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R52	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R53	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R54	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W (A2)	745-2341-000	
R54	RESISTOR,FXD CMPSN, 390 OHMS, 10%, 1/8W	745-2326-000	
R55	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W (A8)	745-2341-000	
R55	RESISTOR,FXD CMPSN, 1K, 5%, 1/8W	745-1863-490	
R56	RESISTOR,FXD,CMPSN, 2000OHM THRU 7500HM,5%,1/8W (A8)	637-2529-000	
R56	RESISTOR,FXD CMPSN, 620 OHMS, 5%, 1/8W	745-1863-440	
R57	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R58	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/8W	745-2353-000	
R59	RESISTOR,FXD CMPSN, 18K, 10%, 1/8W	745-2396-000	
R60	RESISTOR,FXD CMPSN, 820 OHMS, 10%, 1/8W	745-2338-000	
R61	RESISTOR,FXD FILM, 20.5K, 1%, 1/8W	705-1059-000	
R62	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/8W	745-2353-000	
R63	RESISTOR,FXD FILM, 14.3K, 1%, 1/8W	705-3605-550	
R64	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R65	RESISTOR,FXD CMPSN, 680 OHMS, 10%, 1/8W	745-2335-000	
R66	RESISTOR,FXD CMPSN, 33K, 10%, 1/8W	745-2395-000	
R67	NOT USED		
R68	RESISTOR,FXD FILM, 1.40K, 1%, 1/8W	705-1003-000	
R69	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R70	NOT USED		
R71	RESISTOR,FXD FILM, 24.9K, 1%, 1/8W	705-1063-000	
R72	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/8W	745-2292-000	
R73	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R74	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R75	RESISTOR,FXD CMPSN, 1.2K, 10%, 1/8W	745-2344-000	
R76	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R77	RESISTOR,FXD CMPSN, 36 OHMS, 5%, 1/8W	745-1863-140	
R78	RESISTOR,VAR NON-WW,200 OHMS, 10%	382-0052-410	
R79	RESISTOR,FXD CMPSN, 1.2K, 10%, 1/8W	745-2344-000	
R80	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/8W	745-2292-000	
R81,R82	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/8W	745-2356-000	
R83	RESISTOR,FXD CMPSN, 470 OHMS, 10%, 1/8W (A10)	745-2329-000	
R83	RESISTOR,FXD CMPSN, 330 OHMS, 10%, 1/8W	745-2323-000	
R84	RESISTOR,FXD CMPSN, 150 OHMS, 10%, 1/8W	745-2311-000	
R85	RESISTOR,FXD CMPSN, 1.2K, 10%, 1/8W	745-2344-000	
R86	RESISTOR,FXD CMPSN, 220 OHMS, 10%, 1/8W	745-2317-000	
R87	RESISTOR,FXD CMPSN, 4.7K, 10%, 1/8W	745-2365-000	
R88	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/8W	745-2356-000	

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
R89	RESISTOR,FXD CMPSN, 390 OHMS, 10%, 1/8W	745-2326-000	
R90	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R91,R92	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R93	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R94	RESISTOR,FXD CMPSN, 560 OHMS, 10%, 1/8W	745-2332-000	
R95	RESISTOR,FXD FILM, 5.11K, 1%, 1/8W	705-1030-000	
R96	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R97	RESISTOR,FXD,CMPSN, 2000OHM THRU 7500HM,5%,1/8W (A8)	637-2529-000	
R97	RESISTOR,FXD CMPSN, 560 OHMS, 5%, 1/8W	745-1863-430	
R98	RESISTOR,FXD FILM, 5.11K, 1%, 1/8W	705-1030-000	
R99	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/8W	745-2347-000	
R100	RESISTOR,FXD CMPSN, 470 OHMS, 10%, 1/8W (B1)	745-2329-000	
R100	RESISTOR,FXD CMPSN, 270 OHMS, 10%, 1/8W	745-2320-000	
R101	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/8W	745-2347-000	
R102	RESISTOR,FXD CMPSN, 15K, 10%, 1/8W	745-2383-000	
R103	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R104	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W (A10)	745-2377-000	
R104	RESISTOR,FXD CMPSN, 6.8K, 10%, 1/8W	745-2371-000	
R105	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/8W	745-2292-000	
R106	RESISTOR,FXD CMPSN, 470 OHMS, 10%, 1/8W	745-2329-000	
R107	RESISTOR,FXD CMPSN, 220 OHMS, 10%, 1/8W	745-2317-000	
R108	RESISTOR,FXD CMPSN, 1.2K, 10%, 1/8W	745-2344-000	
R109	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R110	RESISTOR,FXD CMPSN, 15K, 10%, 1/8W	745-2383-000	
R111	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R112	RESISTOR,FXD CMPSN, 220 OHMS, 10%, 1/8W	745-2317-000	
R113	RESISTOR,FXD CMPSN, 36 OHMS, 5%, 1/8W	745-1863-140	
R114	RESISTOR,FXD CMPSN, 270 OHMS, 10%, 1/8W	745-2320-000	
R115	RESISTOR,FXD CMPSN, 330 OHMS, 10%, 1/8W	745-2323-000	
R116	NOT USED		
R117	RESISTOR,FXD CMPSN, 8.2MEGO, 5%, 1/8W	745-1864-470	
R118	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R119	RESISTOR,FXD CMPSN, 3.3K, 10%, 1/8W	745-2359-000	
R120	NOT USED		
R121	RESISTOR,FXD FILM, 10K, 1%, 1/8W	705-1044-000	
R122	RESISTOR,FXD FILM, 47.5K, 1%, 1/8W	705-3605-800	
R123	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R124	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/8W	745-2356-000	
R125	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R126	RESISTOR,FXD FILM, 1.40K, 1%, 1/8W	705-1003-000	
R127	RESISTOR,FXD FILM, 18.7K, 1%, 1/8W	705-1057-000	
R128	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R129	RESISTOR,FXD FILM, 100K, 1%, 1/8W	705-1092-000	
R130	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R131	RESISTOR,FXD FILM, 47.5K, 1%, 1/8W	705-3605-800	
R132	RESISTOR,VAR NON-WW,5K, 10%	382-0052-450	
R133	RESISTOR,FXD CMPSN, 6.8K, 10%, 1/8W	745-2371-000	
R134	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R135	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R136	RESISTOR,FXD FILM, 37.4K, 1%, 1/8W	705-3605-750	
R137	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R138	RESISTOR,FXD FILM, 10K, 1%, 1/8W	705-1044-000	
R139	RESISTOR,FXD FILM, 12.4K, 1%, 1/8W	705-3605-520	
R140	RESISTOR,FXD FILM, 30.1K, 1%, 1/8W	705-1067-000	
R141	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R142	RESISTOR,FXD FILM, 22.6K, 1%, 1/8W (A3)	705-1061-000	
R142	RESISTOR,FXD FILM, 15.4K, 1%, 1/8W	705-1053-000	
R143	RESISTOR,VAR NON-WW,20K, 10%	382-0052-470	
R144	RESISTOR,FXD FILM, 38.3K, 1%, 1/8W	705-1072-000	
R145	RESISTOR,FXD FILM, 13K, 1%, 1/8W	705-3605-530	
R146	RESISTOR,FXD FILM, 100K, 1%, 1/8W	705-1092-000	
R147	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/8W	745-2356-000	
R148	RESISTOR,FXD CMPSN, 270K, 10%, 1/8W (A5)	745-2428-000	
R148	RESISTOR,FXD CMPSN, 470K, 10%, 1/8W	745-2437-000	
R149	RESISTOR,FXD CMPSN, 680 OHMS, 10%, 1/8W	745-2335-000	
R150	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R151	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/8W	745-2292-000	
R152	RESISTOR,FXD FILM, 7.32K, 1%, 1/8W	705-3605-410	
R153	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/8W	745-2353-000	
R154,	NOT USED		
R155			
R156	RESISTOR,FXD CMPSN, 16K, 10%, 1/8W	745-2386-000	
R157	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R158	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R159	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R160	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R161	RESISTOR,FXD CMPSN, 560K, 10%, 1/8W	745-2440-000	
R162,	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R163			
R164	RESISTOR,FXD FILM, 221K, 1%, 1/8W	705-3604-170	
R165-	NOT USED		
R167			
R168	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/8W (A13)	745-2353-000	
R168	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R169	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R170-	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R176			
R177,	NOT USED		
R178			
R179	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R180	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	

Channel A IF, Through REV AC, Schematic Diagram
Figure 11 (Sheet 2)



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, INDUCTANCE VALUES ARE IN MICROHENRYS, AND DIODES ARE TYPE 1N4454.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. □ DENOTES CIRCUIT CARD PAD.
4. IF GAIN FROM J1 TO J4 DOES NOT MEET SPECIFICATION (8.2±2dB) USE TEST SELECT RESISTOR 637-2529-001.
5. ALL VOLTAGES ARE NOMINAL FOR INPUT CONDITIONS GIVEN. RF MODULE IS NOT IN AGC LOOP (USB-RECEIVE)

POWER AND GROUND CONNECTIONS

U NO.	TYPE	POWER (V DC)			
		+15	+5	GND	-15
U1, U2	MC1420G				
U3	LM324N	4			11
U4	MC1458PI	8			4
U5	CD4098BE		16	8	
U7	MC14011CF	14		7	
U8	F4049BPC		14	7	
U10	MC14025CP		14	7	
U14	MC1496G		14	7	

6. THE ONLY DIFFERENCE BETWEEN THE 637-2650-001, -002 AND -003 IS USB FILTER, FL1.
   - -001 2.75 kHz BANDWIDTH, 526-9955-010
   - -002 3.05 kHz BANDWIDTH, 526-9980-010
   - -003 3.10 kHz BANDWIDTH, 526-9985-010

637-2397-001
TPA-0441-016 SH 1

Channel A IF, Through REV AC, Schematic Diagram
Figure 11 (Sheet 3)

PARTS LIST (Cont)

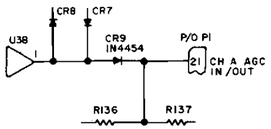
REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
R181	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R182,	NOT USED		
R183			
R184	RESISTOR,FXD CMPSN, 560K, 10%, 1/8W (A7)	745-2440-000	
R185,	NOT USED		
R186			
R187	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W (A7)	745-2413-000	
R188,	NOT USED		
R189			
R190	RESISTOR,FXD CMPSN, 3.9K, 10%, 1/8W	745-2362-000	
R191	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W (A9)	745-2389-000	
R192-	NOT USED		
R204			
R205	RESISTOR,FXD CMPSN, 22 OHMS, 10%, 1/8W	745-2280-000	
R206-	NOT USED		
R250			
R251	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R252	RESISTOR,FXD CMPSN, 820 OHMS, 10%, 1/8W	745-2338-000	
R253	RESISTOR,FXD CMPSN, 56 OHMS, 10%, 1/8W	745-2295-000	
R254	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R255,	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R256			
R257	RESISTOR,FXD CMPSN, 1.3K, 5%, 1/8W	745-1863-520	
R258	RESISTOR,FXD CMPSN, 180 OHMS, 10%, 1/8W	745-2314-000	
R259	RESISTOR,FXD CMPSN, 3K, 5%, 1/8W	745-1863-600	
R260	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R261	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R262	RESISTOR,VAR NON-WW,2K, 10%	382-0052-440	
R263	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/8W	745-2353-000	
R264	NOT USED		
R265	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/4W	745-0713-000	
R266	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R267	RESISTOR,FXD CMPSN, 330K, 5%, 1/8W (A2)	745-1864-130	
R267	RESISTOR,FXD CMPSN, 430K, 5%, 1/8W	745-1864-160	
R268	NOT USED		
R269	RESISTOR,FXD CMPSN, 4.7K, 10%, 1/8W (A7)	745-2365-000	
TP1	JACK,TIP BRN	360-0484-070	
TP2	JACK,TIP RED	360-0484-020	
TP3	JACK,TIP ORN	360-0484-050	
TP4	JACK,TIP YEL	360-0484-060	
T1	TRANSFORMER,RF	278-0430-010	
T2	TRANSFORMER,RF	278-0430-180	
T3	TRANSFORMER,RF	278-0432-010	
T4	TRANSFORMER,RF	278-0430-030	
T5	TRANSFORMER,RF	278-0432-030	
U1,U2	INTEGRATED CKT MC1420G	351-1050-030	
U3	AMPLIFIER,QUAD LM324N	351-1141-030	
U4	INTEGRATED CKT MC1458P1	351-1071-070	
U5	INTEGRATED CKT CD4098BE	351-8278-010	
U6	NOT USED		
U7	INTEGRATED CKT MC14011CP	351-8159-040	
U8	INTEGRATED CKT F4049BPC	351-8159-210	
U9	NOT USED		
U10	INTEGRATED CKT MC14025CP	351-8159-150	
U11-U13	NOT USED		
U14	INTEGRATED CKT MC1496G	351-0043-020	
VR1,VR2	SEMICOND DEVICE 1N755A	353-2718-000	
VR3	SEMICOND DEVICE 1N751A	353-2710-000	
VR4	NOT USED		
VR5	SEMICOND DEVICE 1N758A	353-2724-000	
R49,R56, R94,R97	RESISTOR,FXD,CMPSN, 200OHM THRU 1K,5%,1/8W (TEST SELECT)	637-2529-001	

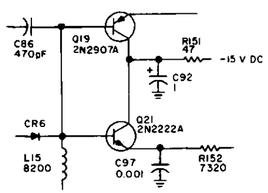
MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Deleted CR9 from AGC in/out line as shown below:	REV E and above
A2	Added CR22, 1N4454. Changed: CR18 from 1N816 to 1N5767. C33 from 0.01μF to 2.2μF. C73 from 0.01μF to 2.2μF. C100 from 4.7μF to 22μF. R54 from 1kΩ to 390Ω. R267 from 300kΩ, 10% to 430 kΩ, 5%.	REV E and above
A3	Changed R142 from 22.6kΩ to 15.4kΩ.	REV F and above
A4	Removed C72, 15pF from across R95 (input to FL1, USB filter).	REV G and above
A5	Added C155, 47μF electrolytic. Changed: C7 from 47;F to 68pF. C15 from 0.01μF ceramic to 1.0μF electrolytic. C29 from 0.01μF to 1.0μF. R148 from 270kΩ to 470kΩ.	REV G and above
A6	Changed Q21 from 2N2222A to 2N2907A. (Circuit was as shown below.)	REV G and above

A7	Added CR17, 1N4454.
	Added C118, 1.5μH.
	Added Q12, 2N2222A.
	Added R184, 560kΩ.
	Added R187, 100kΩ.
	Added R266, 10kΩ.
	Added R269, 4700Ω.
		REV H and above

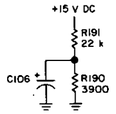
A8	Added C72, 18pF. Changed: C15 from 1.0μF to 10μF. C65 from 1.0μF to 10μF. C66 from 0.1μF to 10μF. C68 from 1.0μF to 10μF.	REV K and above



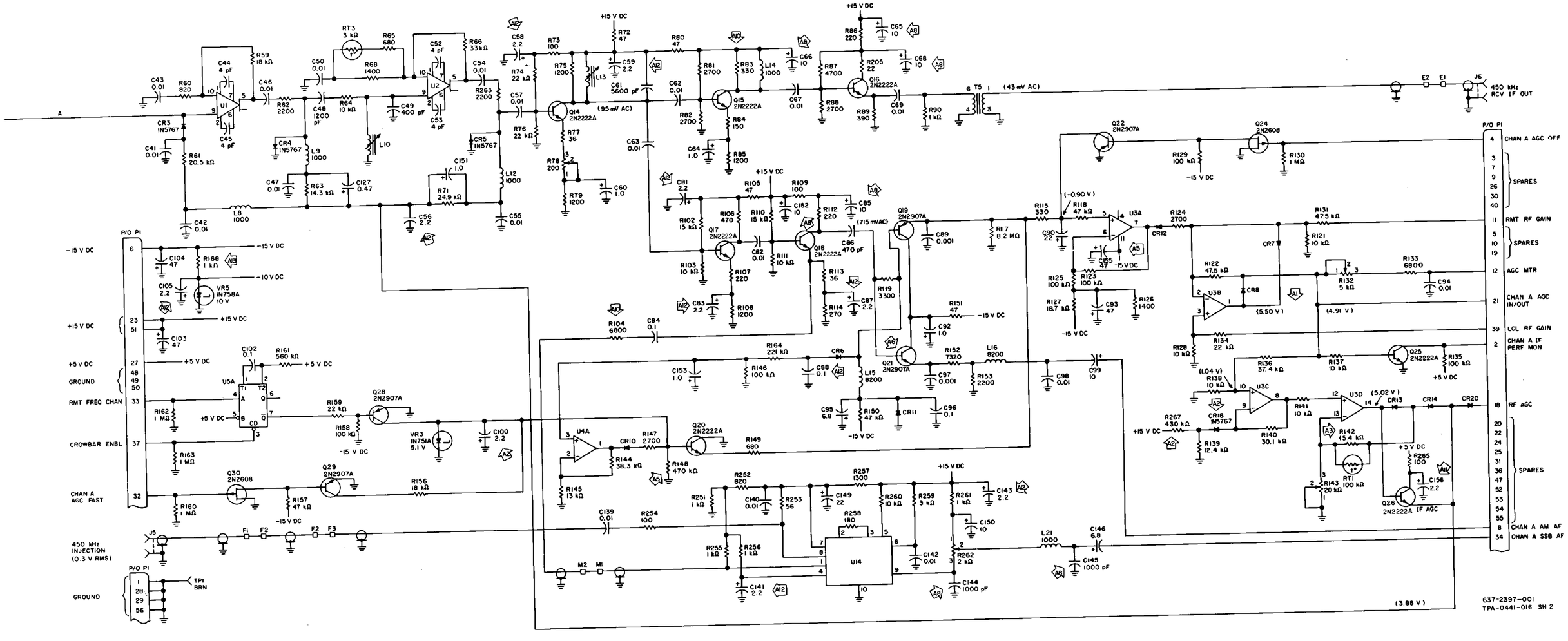


MODIFICATION HISTORY (Cont)

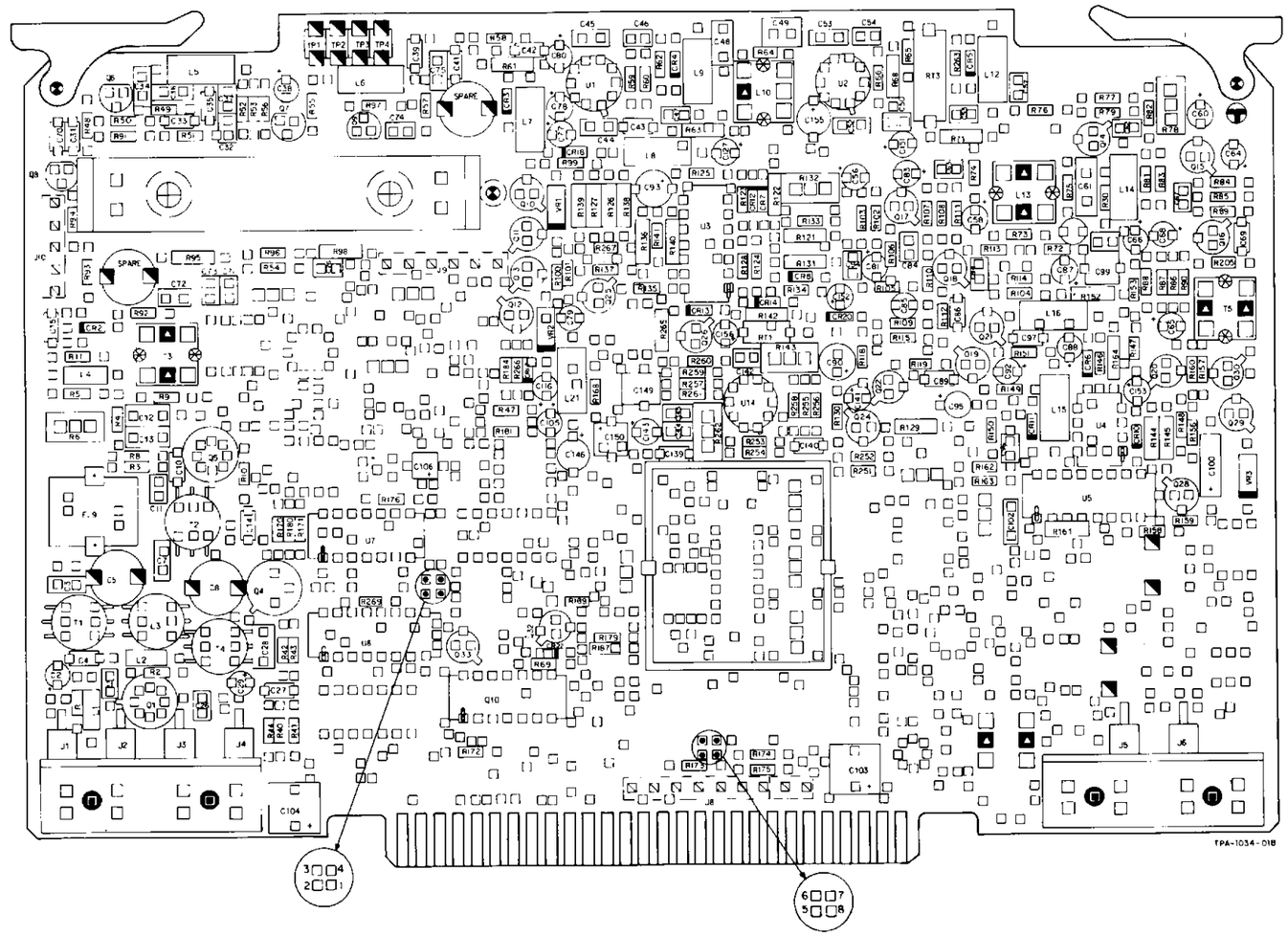
REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
	C75 from 20pF to 6 pF. C85 from 1.0μF to 10μF. C144 from 0.01μF to 1000pF. C145 from 0.01μF to 1000pF. C152 from 1.0μF to 10μF. R49 from test select of 200Ω to 750Ω, to fixed 620Ω. R55 from 1kΩ, 10% to 1kΩ, 5%. R56 from test select of 200Ω to 750Ω, to fixed 620Ω. R97 from test select of 200Ω to 750Ω, to fixed 560Ω.	
A9	Removed C106, 6.8μF; R190, 3900Ω; and R191, 22kΩ from circuit as shown below:	REV K and above
A10	Changed: R83 from 470Ω to 330Ω. R104 from 10kΩ to 6800Ω.	REV N and above
A11	Added C156, 2.2μF electrolytic.	REV P and above
A12	Changed: C2 from 0.1μF to 2.2μF. C56 from 0.1μF to 2.2μF. C58 from 0.1μF to 2.2μF. C59 from 0.1μF to 2.2μF. C77 from 0.1μF to 2.2μF. C78 from 0.1μF to 2.2μF. C79 from 0.1μF to 2.2μF. C80 from 0.1μF to 2.2μF. C81 from 0.1μF to 2.2μF. C83 from 0.1μF to 2.2μF. C87 from 0.1μF to 2.2μF. C88 from 0.1μF electrolytic to 0.1 μF ceramic. C105 from 0.1μF to 2.2μF. C141 from 0.1μF to 2.2μF. C143 from 0.1μF to 2.2μF.	REV R and above
A13	Changed R168 from 2200Ω to 1kΩ.	REV T and above
B1	Changed: C14 from 0.01μF to 470pF. R100 from 470Ω to 270Ω.	REV AA and above
B2	Changed L7 from 2700μH to 5600μH.	REV AC and above



Channel A IF, Through REV AC, Schematic Diagram
Figure 11 (Sheet 4)



Channel A IF, Through REV AC, Schematic Diagram
Figure 11 (Sheet 5)



Channel A IF, REV AD and Above, Schematic Diagram
Figure 12 (Sheet 1 of 5)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
	CHANNEL A IF A8	637-2650-001	A
	CHANNEL A IF A8	637-2650-002	B
CR1	NOT USED		
CR2	SEMICOND DEVICE 1N4454	353-3644-010	
CR3-CR5	SEMICOND DEVICE 1N5767	922-6119-010	
CR6-CR8	SEMICOND DEVICE 1N4454	353-3644-010	
CR9	NOT USED		
CR10-	SEMICOND DEVICE 1N4454	353-3644-010	
CR14			
CR15,	NOT USED		
CR16			
CR17	SEMICOND DEVICE 1N4454	353-3644-010	
CR18	SEMICOND DEVICE 1N5767	922-6119-010	
CR19	NOT USED		
CR20	SEMICOND DEVICE 1N4454	353-3644-010	
CR21	NOT USED		
CR22-	SEMICOND DEVICE 1N4454	353-3644-010	
CR26			
C1	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C2	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C3	CAPACITOR,FXD MICA DIEL, 20PF, PORM 0.5PF, 100V	912-4141-150	
C4	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C5	CAPACITOR,VAR CER DIEL, 9 TO 35PF, 200V	917-1225-000	
C6	NOT USED		
C7	CAPACITOR,FXD MICA DIEL, 68PF, 5%, 50V	912-4141-330	
C8	CAPACITOR,VAR CER DIEL, 9 TO 35PF, 200V	917-1225-000	
C9	NOT USED		
C10	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C11	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-180	
C12,C13	CAPACITOR,FXD CER DIEL, 2200PF, 5%, 100V	913-3281-300	
C14	CAPACITOR,FXD CER DIEL, 470PF, 10%, 200V	913-4014-000	
C15	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C16-C25	NOT USED		
C26	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C27	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C28	CAPACITOR,FXD CER DIEL, 1200PF, 5%, 100V	913-3281-290	
C29	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C30	NOT USED		
C31	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C32	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C33	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C34	CAPACITOR,FXD MICA DIEL, 24PF, PORM 0.5PF, 50V	912-4141-160	
C35	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C36	CAPACITOR,FXD MICA DIEL, 24PF, PORM 0.5PF, 50V	912-4141-160	
C37	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C38	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C39	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C40	NOT USED		
C41-C43	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C44,C45	CAPACITOR,FXD MICA DIEL, 4PF, PORM 0.5PF, 300V	912-4141-060	
C46,C47	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C48	CAPACITOR,FXD CER DIEL, 1200PF, 5%, 100V	913-3281-290	
C49	CAPACITOR,FXD MICA DIEL, 480PF, 5%, 50V	912-4141-520	
C50	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C51	NOT USED		
C52,C53	CAPACITOR,FXD MICA DIEL, 4PF, PORM 0.5PF, 300V	912-4141-080	
C54,C55	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C56	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C57	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C58,C59	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C60	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C61	CAPACITOR,FXD CER DIEL, 5600PF, 5%, 100V	913-3261-360	
C62	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C63	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C64	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C65,C66	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C67	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C68	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C69	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C70	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C71	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C72	CAPACITOR,FXD MICA DIEL, 18PF, PORM 0.5PF, 100V	912-4141-140	
C73	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C74	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C75	CAPACITOR,FXD MICA DIEL, 6PF, PORM 0.5PF, 300V	912-4141-090	
C76	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C77-C81	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C82	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C83	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C84	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-180	
C85	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C86	CAPACITOR,FXD CER DIEL, 470PF, 10%, 200V	913-4014-000	
C87	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C88	CAPACITOR,FXD ELCTLT, 0.22UF, 20%, 35V	184-9102-310	
C89	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C90	CAPACITOR,FXD ELCTLT, 22UF, 20%, 15V	184-9102-140	
C91	NOT USED		
C92	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C93	CAPACITOR,FXD ELCTLT, 47UF, 20%, 6V	184-9102-470	
C94	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C95	CAPACITOR,FXD ELCTLT, 6.8UF, 20%, 6V	184-9102-450	

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
C96	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-180	
C97	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C98	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C99	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-610	
C100	CAPACITOR,FXD ELCTLT, 2.2UF, 10%, 20V	184-9086-430	
C101	NOT USED		
C102	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C103,	CAPACITOR,FXD ELCTLT, 47UF, 20%, 20V	184-9102-630	
C104			
C105	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C106	CAPACITOR,FXD ELCTLT, 6.8UF, 20%, 6V	184-9102-450	
C107-	NOT USED		
C115			
C116	CAPACITOR,FXD ELCTLT, 1.5UF, 20%, 25V	184-9102-210	
C127	CAPACITOR,FXD ELCTLT, 0.47UF, 20%, 35V	184-9102-330	
C128-	NOT USED		
C138			
C139,	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C140			
C141	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C142	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C143	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C144,	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C145			
C146	CAPACITOR,FXD ELCTLT, 6.8UF, 20%, 25V	184-9102-670	
C147,	NOT USED		
C148			
C149	CAPACITOR,FXD ELCTLT, 22UF, 20%, 10V	184-9102-520	
C150	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-610	
C151	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C152	CAPACITOR,FXD ELCTLT, 10UF, 20%, 20V	184-9102-170	
C153	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C154	NOT USED		
C155	CAPACITOR,FXD ELCTLT, 47UF, 20%, 20V	184-9102-630	
C156	CAPACITOR,FXD ELCTLT, 2.2UF, 20%, 25V	184-9102-220	
C157	NOT USED		
C158	CAPACITOR,FXD ELCTLT, 15UF, 20%, 20V	184-9102-620	
C159,	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C160			
FL1	FILTER,USB,2.75 KHZ	526-9955-010	A
FL1	FILTER,USB,3.05 KHZ	526-9980-010	B
FL2-FL8	NOT USED		
FL9	FILTER,XTAL,BP 9.45 MHZ	293-1319-010	
J1-J6	CONNECTOR,RCPT ELEC	357-7267-100	
J7	NOT USED		
J8	HOUSING,CONN	372-2625-016	
J9	HOUSING,CONN	372-2625-015	
J10	HOUSING,CONN	372-2625-014	
L1,L2	COIL,RF 100UH	240-2047-000	
L3	TRANSFORMER,RF	278-0430-040	
L4	COIL,RF 100UH	240-2047-000	
L5,L6	COIL,RF 1000UH	240-2715-490	
L7	COIL,RF 2700UH	240-2715-540	
L8,L9	COIL,RF 1000UH	240-2715-490	
L10	INDUCTOR,RF VAR	242-0441-010	
L11	NOT USED		
L12	COIL,RF 1000UH	240-2715-490	
L13	INDUCTOR,RF VAR	242-0441-020	
L14	COIL,RF 1000UH	240-2715-490	
L15,L16	COIL,RF 8200UH	240-2715-600	
L17-L20	NOT USED		
L21	COIL,RF 1000UH	240-2715-490	
Q1	TRANSISTOR U431	351-1151-010	
Q2,Q3	NOT USED		
Q4	TRANSISTOR 2N5109	352-0766-010	
Q5	TRANSISTOR U431	351-1151-010	
Q6-Q9	TRANSISTOR SPF557	352-1068-010	
Q10	TRANSISTOR 2N2222A	352-0661-020	
Q11	TRANSISTOR 2N2907A	352-0551-010	
Q12	TRANSISTOR 2N2222A	352-0661-020	
Q13	TRANSISTOR 2N2907A	352-0551-010	
Q14-Q18	TRANSISTOR 2N2222A	352-0661-020	
Q19	TRANSISTOR 2N2907A	352-0551-010	
Q20	TRANSISTOR 2N2222A	352-0661-020	
Q21,Q22	TRANSISTOR 2N2907A	352-0551-010	
Q23	NOT USED		
Q24	TRANSISTOR 2N2608	352-0605-010	
Q25,Q26	TRANSISTOR 2N2222A	352-0661-020	
Q27	NOT USED		
Q28,Q29	TRANSISTOR 2N2907A	352-0551-010	
Q30	TRANSISTOR 2N2608	352-0605-010	
Q31	NOT USED		
Q32,Q33	TRANSISTOR 2N2608	352-0605-010	
Q34-Q46	NOT USED		
Q47	TRANSISTOR 2N2608	352-0605-010	
Q48	TRANSISTOR 2N5116	352-0915-030	
RT1	RESISTOR,THRM 100K, 10%, 0.5W	714-1736-000	
RT2	NOT USED		
RT3	RESISTOR,THRM 3K, 10%, 1W	714-1715-000	
R1	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R2	RESISTOR,FXD CMPSN, 820 OHMS, 10%, 1/8W	745-2338-000	
R3	RESISTOR,FXD CMPSN, 7.5K, 5%, 1/8W	745-1863-700	
R4,R5	RESISTOR,FXD CMPSN, 56K, 10%, 1/8W	745-2404-000	

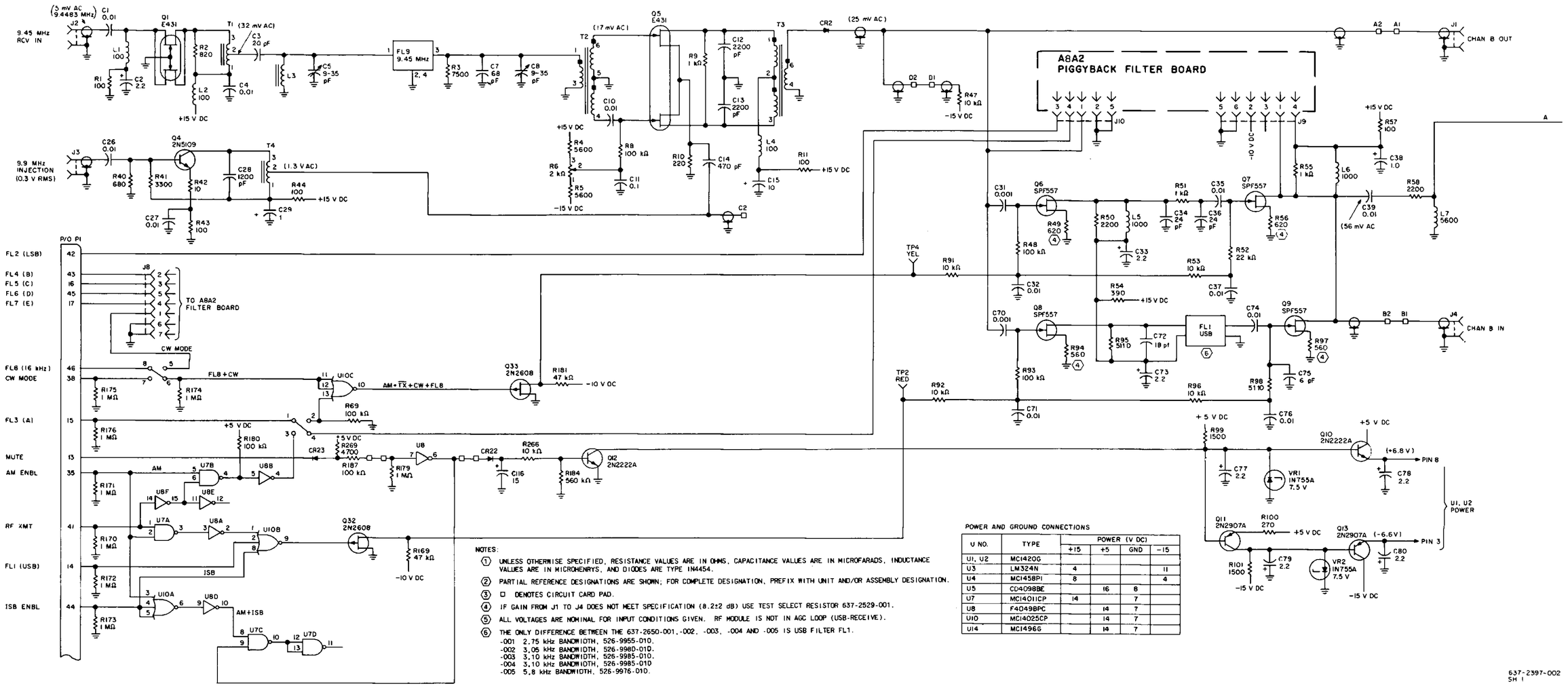
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
R6	RESISTOR,VAR NON-WW,10K, 10%	382-0052-460	
R7	NOT USED		
R8	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R9	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R10	RESISTOR,FXD CMPSN, 220 OHMS, 10%, 1/8W	745-2317-000	
R11	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R12-R39	NOT USED		
R40	RESISTOR,FXD CMPSN, 680 OHMS, 10%, 1/8W	745-2335-000	
R41	RESISTOR,FXD CMPSN, 3.3K, 10%, 1/8W	745-2359-000	
R42	RESISTOR,FXD CMPSN, 10 OHMS, 10%, 1/8W	745-2268-000	
R43,R44	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R45,R46	NOT USED		
R47	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R48	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R49	RESISTOR,FXD CMPSN, 620 OHMS, 5%, 1/8W	745-1863-440	
R50	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/8W	745-2353-000	
R51	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R52	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R53	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R54	RESISTOR,FXD CMPSN, 390 OHMS, 10%, 1/8W	745-2326-000	
R55	RESISTOR,FXD CMPSN, 1K, 5%, 1/8W	745-1863-490	
R56	RESISTOR,FXD CMPSN, 620 OHMS, 5%, 1/8W	745-1863-440	
R57	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R58	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/8W	745-2353-000	
R59	RESISTOR,FXD CMPSN, 18K, 10%, 1/8W	745-2386-000	
R60	RESISTOR,FXD CMPSN, 820 OHMS, 10%, 1/8W	745-2338-000	
R61	RESISTOR,FXD FILM, 20.5K, 1%, 1/8W	705-1059-000	
R62	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/8W	745-2353-000	
R63	RESISTOR,FXD FILM, 14.3K, 1%, 1/8W	705-3605-550	
R64	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R65	RESISTOR,FXD CMPSN, 680 OHMS, 10%, 1/8W	745-2335-000	
R66	RESISTOR,FXD CMPSN, 33K, 10%, 1/8W	745-2395-000	
R67	NOT USED		
R68	RESISTOR,FXD FILM, 1.40K, 1%, 1/8W	705-1003-000	
R69	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R70	NOT USED		
R71	RESISTOR,FXD FILM, 24.9K, 1%, 1/8W	705-1063-000	
R72	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/8W	745-2292-000	
R73	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R74	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R75	RESISTOR,FXD CMPSN, 1.2K, 10%, 1/8W	745-2344-000	
R76	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R77	RESISTOR,FXD CMPSN, 36 OHMS, 5%, 1/8W	745-1863-140	
R78	RESISTOR,VAR NON-WW,200 OHMS, 10%	382-0052-410	
R79	RESISTOR,FXD CMPSN, 1.2K, 10%, 1/8W	745-2344-000	
R80	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/8W	745-2292-000	
R81,R82	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/8W	745-2356-000	
R83	RESISTOR,FXD CMPSN, 330 OHMS, 10%, 1/8W	745-2323-000	
R84	RESISTOR,FXD CMPSN, 150 OHMS, 10%, 1/8W	745-2311-000	
R85	RESISTOR,FXD CMPSN, 1.2K, 10%, 1/8W	745-2344-000	
R86	RESISTOR,FXD CMPSN, 220 OHMS, 10%, 1/8W	745-2317-000	
R87	RESISTOR,FXD CMPSN, 4.7K, 10%, 1/8W	745-2365-000	
R88	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/8W	745-2356-000	
R89	RESISTOR,FXD CMPSN, 390 OHMS, 10%, 1/8W	745-2326-000	
R90	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R91,R92	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R93	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R94	RESISTOR,FXD CMPSN, 560 OHMS, 10%, 1/8W	745-2332-000	
R95	RESISTOR,FXD FILM, 5.11K, 1%, 1/8W	705-1030-000	
R96	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R97	RESISTOR,FXD CMPSN, 560 OHMS, 5%, 1/8W	745-1863-430	
R98	RESISTOR,FXD FILM, 5.11K, 1%, 1/8W	705-1030-000	
R99	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/8W	745-2347-000	
R100	RESISTOR,FXD CMPSN, 270 OHMS, 10%, 1/8W	745-2320-000	
R101	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/8W	745-2347-000	
R102	RESISTOR,FXD CMPSN, 15K, 10%, 1/8W	745-2383-000	
R103	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R104	RESISTOR,FXD CMPSN, 6.8K, 10%, 1/8W	745-2371-000	
R105	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/8W	745-2292-000	
R106	RESISTOR,FXD CMPSN, 470 OHMS, 10%, 1/8W	745-2329-000	
R107	RESISTOR,FXD CMPSN, 220 OHMS, 10%, 1/8W	745-2317-000	
R108	RESISTOR,FXD CMPSN, 1.2K, 10%, 1/8W	745-2344-000	
R109	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R110	RESISTOR,FXD CMPSN, 15K, 10%, 1/8W	745-2383-000	
R111	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R112	RESISTOR,FXD CMPSN, 270 OHMS, 10%, 1/8W	745-2320-000	
R113	RESISTOR,FXD CMPSN, 36 OHMS, 5%, 1/8W	745-1863-140	
R114	RESISTOR,FXD CMPSN, 270 OHMS, 10%, 1/8W	745-2320-000	
R115	RESISTOR,FXD CMPSN, 330 OHMS, 10%, 1/8W	745-2323-000	
R116,	NOT USED		
R117			
R118	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R119	RESISTOR,FXD CMPSN, 3.3K, 10%, 1/8W	745-2359-000	
R120	NOT USED		
R121	RESISTOR,FXD FILM, 10K, 1%, 1/8W	705-1044-000	
R122	RESISTOR,FXD FILM, 47.5K, 1%, 1/8W	705-3605-800	
R123	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R124	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/8W	745-2356-000	
R125	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R126	RESISTOR,FXD FILM, 1.96K, 1%, 1/8W	705-1010-000	
R127	RESISTOR,FXD FILM, 16.7K, 1%, 1/8W	705-1057-000	
R128	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R129	RESISTOR,FXD FILM, 100K, 1%, 1/8W	705-1092-000	

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
R130	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R131	RESISTOR,FXD FILM, 47.5K, 1%, 1/8W	705-3605-800	
R132	RESISTOR,VAR NON-WW,5K, 10%	382-0052-450	
R133	RESISTOR,FXD CMPSN, 6.8K, 10%, 1/8W	745-2371-000	
R134	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R135	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R136	RESISTOR,FXD FILM, 37.4K, 1%, 1/8W	705-3605-750	
R137	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R138	RESISTOR,FXD FILM, 10K, 1%, 1/8W	705-1044-000	
R139	RESISTOR,FXD FILM, 12.4K, 1%, 1/8W	705-3605-520	
R140	RESISTOR,FXD FILM, 30.1K, 1%, 1/8W	705-1067-000	
R141	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R142	RESISTOR,FXD FILM, 15.4K, 1%, 1/8W	705-1053-000	
R143	RESISTOR,VAR NON-WW,20K, 10%	382-0052-470	
R144	RESISTOR,FXD FILM, 38.3K, 1%, 1/8W	705-1072-000	
R145	RESISTOR,FXD FILM, 64.9K, 1%, 1/8W	705-1083-000	
R146	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R147	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R148	RESISTOR,FXD CMPSN, 330K, 10%, 1/8W	745-2431-000	
R149	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/8W	745-2353-000	
R150	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R151	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/8W	745-2292-000	
R152	RESISTOR,FXD FILM, 7.32K, 1%, 1/8W	705-3605-410	
R153	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/8W	745-2353-000	
R154,	NOT USED		
R155			
R156	RESISTOR,FXD CMPSN, 18K, 10%, 1/8W	745-2386-000	
R157	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R158	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R159	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R160	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R161	RESISTOR,FXD FILM, 196K, 1%, 1/8W	705-1106-000	
R162,	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R163			
R164	RESISTOR,FXD FILM, 221K, 1%, 1/8W	705-3604-170	
R165-	NOT USED		
R167			
R168	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R169	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R170-	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R176			
R177,	NOT USED		
R178			
R179	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R180	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R181	RESISTOR,FXD CMPSN, 47K, 10%, 1/8W	745-2401-000	
R182,	NOT USED		
R183			
R184	RESISTOR,FXD CMPSN, 560K, 10%, 1/8W	745-2440-000	
R185,	NOT USED		
R186			
R187	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R188-	NOT USED		
R204			
R205	RESISTOR,FXD CMPSN, 22 OHMS, 10%, 1/8W	745-2280-000	
R206-	NOT USED		
R250			
R251	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R252	RESISTOR,FXD CMPSN, 820 OHMS, 10%, 1/8W	745-2338-000	
R253	RESISTOR,FXD CMPSN, 56 OHMS, 10%, 1/8W	745-2295-000	
R254	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R255,	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R256			
R257	RESISTOR,FXD CMPSN, 1.3K, 5%, 1/8W	745-1863-520	
R258	RESISTOR,FXD CMPSN, 180 OHMS, 10%, 1/8W	745-2314-000	
R259	RESISTOR,FXD CMPSN, 3K, 5%, 1/8W	745-1863-600	
R260	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R261	RESISTOR,FXD CMPSN, 1K, 10%, 1/8W	745-2341-000	
R262	RESISTOR,VAR NON-WW,2K, 10%	382-0052-440	
R263	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/8W	745-2353-000	
R264	NOT USED		
R265	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/4W	745-0713-000	
R266	RESISTOR,FXD CMPSN, 10K, 10%, 1/8W	745-2377-000	
R267	RESISTOR,FXD CMPSN, 430K, 5%, 1/8W	745-1864-160	
R268	NOT USED		
R269	RESISTOR,FXD CMPSN, 4.7K, 10%, 1/8W	745-2365-000	
R270	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R271-	NOT USED		
R274			
R275,	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R276			
R277	RESISTOR,FXD CMPSN, 4.7K, 10%, 1/8W	745-2365-000	
TP1	JACK,TIP BRN	360-0484-070	
TP2	JACK,TIP RED	360-0484-020	
TP3	JACK,TIP ORN	360-0484-050	
TP4	JACK,TIP YEL	360-0484-060	
T1	TRANSFORMER,RF	278-0430-010	
T2	TRANSFORMER,RF	278-0430-180	
T3	TRANSFORMER,RF	278-0432-010	
T4	TRANSFORMER,RF	278-0430-030	
T5	TRANSFORMER,RF	278-0432-030	
U1,U2	INTEGRATED CKT MC14206	351-1050-030	
U3	AMPLIFIER,QUAD LM324	351-1141-030	

Channel A IF, REV AD and Above, Schematic Diagram
Figure 12 (Sheet 2)



POWER AND GROUND CONNECTIONS

U NO.	TYPE	POWER (V DC)			
		+15	+5	GND	−15
U1, U2	MC1420G				
U3	LM324N	4			11
U4	MC1458PI	8			4
U5	CD4098BE		16	8	
U7	MC14011CP	14		7	
U8	F4049BPC		14	7	
U10	MC14025CP		14	7	
U14	MC1496G		14	7	

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, INDUCTANCE VALUES ARE IN MICROHENRYS, AND DIODES ARE TYPE 1N4454.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. □ DENOTES CIRCUIT CARD PAD.
4. IF GAIN FROM J1 TO J4 DOES NOT MEET SPECIFICATION (8.2±2 dB) USE TEST SELECT RESISTOR 637-2529-001.
5. ALL VOLTAGES ARE NOMINAL FOR INPUT CONDITIONS GIVEN. RF MODULE IS NOT IN AGC LOOP (USB-RECEIVE).
6. THE ONLY DIFFERENCE BETWEEN THE 637-2650-001, -002, -003, -004 AND -005 IS USB FILTER FL1.
   - -001 2.75 kHz BANDWIDTH, 526-9955-010.
   - -002 3.05 kHz BANDWIDTH, 526-9980-010.
   - -003 3.10 kHz BANDWIDTH, 526-9985-010.
   - -004 3.10 kHz BANDWIDTH, 526-9985-010
   - -005 5.8 kHz BANDWIDTH, 526-9976-010.

Channel A IF, REV AD and Above, Schematic Diagram
Figure 12 (Sheet 3)

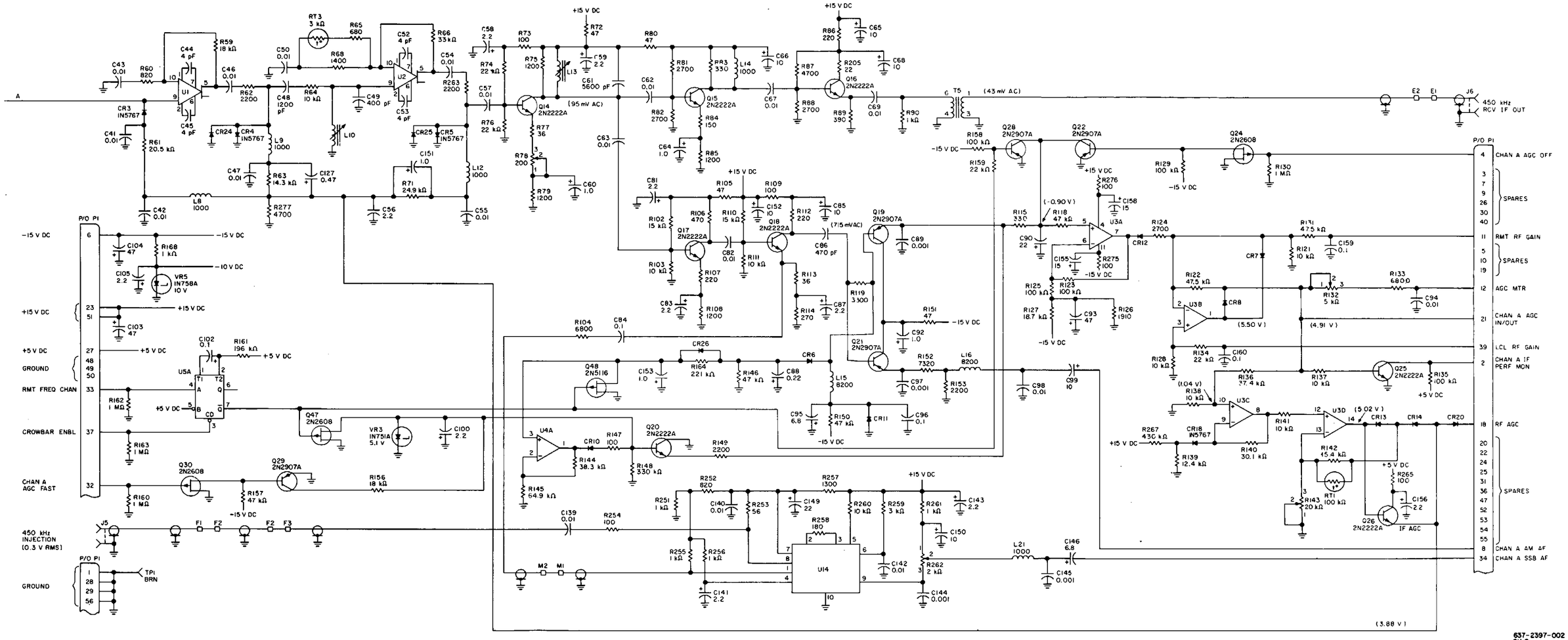
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
U4	INTEGRATED CKT MC1458G	351-1071-070	
U5	INTEGRATED CKT CD4098BE	351-8278-010	
U6	NOT USED		
U7	INTEGRATED CKT CD4011G	351-8159-040	
U8	INTEGRATED CKT CD4049A	351-8159-210	
U9	NOT USED		
U10	INTEGRATED CKT CD4025A	351-8159-150	
U11-U13	NOT USED		
U14	INTEGRATED CKT MC1496G	351-0043-020	
VR1,VR2	SEMICOND DEVICE 1N755A	353-2718-000	
VR3	SEMICOND DEVICE 1N751A	353-2710-000	
VR4	NOT USED		
VR5	SEMICOND DEVICE 1N758A	353-2724-000	
R49,R56, R94,R97	RESISTOR,FXD,CMPSN, 200OHM THRU 1K,5%,1/8W (TEST SELECT)	637-2529-001	

MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
None	Note For configuration before REV AD, refer to figure 10. Changed layout of base planar board. Deleted CR17, 1N4454 R117, 8.2 MΩ Changed C88 from 0.1μF to 0.22μF. C155 from 47μF to 15μF. R126 from 1400Ω to 1910Ω. R145 from 13kΩ to 84.9kΩ. R146 from 100kΩ to 47kΩ. R147 from 2700Ω to 100Ω. R148 from 470kΩ to 330kΩ. R149 from 680Ω to 220Ω. Added CR23, 1N4454. CR24, 1N4454. CR25, 1N4454. CR26, 1N4454. C158, 15μF electrolytic. C159, 0.1μF. C160, 0.1μF. R275, 100Ω. R276, 100Ω. R277, 4700Ω. Q47, 2N2608. Q48, 2N5116.	AD and above

Channel A IF, REV AD and Above, Schematic Diagram
Figure 12 (Sheet 4)



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SH 2

Channel A IF, REV AD and Above, Schematic Diagram
Figure 12 (Sheet 5)

Filter
(637-2515-( ))

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

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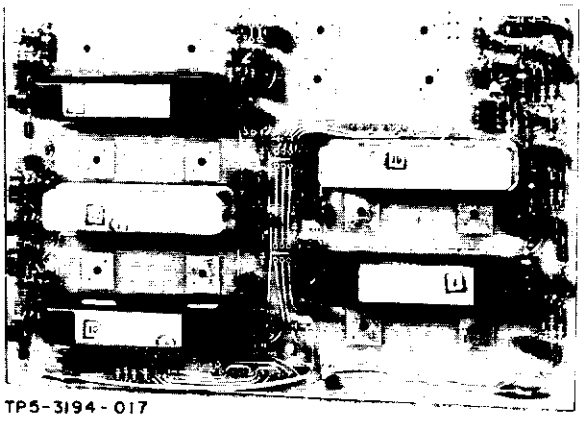
3rd Edition, 1 January 1979

1. DESCRIPTION

Filter 637-2515-( ), shown in figure 1, is a 2-layer planar card with one 7-pin, one 6-pin, and one 5-pin blue-line connector. The filter card mates with a channel A if card and provides additional selectable filters.

The filter card consists of six filter circuits and a CW strapping circuit. Refer to table 1.



Filter
Figure 1

Table 1. Filter Complement.

REF DES	COLLINS PART NO	FILTER 637-2515-( )						DESCRIPTION
		001	002	003	004	005	006	
FL2	526-9956-010	NA	NA	NA	X	X	NA	2.75 kHz bandwidth (LSB 250 - 3000 Hz)
FL3	526-9963-060	X	X	X	NA	X	X	6.0 kHz bandwidth (AM ±3000 Hz)
FL4	526-9963-040	X	NA	X	NA	X	X	3.0 kHz bandwidth (AM ±1500 Hz)
FL5	526-9963-030 526-9974-030	X	NA	 X	NA	X	X	1.0 kHz bandwidth (AM ±500 Hz) 1.0 kHz bandwidth (USB 500 - 1500 Hz)
FL6	526-9963-020 526-9974-030	X	NA	 X	NA	X	X	0.5 kHz bandwidth (AM ±250 Hz) 0.5 kHz bandwidth (USB 750 - 1250 Hz)
FL7	526-9963-010 526-9974-010 293-1333-010	X	 X	 X	NA	X	 X	0.2 kHz bandwidth (AM ±100 Hz) 0.2 kHz bandwidth (USB 900 - 1100 Hz) 0.1 kHz bandwidth (AM ±50 Hz)
CR11	353-3644-010	NA	X	NA	NA	NA	NA	Anode to E1, cathode to E5

NOTICE: This section replaces second edition dated 1 June 1978.

2. PRINCIPLES OF OPERATION (Refer to figure 4.)

2.1 General

The filter card receives 450 kHz if from the channel A if card, makes filter selection as controlled by the FL2 through FL7, or CW mode switching inputs, and supplies 450-kHz filtered if to the channel A if card.

2.2 CW Mode Strapping

CW mode can be strapped to FL4, FL5, FL6, or FL7. To strap CW mode for the desired filter, CR11 is connected as follows:

a. For FL4(B), connect CR11 anode to E1 and cathode to E2.
b. For FL5 (C), connect CR11 anode to E1 and cathode to E3.
c. For FL6 (D), connect CR11 anode to E1 and cathode to E4.
d. For FL7 (E), connect CR11 anode to E1 and cathode to E5.

2.3 Bandpass Filter Control Circuits

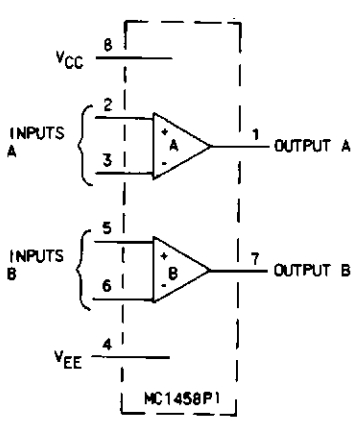
The filter card provides filter selection of 450-kHz if signals. Filter selection is initiated by the CW mode control signal or by a bandwidth control signal. This means only that these signals are applied to the filter card to initiate filter selection and does not reflect a mode of operation or selection of a bandwidth.

FL2 (LSB), FL3 (A), FL4 (B), FL5 (C), FL6 (D), and FL7 (E) are selected when the associated enable signal is applied to the filter card. FL4 (B), FL5 (C), FL6 (D), and FL7 (E) can also be selected by CW mode signal when strapped as described in paragraph 2.2. These filters are optional and the following are typical frequency bandwidths.

a. FL2 (LSB), 2.7 kHz, LSB
b. FL3 (A), 6 kHz, AM
c. FL4 (B), 3 kHz, AM
d. FL5 (C), 1 kHz, AM
e. FL6 (D), 0.5 kHz, AM
f. FL7 (E), 0.2 kHz, AM

2.4 Dual Operational Amplifier MC1458P1 (Refer to figure 2.)

The MC1458P1 consists of two operational amplifiers in one package designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components.



CHARACTERISTICS
SUPPLY VOLTAGE: V_{CC} +18 V DC MAX
V_{EE} -18 V DC MAX
INPUT DIFF VOLTAGE: ±30 V MAX
INPUT COMMON MODE VOLTAGE:
±15 V MAX (1)
OUTPUT SHORT CIRCUIT DURATION:
CONTINUOUS (2)
INPUT RESISTANCE: 300 kΩ MIN, 2.0 MΩ MAX
OUTPUT RESISTANCE: 75Ω TYPICAL
VOLTAGE GAIN: 15 MIN

NOTES:
(1) FOR SUPPLY VOLTAGE LESS THAN ±15.0 V, MAX INPUT VOLTAGE EQUAL TO SUPPLY VOLTAGE.
(2) SUPPLY VOLTAGE EQUAL TO OR LESS THAN 15 V.

TP5-2285-013

Dual Operational Amplifier MC1458P1
Figure 2

2.5 Quad Operational Amplifier LM324N (Refer to figure 3.)

The LM324N consists of four independent, high-gain, internally frequency-compensated operational amplifiers that are designed to operate from a single power supply over a wide range of voltages. Common applications include transducer amplifiers, dc gain blocks, and all conventional operational amplifier circuits.

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the filter card are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 2 check total performance of the filter card. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

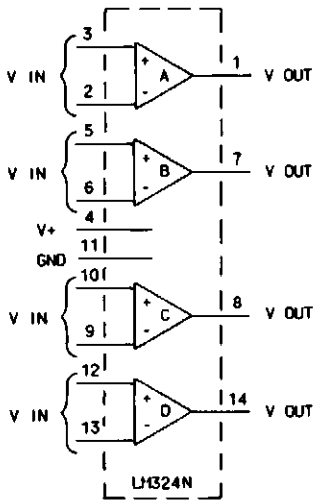
4. ALIGNMENT/ADJUSTMENT

4.1 Filter Amplifier Gain Adjustment

a. Set front-panel MODE switch to AM and BANDWIDTH switch to 16. Set AGC switch to FAST.
b. Measure signal at channel A if J1 with no receive input signal.

4.1.1 AM Filters

a. Connect receive input of 9.4500 MHz to channel A if.
b. Set receive signal to 50 μV (9.4500 MHz). Find a passband response minimum between 9.4493 and 9.4489 MHz at channel A if J4. Measure voltage gain between channel A if J1 and J4; should be 8.2 ±2.0 dB.



CHARACTERISTICS
SUPPLY VOLTAGE (V+): 32 V DC MAX
INPUT DIFF VOLTAGE: 32 V DC MAX
INPUT COMMON MODE VOLTAGE: V+ (-1.5 V DC)
OUTPUT SHORT CIRCUIT DURATION:
CONTINUOUS (1)
VOLTAGE GAIN: 25 MIN

NOTE:
(1) SUPPLY VOLTAGE EQUAL TO OR LESS THAN 15 V.

TP5-2289-013

Quad Operational Amplifier LM324N
Figure 3

Table 2. Filter, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of unit containing the control that is to be tested.		
	b. Remove channel A if (with filter installed).		
	c. Remove filter from channel A if.		
	d. Test channel A if.		
	e. When channel A if operation is verified mount filter on channel A if. Install channel A if with filter on an extender card and place it in the unit.		
	f. Set unit LINE SELECTOR switch to 115 V.		
	g. Connect unit to 115-V ac power source and set power on.		
	h. Measure dc voltages between the following pins and ground (P8-6, 7; P9-5, 6; or P10-2, 5):		
	P9-4 P9-2	15 1.0 V dc. -10 1.0 V dc.	Check associated power supply.
2. 2.75-kHz LSB filter measurement	**Note** This test applies only to 2.75-kHz LSB filter (526-9956-010).		
	a. Set front-panel MODE switch to SSB/CW and BANDWIDTH switch to LSB.		
	b. Set AGC switch to OFF.		
	c. Set receive input at channel A if J2 for 9.4517 MHz.		
	d. Using an rf voltmeter, measure rf voltage at channel A if J4. Adjust receive input level and frequency for a 70-mV peak reading at channel A if J4.	Reference.	
	e. Adjust input frequency down until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NMT 9.450250 MHz.	Check FL2, Q9, Q10, and associated circuit.
	f. Adjust input frequency up until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NLT 9.453000 MHz.	Check FL2, Q9, Q10, and associated circuit.

Table 2. Filter, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. 6-kHz AM filter measurement	**Note** This test applies only to 6-kHz AM filter (526-9963-060).		
	a. Set front-panel MODE switch to SSB/CW and BANDWIDTH switch to A. **Note** If 6-kHz filter is in any filter slot other than A, set BANDWIDTH switch to that position.		
	b. Set AGC switch to OFF.		
	c. Set receive input at channel A if J2 for 9.4500 MHz.		
	d. Using an rf voltmeter, measure rf voltage at channel A if J4. Adjust receive input level and frequency for a 70-mV peak reading at channel A if J4.	Reference.	
	e. Adjust input frequency down until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NMT 9.447000 MHz.	Check FL3, Q11, Q12, and associated circuit.
	f. Adjust input frequency up until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NLT 9.453000 MHz	Check FL3, Q11, Q12, and associated circuit.
4. 3-kHz AM filter measurement	**Note** This test applies only to 3-kHz AM filter (526-9963-040).		
	a. Set front-panel MODE switch to SSB/CW and BANDWIDTH switch to B. **Note** If 3-kHz filter is in any filter slot other than B, set BANDWIDTH switch to that position.		
	b. Set AGC switch to OFF.		
	c. Set receive input at channel A if J2 for 9.4500 MHz.		
(Cont)	d. Using an rf voltmeter, measure rf voltage at channel A if J4. Adjust receive input level and frequency for a 70-mV peak reading at channel A if J4.	Reference.	

Table 2. Filter, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	e. Adjust input frequency down until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NMT 9.448500 MHz.	Check FL4, Q1, Q2, and associated circuit.
	f. Adjust input frequency up until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NLT 9.451500 MHz.	Check FL4, Q1, Q2, and associated circuit.
5. 1.0-kHz AM filter measurement	**Note** This test applies only to 1.0-kHz AM filter (526-9963-030).		
	a. Set front-panel MODE switch to SSB/CW and BANDWIDTH switch to C. **Note** If 1.0-kHz filter is in any filter slot other than C, set BANDWIDTH switch to that position.		
	b. Set AGC switch to OFF.		
	c. Set receive input at channel A if J2 for 9.4500 MHz.		
	d. Using an rf voltmeter, measure rf voltage at channel A if J4. Adjust receive input level and frequency for a 70-mV peak reading at channel A if J4.	Reference.	
	e. Adjust input frequency down until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NMT 9.449500 MHz.	Check FL4, Q3, Q4, and associated circuit.
	f. Adjust input frequency up until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NLT 9.450500 MHz.	Check FL5, Q3, Q4, and associated circuit.
5A. 1.0-kHz USB filter measurement	**Note** This test applies only to 1.0-kHz USB filter (526-9974-030).		
	a. Set front-panel MODE switch to SSB/CW and BANDWIDTH switch to C. **Note** If 1.0-kHz filter is in any filter slot other than C, set BANDWIDTH switch to that position.		
(Cont)	b. Set AGC switch to OFF.		

Table 2. Filter, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5.A (Cont)	c. Set receive input at channel A if J2 for 9.4490 MHz.		
	d. Using an rf voltmeter, measure rf voltage at channel A if J4. Adjust receive input level and frequency for a 70-mV peak reading at channel A if J4.	Reference.	
	e. Adjust input frequency down until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NMT 9.448500 MHz.	Check FL4, Q3, Q4, and associated circuit.
	f. Adjust input frequency up until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NLT 9.449500 MHz.	Check FL5, Q3, Q4, and associated circuit.
6. 0.5-kHz AM filter measurement	**Note** This test applies only to 0.5-kHz AM filter (526-9963-020).		
	a. Set front-panel MODE switch to SSB/CW and BANDWIDTH switch to D. **Note** If 0.5-kHz filter is in any filter slot other than D, set BANDWIDTH switch to that position.		
	b. Set AGC switch to OFF.		
	c. Set receive input at channel A if J2 for 9.4500 MHz.		
	d. Using an rf voltmeter, measure rf voltage at channel A if J4. Adjust receive input level and frequency for 70-mV peak reading at channel A if J4.	Reference.	
	e. Adjust input frequency down until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NMT 9.449750 MHz.	Check FL6, Q5, Q6, and associated circuit.
	f. Adjust input frequency up until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NLT 9.450250 MHz.	Check FL6, Q5, Q6, and associated circuit.
6A. 0.5-kHz USB filter measurement (Cont)	**Note** This test applies only to 0.5-kHz USB filter (526-9974-020).		
	a. Set front-panel MODE switch to SSB/CW and BANDWIDTH switch to D.		

Table 2. Filter, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
6.A (Cont)	**Note** If 0.5-kHz filter is in any filter slot other than D, set BANDWIDTH switch to that position.		
	b. Set AGC switch to OFF.		
	c. Set receive input at channel A if J2 for 9.4490 MHz.		
	d. Using an rf voltmeter, measure rf voltage at channel A if J4. Adjust receive input level and frequency for 70-mV peak reading at channel A if J4.	Reference.	
	e. Adjust input frequency down until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NMT 9.448750 MHz.	Check FL6, Q5, Q6, and associated circuit.
	f. Adjust input frequency up until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NLT 9.449250 MHz.	Check FL6, Q5, Q6, and associated circuit.
7. 0.2-kHz AM filter measurement	**Note** This test applies only to 0.2-kHz AM filter (526-9963-010).		
	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to E.		
	Note If 0.2-kHz filter is in any filter slot other than E, set BANDWIDTH switch to that position.		
	b. Set AGC switch to OFF.		
	c. Set receive input at channel A if J2 for 9.4500 MHz.		
	d. Using an rf voltmeter, measure rf voltage at channel A if J4. Adjust receive input level and frequency for a 70-mV peak reading at channel A if J4.	Reference.	
	e. Adjust input frequency down until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NMT 9.449900 MHz.	Check FL7, Q7, Q8, and associated circuit.
	f. Adjust input frequency up until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NLT 9.450100 MHz.	Check FL7, Q7, Q8, and associated circuit.

Table 2. Filter, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
7.A. 0.2-kHz USB filter measurement	**Note** This test applies only to 0.2-kHz USB filter (526-9974-010).		
	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to E. **Note** If 0.2-kHz filter is in any filter slot other than E, set BANDWIDTH switch to that position.		
	b. Set AGC switch to OFF.		
	c. Set receive input at channel A if J2 for 9.4490 MHz.		
	d. Using an rf voltmeter, measure rf voltage at channel A if J4. Adjust receive input level and frequency for a 70-mV peak reading at channel A if J4.	Reference	
	e. Adjust input frequency down until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NMT 9.448900 MHz.	Check FL7, Q7, Q8, and associated circuit.
	f. Adjust input frequency up until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NLT 9.449100 MHz.	Check FL7, Q7, Q8, and associated circuit.
8. 0.1-kHz AM filter measurement	**Note** This test applies only to 0.1-kHz AM filter (293-1333-010).		
	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to E. **Note** If 0.1-kHz filter is in any filter slot other than E, set BANDWIDTH switch to that position.		
	b. Set AGC switch to OFF.		
	c. Set receive input at channel A if J2 for 9.1500 MHz.		
	d. Using an rf voltmeter, measure rf voltage at channel A if J4. Adjust receive input level and frequency for a 70-mV peak reading at channel A if J4.	Reference.	
(Cont)	e. Adjust input frequency down until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NMT 9.449950 MHz.	Check FL7, Q7, Q8, and associated circuit.

Table 2. Filter, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
8. (Cont)	f. Adjust input frequency up until rf voltage at channel A if J4 is 3 dB below level of step d. Note input frequency.	NLT 9.450050 MHz.	Check FL7, Q7, Q8, and associated circuit.

c. Set front-panel BANDWIDTH switch to position associated with filter being gain adjusted (refer to table 3).
d. Find a passband response minimum between 9.4493 and 9.4489 MHz at channel A if J4. Measure voltage gain between channel A if J1 and J4; should be 8.2 ±2.0 dB. Select value of gain adjust resistor shown in table 3. (200 through 750 Ω) to give a voltage gain of 8.2 ±2.0 dB.

4.1.2 LSB Filter

a. Connect receive input of 9.4517 MHz to channel A if.
b. Set receive signal to 50 μV (9.4517 MHz). Find a passband response minimum between 9.4507 and 9.4511 MHz at channel A if J4. Measure voltage gain between channel A if J1 and J4. Should be 8.2 ±2.0 dB.
c. Set front-panel BANDWIDTH switch to position associated with filter being gain adjusted (refer to table 3).
d. Find a passband response minimum between 9.4507 and 9.4511 MHz at channel A if J4. Measure voltage gain between channel A if J1 and J4. Should be 8.2 ±2.0 dB. Select value of gain adjust resistor shown in table 3 (330 through 1500 Ω) to give a voltage gain of 8.2 ±2.0 dB.

4.1.3 USB Filters

a. Connect receive input of 9.4490 MHz to channel A if.
b. Set receive signal to 50 μV (9.4490 MHz). Find a passband response minimum between 9.44 and 9.44 MHz at channel A if J4. Should be 8.2 ±2.0 dB. Note this level for reference.
c. Set front panel BANDWIDTH switch to position associated with filter being adjusted (refer to table 3).
d. Find a passband response minimum between 944 and 9.44 MHz at channel A if J4. Measure voltage gain between channel A if J1 and J4. This should be 8.2 ±2.0 dB. Select value of gain adjust resistor shown in table 3 (330 thru 1500 Ω) to give a voltage gain equal to 8.2 ±2.0 dB.

4.2 Filter Passband Measurement

a. Set front-panel MODE switch to SSB/CW and BANDWIDTH switch to position associated with filter having it passband measured (refer to table 3).
b. Set AGC switch to OFF.
c. Set receive input at channel A if J2 for receive if input frequency shown in table 4.

d. Using an rf voltmeter, measure voltage at channel A if J4. Adjust receive input level and frequency for a 70-mV peak reading at channel A if J4. Note this level for reference.
e. Adjust input frequency down until rf voltage at channel A if J4 is 3 dB below level of step d. Note the input frequency. If more than the lower 3 dB frequency of the applicable filter in table 4, select value of associated passband adjust capacitors (refer to table 3) until the lower 3-dB frequency is not more than that listed in table 4.
f. Adjust input frequency up until rf voltage at channel A if J4 is 3 dB below level of step d. Note the input frequency. If less than the upper 3 dB frequency of the applicable filter in table 4, select value of associated passband adjust capacitors (refer to table 3) until the upper 3-dB frequency is not less than that listed in table 4.

4.3 CW Mode Strapping

Input to enable CW mode filter is strapped as required for special applications. If FL8 (16-kHz passband) is to be used, CW mode diode strapping is not required. Refer to table 5 for strap-filter selection for CW mode.

Table 3. Filter Amplifier Gain/Passband Component Selection.

BANDWIDTH SWITCH POSITION	FILTER	GAIN ADJUST	PASSBAND TRIM CAPACITORS
LSB	FL2	R31	C31, C34, C58, C64
A	FL3	R38	C38, C41, C59, C65
B	FL4	R3	C3, C6, C54, C60
C	FL5	R10	C10, C13, C55, C61
D	FL6	R17	C17, C20, C56, C62
E	FL7	R24	C24, C27, C57, C63

Table 4. Filter Passband Frequencies.

FILTER PASSBAND	RECEIVE IF INPUT	LOWER 3 dB (NMT)	UPPER 3 dB (NLT)
LSB 2.7 kHz	9.4517 MHz	9.450250 MHz	9.453000 MHz
AM 6 kHz	9.4500 MHz	9.447000 MHz	9.453000 MHz
AM 3 kHz	9.4500 MHz	9.448500 MHz	9.451500 MHz
AM 1 kHz	9.4500 MHz	9.449500 MHz	9.450500 MHz
USB 1 kHz	9.4490 MHz	9.448500 MHz	9.449500 MHz
AM 0.5 kHz	9.4500 MHz	9.449750 MHz	9.450250 MHz
USB 0.5 kHz	9.4490 MHz	9.448750 MHz	9.449250 MHz
AM 0.2 kHz	9.4500 MHz	9.449900 MHz	9.450100 MHz
USB 0.2 kHz	9.4490 MHz	9.448900 MHz	9.449100 MHz
AM 0.1 kHz	9.4500 MHz	9.449950 MHz	9.450050 MHz

Table 5. CW Mode Strapping.

INPUT	ANODE STRAP	DIODE	CATHODE STRAP	FILTER SELECTED
P8-1	E1	CR11	E2 E3 E4 E5	FL4 FL5 FL6 FL7

5. REPAIR

Repair of the filter card is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

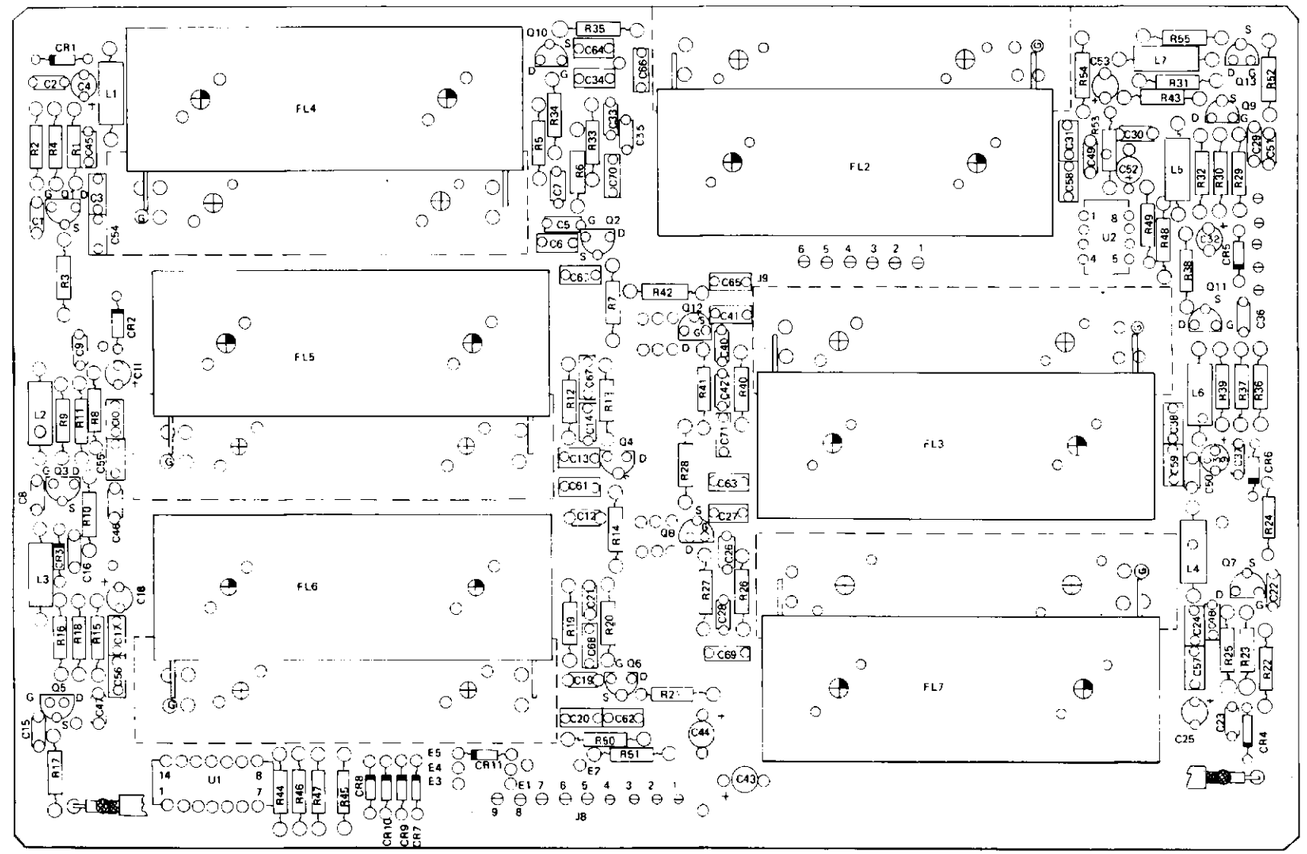
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figure 4). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description is listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points to the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Filter	637-2515-001	REV B
Filter	637-2515-002	REV C
Filter	637-2515-003	REV C
Filter	637-2515-004	REV D
Filter	637-2515-005	REV E
Filter	637-2515-006	REV F
Filter board	635-0905-001	REV—
Filter board	635-0905-002	REV—



Filter, Schematic Diagram
Figure 4 (Sheet 1 of 3)

PARTS LIST

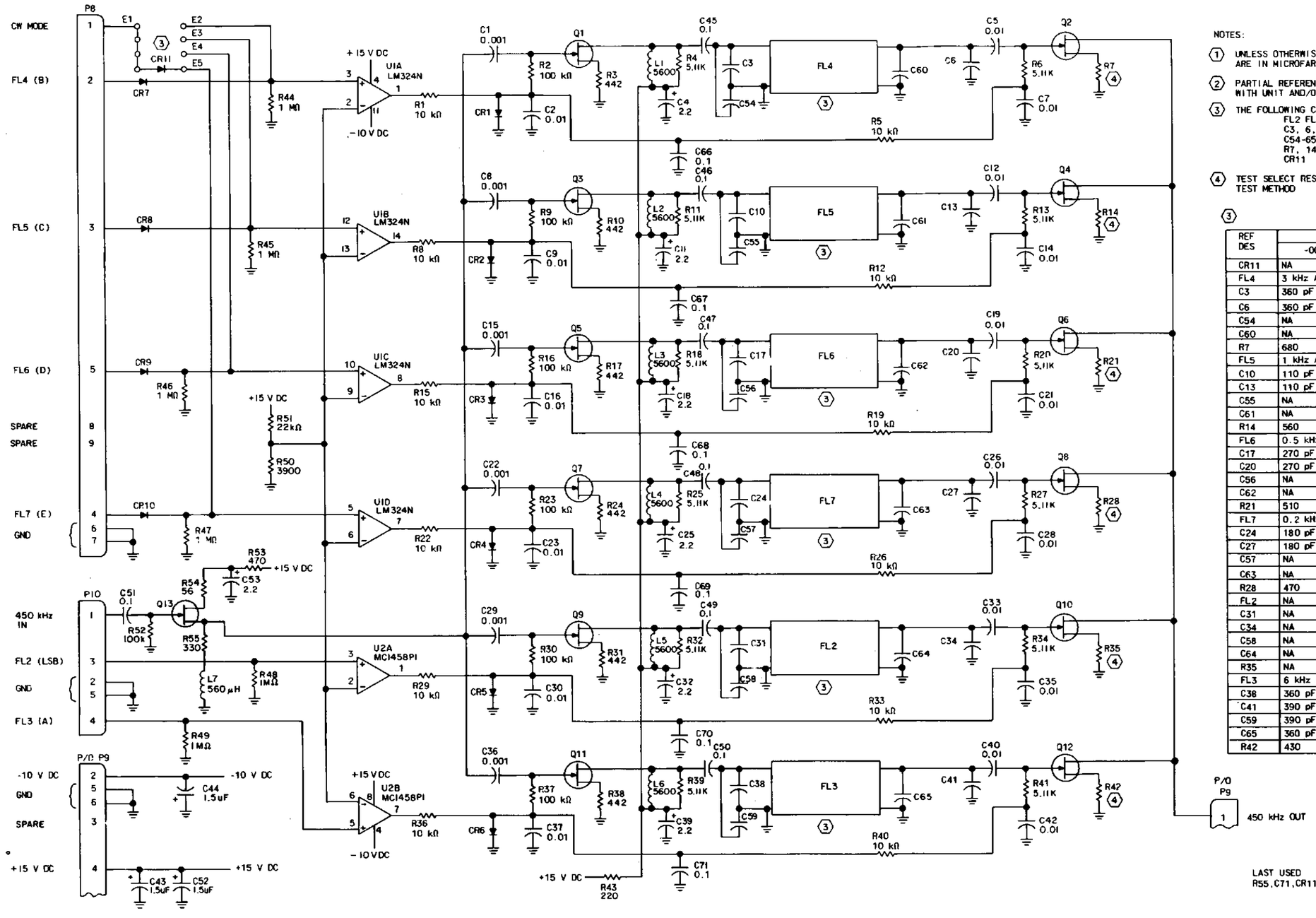
REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	FILTER 637-2515-001		A
	FILTER 637-2515-002		B
	FILTER 637-2515-003		C
	FILTER 637-2515-004		D
	FILTER 637-2515-005		E
	FILTER 637-2515-006		F
CR1-CR10	NOT USED		
CR11	SEMICOND DEVICE, 1N4454	353-3644-010	B
C1, C2	NOT USED		
C3	CAPACITOR, FXD, MICA DIEL, 360pF, 5%, 50V	912-4141-500	ACEF
C4, C5	NOT USED		
C6	CAPACITOR, FXD, MICA DIEL, 360pF, 5%, 50V	912-4141-500	ACEF
C7-C9	NOT USED		
C10	CAPACITOR, FXD, MICA DIEL, 110pF, 5%, 50V	912-4141-370	ACEF
C11, C12	NOT USED		
C13	CAPACITOR, FXD, MICA DIEL, 110pF, 5%, 50V	912-4141-370	ACEF
C14-C16	NOT USED		
C17	CAPACITOR, FXD, MICA DIEL, 270pF, 5%, 50V	912-4141-470	AEF
C17	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 50V	912-4141-050	C
C18, C19	NOT USED		
C20	CAPACITOR, FXD, MICA DIEL, 270pF, 5%, 50V	912-4141-470	AEF
C20	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 50 V	912-4141-050	C
C21-C23	NOT USED		
C24	CAPACITOR, FXD, MICA DIEL, 180pF, 5%, 50V	912-4141-430	ABCE
C25, C26	NOT USED		
C27	CAPACITOR, FXD, MICA DIEL, 180pF, 5%, 50V	912-4141-430	ABCE
C28-C30	NOT USED		
C31	CAPACITOR, FXD, MICA DIEL, 22pF, ±0.5pF, 300V	912-4141-030	DE
C32, C33	NOT USED		
C34	CAPACITOR, FXD, MICA DIEL, 22pF, ±0.5pF, 300V	912-4141-030	DE
C35-C37	NOT USED		
C38	CAPACITOR, FXD, MICA DIEL, 360 pF, 5%, 50V	912-4141-500	ABCEF
C39, C40	NOT USED		
C41	CAPACITOR, FXD, MICA DIEL, 390pF, 5%, 50V	912-4141-510	ABCEF
C42-C55	NOT USED		
C56	CAPACITOR, FXD, MICA DIEL, 150pF, 5%, 50V	912-4141-400	C
C57, C58	NOT USED		
C59	CAPACITOR, FXD, MICA DIEL, 390pF, 5%, 50V	912-4141-510	ABCEF
C60, C61	NOT USED		
C62	CAPACITOR, FXD, MICA DIEL, 150pF, 5%, 50V	912-4141-400	C
C63-C64	NOT USED		
C65	CAPACITOR, FXD, MICA DIEL, 360pF, 5%, 50V	912-4141-500	ABCEF
FL1	NOT USED		
FL2	FILTER, LSB, 2.7 kHz	526-9956-010	DE
FL3	FILTER, 6kHz AM BANDPASS	526-9963-060	ABCEF
FL4	FILTER, 3kHz AM BANDPASS	526-9963-040	ACEF
FL5	FILTER, 1kHz AM BANDPASS	526-9963-030	AEF
FL5	FILTER, 1kHz USB BANDPASS	526-9974-030	C
FL6	FILTER, 0.5kHz AM BANDPASS	526-9963-020	AEF
FL6	FILTER, 0.5kHz USB BANDPASS	526-9974-020	C
FL7	FILTER, 0.2kHz AM BANDPASS	526-9963-010	AE
FL7	FILTER, 0.2kHz USB BANDPASS	526-9974-010	BC
FL7	FILTER, 0.1kHz AM BANDPASS	293-1333-010	F
R1-R6	NOT USED		
R7	RESISTOR, FXD, CMPSN, 680Ω, 5%, 1/4W	745-0742-000	ACEF
R8-R13	NOT USED		
R14	RESISTOR, FXD, CMPSN, 560Ω, 5%, 1/4W	745-0739-000	AC
R15-R20	NOT USED		
R21	RESISTOR, FXD, CMPSN, 510Ω, 5%, 1/4W	745-0738-000	ACEF
R22-R27	NOT USED		
R28	RESISTOR, FXD, CMPSN, 470Ω, 5%, 1/4W	745-0736-000	ABCEF
R29-R34	NOT USED		
R35	RESISTOR, FXD, CMPSN, 430Ω, 5%, 1/4W	745-0735-000	D
R35	RESISTOR, FXD, CMPSN, 470Ω, 5%, 1/4W	745-0736-000	E
R36-R41	NOT USED		
R42	RESISTOR, FXD, CMPSN, 430Ω, 5%, 1/4W	745-0735-000	ABCEF
	CIRCUIT CARD ASSEMBLY	635-0905-001	ABCEF
	CIRCUIT CARD ASSEMBLY	635-0905-002	D

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	CIRCUIT CARD ASSEMBLY 635-0905-001		ABCEF
	CIRCUIT CARD ASSEMBLY 635-0905-002		D
CR1-CR4	SEMICOND DEVICE, 1N4454	353-3644-010	ABCEF
CR5	SEMICOND DEVICE, 1N4454	353-3644-010	
CR6-CR10	SEMICOND DEVICE, 1N4454	353-3644-010	ABCEF
C1	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 100V	913-4018-000	ABCEF
C2	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	ABCEF
C3	NOT USED		
C4	CAPACITOR, FXD, ELCTLT, 2.2μF, 20%, 25V	184-9102-220	ABCEF
C5	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	ABCEF
C6	NOT USED		
C7	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	ABCEF
C8	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	ABCEF
C9	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	ABCEF
C10	NOT USED		
C11	CAPACITOR, FXD, ELCTLT, 2.2 μF, 20%, 25V	184-9102-220	ABCEF
C12	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	ABCEF
C13	NOT USED		
C14	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	ABCEF
C15	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	ABCEF
C16	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	ABCEF
C17	NOT USED		
C18	CAPACITOR, FXD, ELCTLT, 2.2μF, 20%, 25V	184-9102-220	ABCEF
C19	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	ABCEF
C20	NOT USED		
C21	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	ABCEF
C22	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	ABCEF
C23	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	ABCEF
C24	NOT USED		
C25	CAPACITOR, FXD, ELCTLT, 2.2μF, 20%, 25V	184-9102-220	ABCEF
C26	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	ABCEF
C27	NOT USED		
C28	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	ABCEF
C29	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	914018-000	
C30	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	
C31	NOT USED		
C32	CAPACITOR, FXD, ELCTLT, 2.2μF, 20%, 25V	184-9102-220	
C33	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	
C34	NOT USED		
C35	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	
C36	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	ABCEF
C37	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	ABCEF
C38	NOT USED		
C39	CAPACITOR, FXD, ELCTLT, 2.2μF, 20%, 25V	184-9102-220	ABCEF
C40	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5014-200	ABCEF
C41	NOT USED		
C42	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	ABCEF
C43, C44	CAPACITOR, FXD, ELCTLT, 1.5μF, 20%, 35V	184-9102-800	
C45-C48	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	ABCEF
C49	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	
C50	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	ABCEF
C51	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	
C52	CAPACITOR, FXD, ELCTLT, 1.5μF, 20%, 35V	184-9102-800	
C53	CAPACITOR, FXD, ELCTLT, 2.2μF, 20%, 25V	184-9102-220	
C54-C65	NOT USED		
C66-C69	CAPACITOR, FXD, CER DIEL, 0.1μF, 10%, 100V	913-5019-440	ABCEF
C70	CAPACITOR, FXD, CER DIEL, 0.1μF, 10%, 100V	913-5019-440	
C71	CAPACITOR, FXD, CER DIEL, 0.1μF, 10%, 100v	913-5019-440	ABCEF
L1-L3	COIL, RF, SHIELDED, 5600μH	637-3767-001	ABCEF
L4	COIL, RF, 5600μH	240-2715-580	ABCEF
L5	COIL, RF, 5600μH	240-2715-580	
L6	COIL, RF, 5600μH	240-2715-580	ABCEF
L7	COIL, RF, 560μH	240-2715-460	
Q1-Q5	TRANSISTOR, FET, SPF557	352-1068-010	ABCEF
Q6, Q10	TRANSISTOR, FET, SPF557	352-1068-010	
Q11, Q12	TRANSISTOR, FET, SPF557	352-1068-010	ABCEF
Q13	TRANSISTOR, FET, SPF557	352-1068-010	
R1	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	AVCEF
R2	RESISTOR, FXD, CMPSN, 100kΩ, 10%, 1/4W	745-0821-000	ABCEF
R3	RESISTOR, FXD, FILM, 442Ω, 1%, 1/8W	705-0979-000	ABCEF
R4	RESISTOR, FXD, FILM, 5.11kΩ, 1%, 1/8W	705-1030-000	ABCEF

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
R5	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	ABCEF
R6	RESISTOR, FXD, FILM, 5.11kΩ, 1%, 1/8W	705-1030-000	ABCEF
R7	NOT USED		
R8	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	ABCEF
R9	RESISTOR, FXD, CMPSN, 100kΩ, 10%, 1/4W	745-0821-000	ABCEF
R10	RESISTOR, FXD, FILM, 442Ω, 1%, 1/8W	705-0979-000	ABCEF
R11	RESISTOR, FXD, FILM, 5.11kΩ, 1%, 1/8W	705-1030-000	ABCEF
R12	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	ABCEF
R13	RESISTOR, FXD, FILM, 5.11kΩ, 1%, 1/8W	705-1030-000	ABCEF
R14	NOT USED		
R15	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	ABCEF
R16	RESISTOR, FXD, CMPSN, 100kΩ, 10%, 1/4W	745-0821-000	ABCEF
R17	RESISTOR, FXD, FILM, 442Ω, 1%, 1/8W	705-0979-000	ABCEF
R18	RESISTOR, FXD, FILM, 5.11kΩ, 1%, 1/8W	705-1030-000	ABCEF
R19	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	ABCEF
R20	RESISTOR, FXD, FILM, 5.11kΩ, 1%, 1/8W	705-1030-000	ABCEF
R21	NOT USED		
R22	RESISTOR, FXD, CMPSN, 10kΩ, 10% 1/4W	745-0785-000	ABCEF
R23	RESISTOR, FXD, CMPSN, 100kΩ, 10%, 1/4W	745-0821-000	ABCEF
R24	RESISTOR, FXD, FILM, 442Ω, 1%, 1/8W	705-0979-000	ABCEF
R25	RESISTOR, FXD, FILM, 5.11kΩ, 1%, 1/8W	705-1030-000	ABCEF
R26	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	ABCEF
R27	RESISTOR, FXD, FILM, 5.11kΩ, 1%, 1/8W	705-1030-000	ABCEF
R28	NOT USED		
R29	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R30	RESISTOR, FXD, CMPSN, 100kΩ, 10%, 1/4W	745-0821-000	
R31	RESISTOR, FXD, FILM, 442Ω, 1%, 1/8W	705-0979-000	D
R32	RESISTOR, FXD, FILM, 5.11kΩ, 1%, 1/8W	705-1030-000	
R33	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R34	RESISTOR, FXD, FILM, 5.11kΩ, 1%, 1/8W	745-1030-000	
R35	NOT USED		
R36	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	ABCEF
R37	RESISTOR, FXD, CMPSN, 100kΩ, 10%, 1/4W	745-0821-000	ABCEF
R38	RESISTOR, FXD, FILM, 442Ω, 1%, 1/8W	705-0979-000	ABCEF
R39	RESISTOR, FXD, FILM, 5.11kΩ, 1%, 1/8W	705-1030-000	ABCEF
R40	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	ABCEF
R41	RESISTOR, FXD, FILM, 5.11kΩ, 1%, 1/8W	705-1030-000	ABCEF
R42	NOT USED		
R43	RESISTOR, FXD, CMPSN, 220Ω, 10%, 1/4W	745-0725-000	
R44-R47	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	ABCEF
R48, R49	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R50	RESISTOR, FXD, CMPSN, 3.9kΩ, 10%, 1/4W	745-0779-000	
R51	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R52	RESISTOR, FXD, CMPSN, 100kΩ, 10%, 1/4W	745-0821-000	
R53	RESISTOR, FXD, CMPSN, 470Ω, 10%, 1/4W	745-0737-000	
R54	RESISTOR, FXD, CMPSN, 56Ω, 10%, 1/4W	745-0704-000	
R55	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/4W	745-0731-000	
U1	INTEGRATED CKT, LM324N	351-1141-030	ABCEF
U2	INTEGRATED CKT, MC1458P1	351-1071-070	



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, DIODES ARE TYPE 1N4454, AND FETS ARE TYPE SPF557
2. PARTIAL REFERENCE DESIGNATORS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATIONS
3. THE FOLLOWING COMPONENTS ARE PART OF ASSEMBLY 637-2515-XXX
   FL2 FL7
   C3, 6, 10, 13, 17, 20, 24, 27, 31, 34, 38, 41
   C54-65
   R7, 14, 21, 28, 35, 42
   CR11
4. TEST SELECT RESISTOR 637-1468-001 MAY BE USED AS REQUIRED BY PRODUCTION TEST METHOD

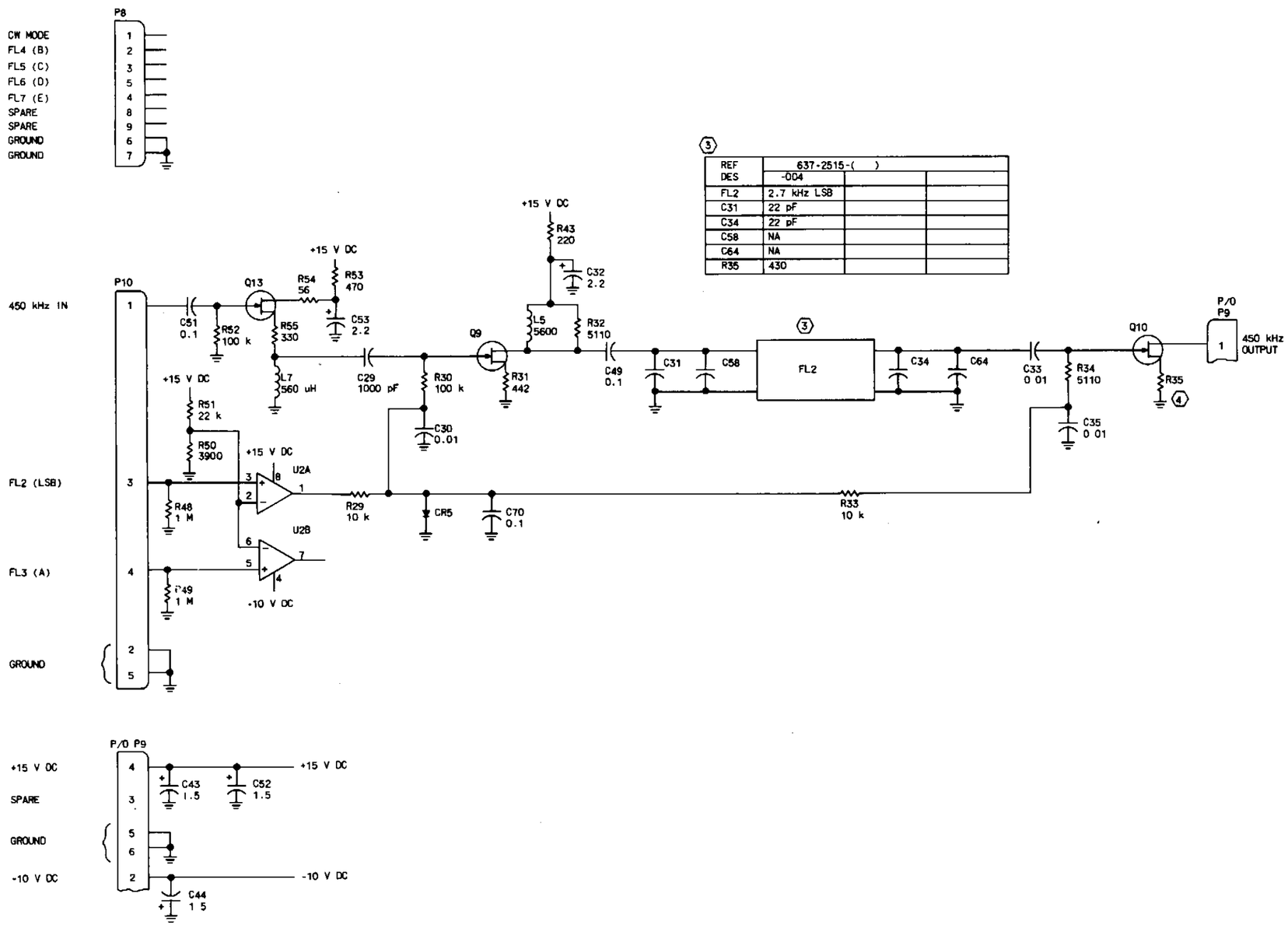
(3)

REF DES	637-2515-( )				
	-001	-002	-003	-005	-006
CR11	NA	E1-E5	NA	NA	NA
FL4	3 kHz AM	NA	3 kHz AM	3 kHz AM	3 kHz AM
C3	360 pF	NA	360 pF	360 pF	360 pF
C6	360 pF	NA	360 pF	360 pF	360 pF
C54	NA	NA	NA	NA	NA
C60	NA	NA	NA	NA	NA
R7	680	NA	680	680	680
FL5	1 kHz AM	NA	NA	1 kHz AM	1 kHz AM
C10	110 pF	NA	NA	110 pF	110 pF
C13	110 pF	NA	NA	110 pF	110 pF
C55	NA	NA	NA	NA	NA
C61	NA	NA	NA	NA	NA
R14	560	NA	NA	560	560
FL6	0.5 kHz AM	NA	NA	0.5 kHz AM	0.5 kHz AM
C17	270 pF	NA	NA	270 pF	270 pF
C20	270 pF	NA	NA	270 pF	270 pF
C56	NA	NA	NA	NA	NA
C62	NA	NA	NA	NA	NA
R21	510	NA	NA	510	510
FL7	0.2 kHz AM	0.2 kHz USB	0.2 kHz USB	0.2 kHz AM	0.1 kHz AM
C24	180 pF	180 pF	180 pF	180 pF	NA
C27	180 pF	180 pF	180 pF	180 pF	NA
C57	NA	NA	NA	NA	NA
C63	NA	NA	NA	NA	NA
R28	470	470	470	470	470
FL2	NA	NA	NA	2.75 kHz LSB	NA
C31	NA	NA	NA	22 pF	NA
C34	NA	NA	NA	22 pF	NA
C58	NA	NA	NA	NA	NA
C64	NA	NA	NA	NA	NA
R35	NA	NA	NA	470	NA
FL3	6 kHz AM	6 kHz AM	6 kHz AM	6 kHz AM	6 kHz AM
C38	360 pF	360 pF	360 pF	360 pF	360 pF
C41	390 pF	390 pF	390 pF	390 pF	390 pF
C59	390 pF	390 pF	390 pF	390 pF	390 pF
C65	360 pF	360 pF	360 pF	360 pF	360 pF
R42	430	430	430	430	430

LAST USED
R55, C71, CR11, U2, Q13, L7

635-0441

Filter, Schematic Diagram
Figure 4 (Sheet 3)



(3)

REF DES	637-2515-( ) -004		
FL2	2.7 kHz LSB		
C31	22 pF		
C34	22 pF		
C58	NA		
C64	NA		
R35	430		

NOTES:

(1) UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS. CAPACITANCE VALUES ARE IN MICROFARADS, DIODES ARE TYPE IN4454, AND FETS ARE TYPE SPF557.

(2) PARTIAL REFERENCE DESIGNATORS ARE SHOWN, FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATIONS

(3) THE FOLLOWING COMPONENTS ARE PART OF ASSEMBLY 637-2515-004.
FL2
C31, 34, 58, 64
R35

(4) TEST SELECT RESISTOR 637-1468-001 MAY BE USED AS REQUIRED BY PRODUCTION TEST METHOD.

(5) THIS DRAWING TO BE USED WITH 635-0905-002 AND ASSEMBLY 637-2515-004.

635-0441

Filter, Schematic Diagram
Figure 4 (Sheet 4)

RF Translator (637-1767-( ))

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

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1st Revision, 1 January 1979

1. DESCRIPTION

RF Translator 637-1767-( ), shown in figure 1, is a module enclosed in an rf secure compartment (metal box construction). The rf translator module contains a metal box subassembly with internal shielding between various circuit elements and three 2-layer planar cards. It uses a 56-pin edge-on connector (2 layers, 28 pins each) and four subminiax rf connectors for external connections.

The rf translator module consists of two mixers, a receive overload, and rf filter circuits.

The rf translator configuration differences are as follows:

a. 637-1767-001, FL14 109.350 00 MHz filter, ±7.50 kHz at 3-dB points (narrowband filter).
b. 637-1767-002, FL14 109.350 00 MHz filter, ±6.10 kHz at 0.5-dB points (broadband filter).

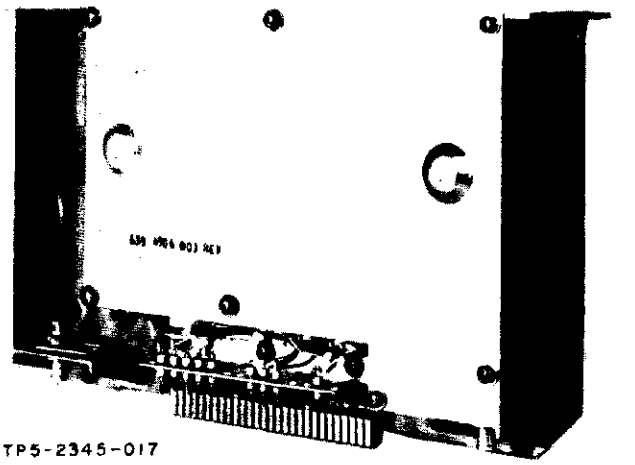
2. PRINCIPLES OF OPERATION

2.1 General (Refer to figure 2.)

The rf translator converts the 100-kHz (0.100-MHz) to 30.0-MHz receive rf input to a 9.45-MHz receive if frequency.

2.2 Receive Function (Refer to figure 2.)

When a receive signal is supplied to the rf translator, it is overload checked and supplied through K1 to the associated bandpass filter. If an overload exists, Q1 causes K1 to deenergize, and the receive rf is loaded through R4 and supplied as receive rf through K1 to the associated bandpass filter.

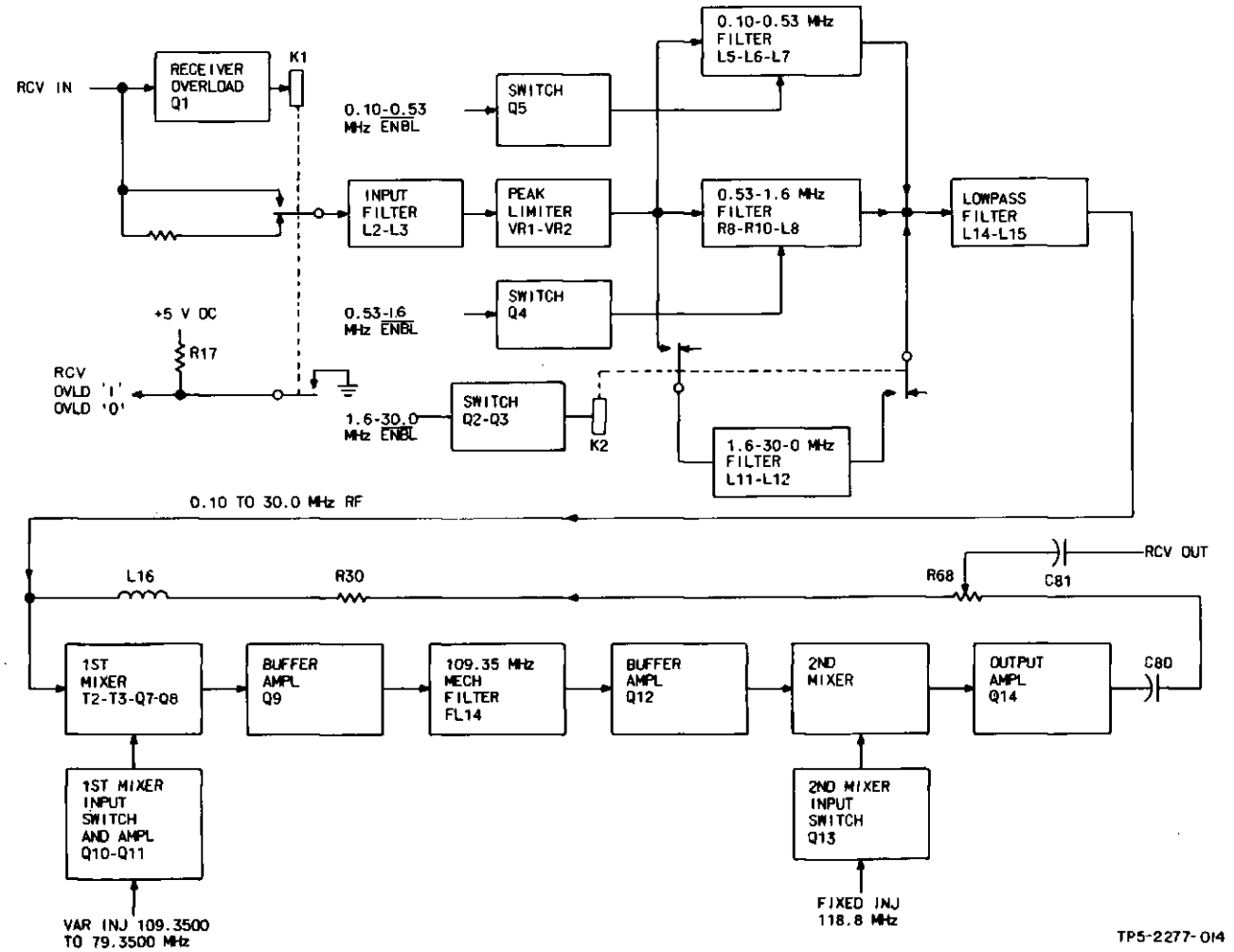


RF Translator
Figure 1

The bandpass filter is selected by the receiver frequency control. Enable signals from the receiver frequency control enable filter L5-L7 for 100- to 530-kHz (0.10- to 0.53-MHz) operation; enable filter R8-R10-L8 for 530-kHz to 1.6-MHz (0.53- to 1.6-MHz) operation; and energize K2 to enable filter L11-L12 for 1.6- to 30.0-MHz operation.

The signal from K1 is supplied through the selected bandpass filter and through low-pass filter L14-L15 to the grounded gate balanced FET first mixer circuit T1-T2, Q7-Q8.

In the first mixer the 100-kHz to 30.0-MHz signal is mixed with a 109.3500- to 79.3500-MHz variable injection signal to provide a 109.35-MHz if signal. This signal is supplied through source follower FET buffer amplifier Q9, mechanical filter FL14, and a second source follower FET buffer amplifier Q12 to the second mixer circuit.



Functional Block Diagram
Figure 2

In the second mixer the 109.35-MHz if signal is mixed with a 118.8-MHz fixed injection signal to provide a 9.45-MHz receive if output signal. The receive if output signal is supplied through output amplifier Q14, receive output switch CR24-CR25, and output control R68, to the rf translator receive if output.

2.3 RF Mixer SRA-1 (Refer to figure 3.)

The SRA-1 is a broadband ring modulator mixer device used in 50-ohm rf/if applications.

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

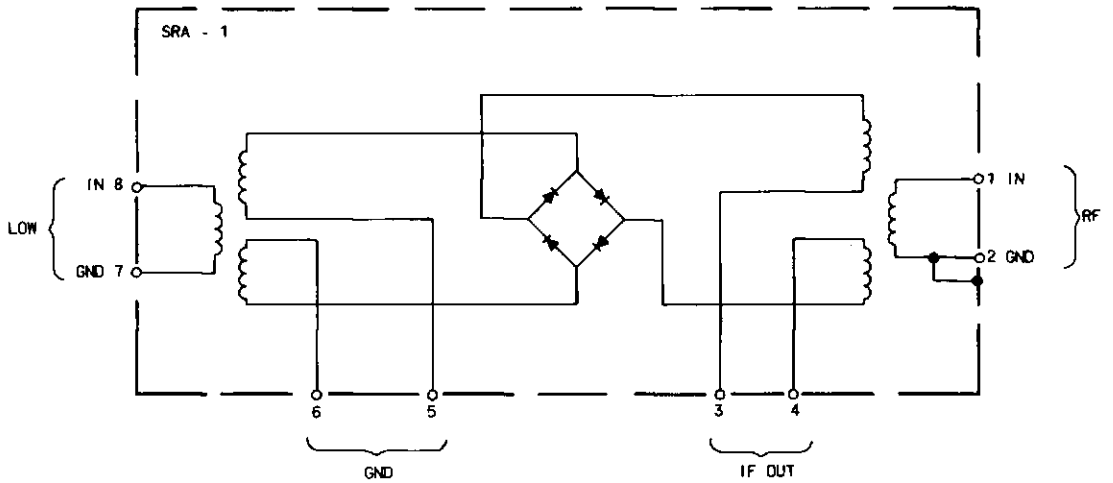
Test equipment and power sources required to test, troubleshoot, and repair the rf translator module are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 1 check total performance of the rf translator module. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

Note

In emergencies, RF Translator 637-1767-001 can be replaced by RF Translator 635-4903-001. In this type of repair, use the test procedures given in table 1 to test RF Translator 635-4903-001.



CHARACTERISTICS

PEAK INPUT POWER: 50 mW MAX.
PEAK CURRENT, ANY PORT: 40 mA MAX.
FREQUENCY RANGE (MHz):
LOW - 0.5 TO 500
RF - 0.5 TO 500
IF - DC TO 500
CONVERSION LOSS: 6.5 dB TYPICAL, 8.5 dB MAX. (SIGNAL AT IF PORT, OUTPUT AT RF PORT)
TEST CURRENT WHEN CHECKING CONTINUITY MUST NOT EXCEED 20 mA.

ISOLATION (dB):
LOW BAND EDGE;
LOW TO RF - 35 dB MIN.
LOW TO IF - 30 dB MIN
MID-RANGE;
LOW TO RF - 30 dB MIN.
LOW TO IF - 25 dB MIN.
UPPER BAND EDGE;
LOW TO RF - 25 dB MIN.
LOW TO IF - 20 dB MIN.

TP5-2278-013

RF Mixer SRA-1
Figure 3

Table 1. RF Translator, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of unit containing the rf translator that is to be tested.		
	b. Remove rf translator. Install rf translator on extender and place it in the unit.		
	c. Set unit LINE SELECTOR switch to 115 V.		
	d. Connect unit to 115-V ac power source and set power on.		
	e. Measure dc voltages between the following pins and ground (P1-1, 28, 29, 56):		
	P1-25 P1-53	+24.0 ±1.0 V dc	Check associated power supply.
	P1-23 P1-51	+15.0 ±1.0 V dc	
	P1-27	+5.0 ±0.2 V dc	
	P1-6	-15.0 ±1.0 V dc	

Table 1. RF Translator, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. Receiver SSB sensitivity	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.		
	b. Connect an rf signal generator to J1 (RW ANT jack on rear panel).		
	c. Connect an audio vtvm to A6TP2 (SSB audio).		
	d. Set the rf signal generator to 250.0 kHz and receiver front panel frequency controls to 249.0 kHz.		
	e. Set the rf signal generator level at 0.00 μV.		
	f. Note noise level on audio vtvm.	Reference	
	g. Adjust rf signal generator level to 0.30 μV and note signal level on audio vtvm.	NLT 2 dB above reference	Check M1, Q14, Q12, FL14, Q9, Q8, Q7, Q5, and associated circuits.
	h. Repeat steps e, f, and g with rf signal generator at each of the following frequencies: (receiver front panel frequency controls set 1000 Hz below each frequency given).	*Note* Signal strength of step g varies with frequency.	
	500 kHz	NLT 3 dB above reference	Same as step g.
	1.0 MHz	NLT 3 dB above reference	Check Q4 and associated circuits.
	1.6 MHz	NLT 10.5 dB above reference	Check Q2, Q3, K2, and associated circuits.
	5.0 MHz	NLT 10.5 dB above reference	Same as 1.6 MHz.
	10.0 MHz	NLT 10.5 dB above reference	
	15.0 MHz	NLT 10.5 dB above reference	
	20.0 MHz	NLT 10.5 dB above reference	
	25.0 MHz	NLT 10.5 dB above reference	
	30.0 MHz	NLT 10.5 dB above reference	
3. Receiver gain	a. Connect an rf signal generator to J1 (RCV ANT jack on rear panel).		
	b. Connect an rf vtvm (with 50-Ω load) to J3.		
	c. Set the rf signal generator and receiver front panel frequency controls to 1.600 MHz.		
(Cont)	d. Set the rf signal generator level at -30 dB mW.		

Table 1. RF Translator, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	e. Note the signal level on the rf vtvm.	NLT -12.0 dB mW	Same as test 2.
	f. Repeat steps d and e at each of the following frequencies:		
	5.0 MHz	NLT -11.5 dB mW	
	10.0 MHz	NLT -11.5 dB mW	
	15.0 MHz	NLT -10.1 dB mW	
	20.0 MHz	NLT -11.5 dB mW	
	25.0 MHz	NLT -11.5 dB mW	
	29.9 MHz	NLT -11.1 dB mW	
4. Receiver overload protection	a. Connect an rf signal generator to J1 (RCV ANT jack on rear panel).		
	b. Connect a dvm to P1-3. Note voltage.	0 V	Check Q1, K1, and associated circuits.
	c. Set the rf signal generator and the receiver front panel frequency controls to 500 kHz.		
	d. Increase the rf signal generator output level until the receive overload relay just clicks.		
	e. Note rf output level of rf signal generator.	1.4 to 1.9 V rms	Same as step b.
	f. Note dvm reading.	NLT +3.0 V dc	Check K1 and associated output circuit.
	g. Remove rf signal generator.		
5. Receive AGC	a. Remove rf translator from extenders and install it in unit.		
	b. Remove channel A if. Install it on extender card and place it in unit.		
	c. Connect an rf signal generator to J1 (RCV ANT jack on rear panel).		
	d. Connect an rf vtvm (with high impedance probe) to J3 (A8J1).		
	e. Set front panel AGC switch to OFF.		
	f. Set the rf signal generator and receiver front panel frequency controls to 15.0000 MHz.		
	g. Set the rf signal generator level at -30 dB mW.		
	h. Note the signal level on the rf vtvm.	Reference	
	i. Set front panel AGC switch to FAST.		
(Cont)	j. Increase rf signal generator level until reference on rf vtvm is reached.		

Table 1. RF Translator, Testing and Troubleshooting Procedures (Cont).

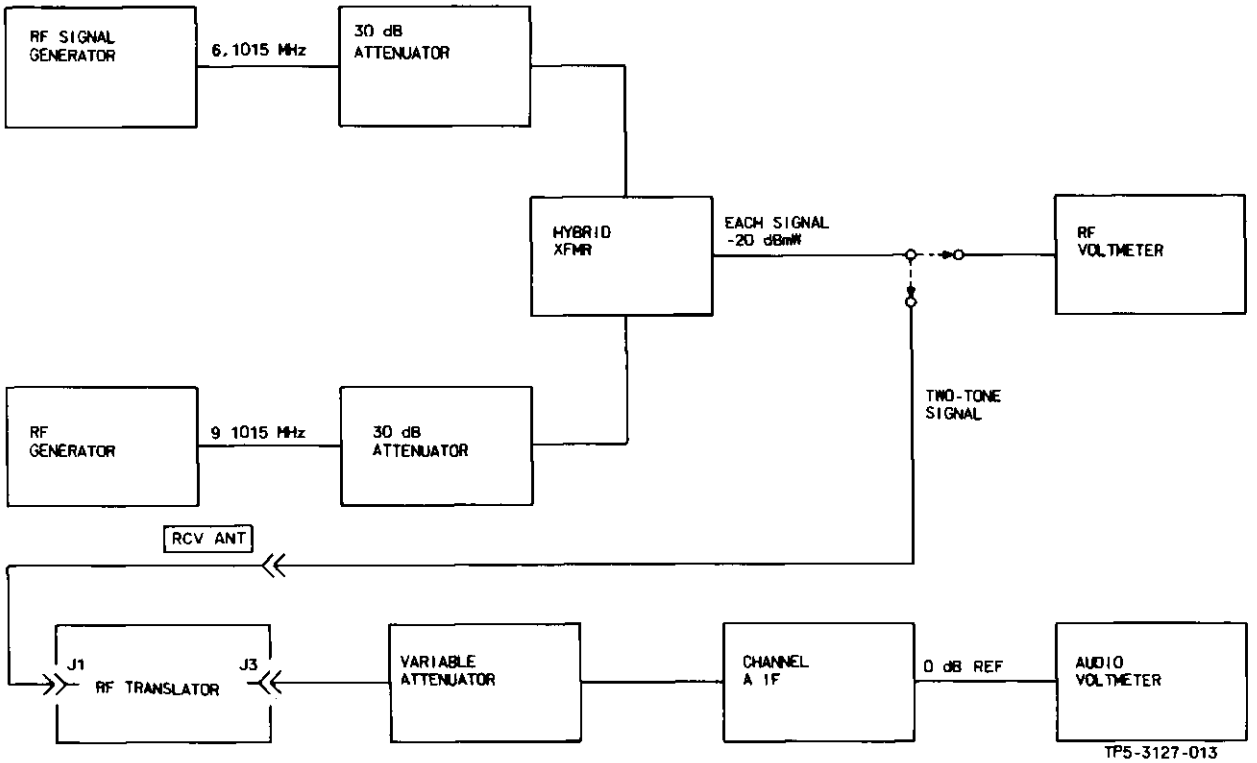
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	k. Note increase in rf signal generator level.	37 to 43 dB	Check CR19, CR20, CR22, CR23, and associated circuits.
	l. Remove channel A if from extenders and install it in unit.		
	m. Remove rf translator. Install it on extender card and place it in unit.		
6. Filter ripple	a. Connect an rf signal generator to J1 (RCV ANT jack on rear panel).		
	b. Connect an rf vtvm (with 50-Ω load) to J3.		
	c. Set the rf signal generator and receiver front panel frequency controls to 15.0000 MHz.		
	d. Set the rf signal generator level for -10-dB mW rf vtvm reading.	Reference	
	e. Adjust the rf signal generator down to 14.9970 MHz and up to 15.0030 MHz while noting the variation in the rf vtvm reading.	NMT 0.7-dB variation	Check M1, FL14, and associated circuits. If only slightly out of tolerance, adjustment of L24 and L20 may remedy indication.
	f. Adjust the rf signal generator down to 14.9940 MHz and up to 15.0060 MHz while noting the variation in the rf vtvm reading.	NMT 5.0-dB variation	Same as step e.
7. Receiver intermodulation, 3rd order products	a. Connect two rf signal generators to rf translator as shown in figure 4.		
	b. Set one rf signal generator to 6.1015 MHz.		
	c. Set the second rf signal generator to 9.1015 MHz.		
	d. Using the rf vtvm (with 50-Ω load) connected at the output of the hybrid transformer, independently adjust each rf signal generator for -20-dB mW outputs.		
	e. Connect the two-tone signal to J1 (RCV ANT jack on rear panel).		
	f. Set the receiver front panel frequency controls to 3000.00 kHz.		
	g. Slightly adjust (300 to 2000 Hz) the frequency of the 6.1015-MHz generator for a peak audio output (at A6TP2) as indicated on the audio voltmeter.		
(Cont)	h. Adjust the variable attenuator for 0-dB reference on the audio voltmeter.	Reference	

Table 1. RF Translator, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
7. (Cont)	**Note** Adjust variable attenuator for a 0-dB reference at point where AGC just begins to affect the audio output.	Reference	
	i. Note 6.1015-MHz rf signal generator output.		
	j. Set the receiver front panel frequency controls to 6100.00 kHz.		
	k. Slightly adjust the frequency of the 6.1015-MHz generator for a peak audio output as indicated on the audio voltmeter.		
	l. Adjust the output level of the rf signal generator for 0-dB reference in step h on the audio voltmeter.		
	m. Note the decrease in dB of the rf signal generator output from that referenced in step i.	NLT 83 dB down	To repair, return to factory
	n. Repeat steps g through m with the receiver front panel frequency controls at each of the following settings:		
	12100.00 kHz	NLT 83 dB down	Same as step m.
	21300.00 kHz	NLT 83 dB down	
	24300.00 kHz	NLT 83 dB down	
8. Receiver intermodulation, 2nd order products	a. Connect two rf signal generators to rf translator as shown in figure 4.		
	b. Set one rf signal generator to 6.1015 MHz.		
	c. Set the second rf signal generator to 9.1015 MHz.		
	d. Using the rf vtvm (with 50-Ω load) connected at the output of the hybrid transformer, independently adjust each rf signal generator for -20-dB mW outputs.		
	e. Connect the two-tone signal to J1 (RCV ANT jack on rear panel).		
	f. Set the receiver front panel frequency controls to 3000.00 kHz.		
	g. Slightly adjust (300 to 2000 Hz) the frequency of the 6.1015-MHz generator for a peak audio output (at A6TP2) as indicated on the audio voltmeter.		
(Cont)	h. Adjust the variable attenuator for 0-dB reference on the audio voltmeter.	Reference	

Table 1. RF Translator, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
8. (Cont)	**Note** Adjust variable attenuator for a 0-dB reference at point where AGC just begins to affect the audio output.	Reference	
	i. Note 6.1015-MHz rf signal generator output.		
	j. Set the receiver front panel frequency controls to 6100.00 kHz.		
	k. Slightly adjust the frequency of the 6.1015-MHz generator for a peak audio output as indicated on the audio voltmeter.		
	l. Adjust the output level on the rf signal generator for 0-dB reference in step h on the audio voltmeter.		
	m. Note the decrease in dB of the rf signal generator output from that referenced in step i.	NLT 70 dB down	To repair, return to factory.
	n. Repeat steps g through m with the receiver front panel frequency controls at 15 200.00 kHz.	NLT 70 dB down	Same as step m.



Receive Intermodulation Test Setup
Figure 4

4. ALIGNMENT/ADJUSTMENT

4.1 Receiver Alignment (Adjustment of T3, L24, L26, and L29)

a. Connect an rf signal generator through a 6-dB load to J1 (RCV ANT jack on rear panel).
b. Connect an rf vtvm (with 50-Ω load) to J3.
c. Set input to J1 at 15.0000 MHz and -30 dB mW.
d. Set front panel controls for 15 000.0 kHz.
e. Set R68 (receive gain) at full counterclockwise position.
f. Adjust T3, L24, L26, and L29 for maximum output, as indicated by vf vtvm.
g. Perform step f a minimum of three times.

4.2 Mixer Balance (Adjustment of R31)

a. Use a dvm with a 10-μH choke in series with a test probe to measure voltage readings at T2-2 and T2-5 to ground.
b. Adjust R31 for equal dc voltage reading at T2-2 and T2-5 to ground.

4.3 Injection Level Adjustment (Adjustment of T4)

a. Connect an rf vtvm (set to 10-V scale) between T2-1 and ground.
b. Vary input frequency from 2.0 to 29.9 MHz, and note that voltage varies between 3.0 and 7.0 V rms and that the higher voltage readings occur between 27 and 29.9 MHz.
c. If voltage exceeds the limits of step b or is higher at other than 27 to 29.9 MHz, adjust slug of T4 to achieve the desired levels.

4.4 Translator Gain Adjustment (Adjustment of R68, T1, and T2)

a. Set the rf signal generator for 15.000 00 MHz at -30 dB mW and the front panel frequency controls to 15 000.00 kHz.
b. Connect an rf vtvm (with 50-Ω load) to J3.
c. Adjust R68 for -10-dB mW reading on the rf vtvm.
d. Set the rf signal generator for 29.9000 MHz at -30 dB mW and the front panel frequency controls to 15 000.00 kHz.
e. Using a pointed plastic tool, carefully adjust the leads and windings of T1 and T2 for maximum reading on the rf vtvm.

Note

The objective is to make the output at 29.900 00 MHz as large as possible with an output difference between 29.900 00 and 15.000 00 MHz of not more than 1.0 dB.

f. Repeat steps c, d, and e until no improvement is possible.

4.5 Final Noise Balance (Adjustment of R31)

a. Set the front panel frequency controls for 15 000.00 kHz and disconnect the rf signal generator.
b. Connect an audio voltmeter to the channel A if SSB audio output. Reference the background noise level on the audio voltmeter.
c. Adjust R31 (20-turn potentiometer) for a minimum noise level. Make this adjustment very slowly to assure a true minimum.

4.6 T1 and T2 Position Fixing

Note

If T1 and T2 require position fixing, it is recommended that the rf translator be returned to the factory. If field repair of T1 and T2 is desired, the following procedures may be used. Do not make these adjustments unless repair has been made to the T1 and/or T2 area of the rf translator.

a. Set the rf signal generator for 29.900 00 MHz at -24 dB mW and the front panel frequency controls to 15 000.00 kHz.
b. Connect an rf vtvm (with 50-Ω load) to J3. Reference the rf vtvm reading.
c. Using a pipe cleaner, carefully apply a very thin coat of Q-Max to the windings of T1 and T2 and the support rods that hold T1 and T2 in position.
d. After Q-Max is applied, it may be necessary to slightly readjust wires for maximum output. Refer to paragraph 4.4.

5. REPAIR

Repair of the rf translator module is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

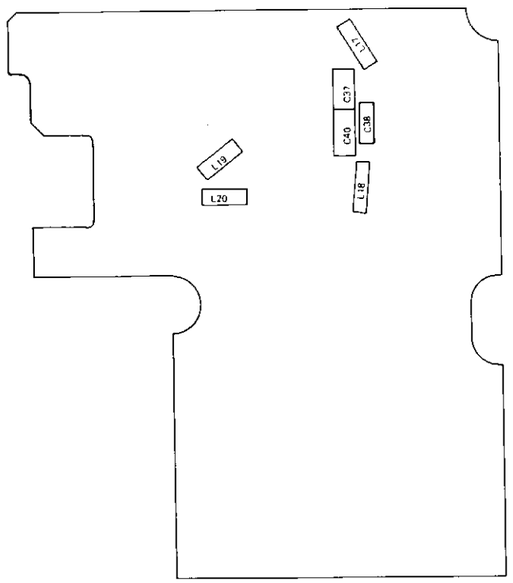
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram, figure 4. The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

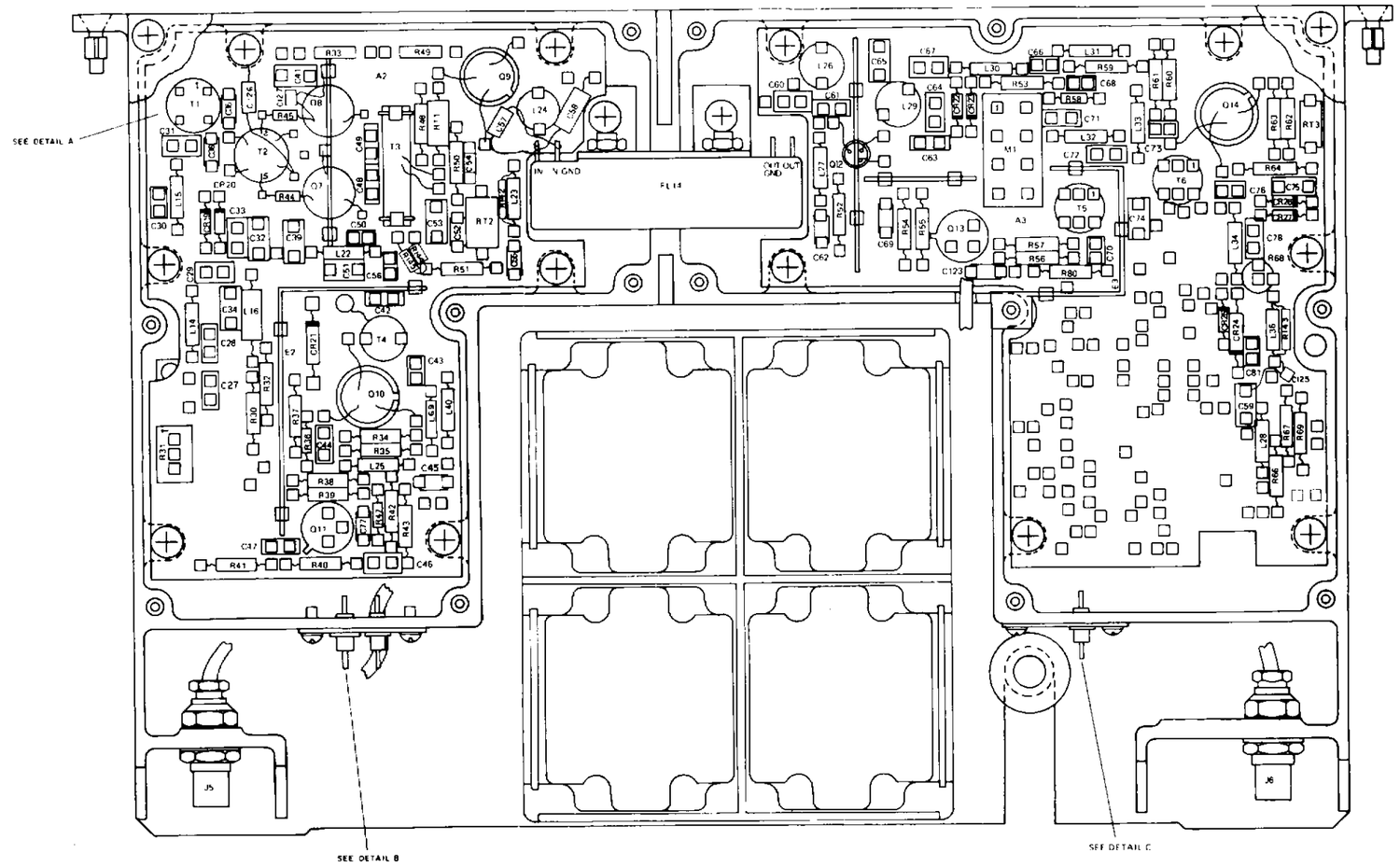
Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points to the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Rf translator module	637-1767-001	REV P
Rf translator module	637-1767-002	REV P
Rf filter board A1	635-0780-002	REV H
First mixer board A2	635-0782-002	REV L
Second mixer board A3	635-0784-002	REV J



DETAIL A



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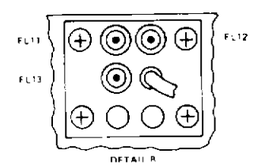
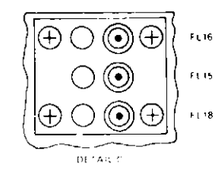


DETAIL B



DETAIL C

TP5-1239-039

RF Translator, Schematic Diagram
Figure 5 (Sheet 1 of 6)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	RF TRANSLATOR 637-1767-001		
	RF TRANSLATOR 637-1767-002		
A1	RF FILTER BOARD	635-0780-002	
A2	FIRST MIXER BOARD	635-0782-002	
A3	SECOND MIXER BOARD	635-0784-002	
C1-C56	NOT USED		
C57	CAPACITOR, FXD, MICA DIEL, 56pF, 5%, 50V (B3)	912-4141-310	A
C57	CAPACITOR, FXD, MICA DIEL, 68pF, 5%, 50V	912-4141-330	
C58	CAPACITOR, FXD, MICA DIEL, 56pF, 5%, 50V (B3)	912-4141-310	A
C58	CAPACITOR, FXD, MICA DIEL, 47pF, 5%, 50V	912-4141-280	
C59-C125	NOT USED		
	CAPACITOR, TEST SELECT		
C126	CAPACITOR, FXD, MICA DIEL, 2pF, ±0.5pF, 300V (A2)	912-4141-540	
C126	CAPACITOR, FXD, MICA DIEL, 3pF, ±0.5pF, 300V (A2)	912-4141-070	
C126	CAPACITOR, FXD, MICA DIEL, 4pF, ±0.5pF, 300V (A2)	912-4141-080	
C126	CAPACITOR, FXD, MICA DIEL, 5pF, ±0.5pF, 300V (A2)	912-4141-010	
C126	CAPACITOR, FXD, MICA DIEL, 6pF, ±0.5pF, 300V (A2)	912-4141-090	
	CAPACITOR, TEST SELECT		
C127	CAPACITOR, FXD, MICA DIEL, 1pF, ±0.5pF, 300V (A8)	912-4141-060	
C127	CAPACITOR, FXD, MICA DIEL, 2pF, ±0.5pF, 300V (A8)	912-4141-540	
C130-C132	CAPACITOR, FXD, ELCTLT, 2.2μF, 20%, 25V (B1)	184-9102-220	A
C130-C132	CAPACITOR, FXD, ELCTLT, 2.2μF, 20%, 25V	184-9102-220	B
C133	CAPACITOR, FXD, ELCTLT, 22μF, 20%, 10V (B1)	184-9102-080	A
C133	CAPACITOR, FXD, ELCTLT, 22μF, 20%, 10V	184-9102-080	B
FL1-FL13	FILTER, RAD INTR, 1750pF	241-5006-010	
FL14	FILTER, BP, 109.35 MHZ	293-1222-030	A
FL14	FILTER, BP, 109.35 MHZ	293-1330-010	B
FL15, FL16	FILTER, RAD INTR, 1750pF	241-5006-010	
FL17	NOT USED		
FL18	FILTER, RAD INTR, 1750pF	241-5006-010	
FL19, FL20	NOT USED		
FL21	FILTER, RAD INTR, 1750pF	241-5006-010	
FL22-FL32	NOT USED		
FL33-FL36	FILTER, RAD INTR, 1750pF	241-5006-010	
FL37-FL55	NOT USED		
FL56	FILTER, RAD INTR, 1750pF	241-5006-010	
J1	CONNECTOR, RCPT, ELEC	372-7207-030	
J2	NOT USED		
J3	CONNECTOR, RCPT, ELEC	372-7207-030	
J4	NOT USED		
J5, J6	CONNECTOR, RCPT, ELEC	372-7207-030	
L1-L43	NOT USED		
L44-L47	COIL, RF, 220μH	240-2723-060	
L48-L56	NOT USED		
L57	COIL, RF, 12μH	240-1581-000	
L58	COIL, RF, 470μH (B1)	240-2711-210	A
L58	COIL, RF, 120μH	240-2715-380	
L59, L60	COIL, RF, 15μH	240-1602-000	
Q1-Q8	NOT USED		
Q9	TRANSISTOR, FET, U322 (TEST SELECT)	637-9117-002	
Q10	TRANSISTOR, 2N5109	352-0766-010	
Q11-Q13	NOT USED		
Q14	TRANSISTOR, 2N5109	352-0766-010	
R1-R16	NOT USED		
R17	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R18-R138	NOT USED		
R139	RESISTOR, FXD, CMPSN, 180Ω, 10%, 1/4W (A11)	745-0722-000	A

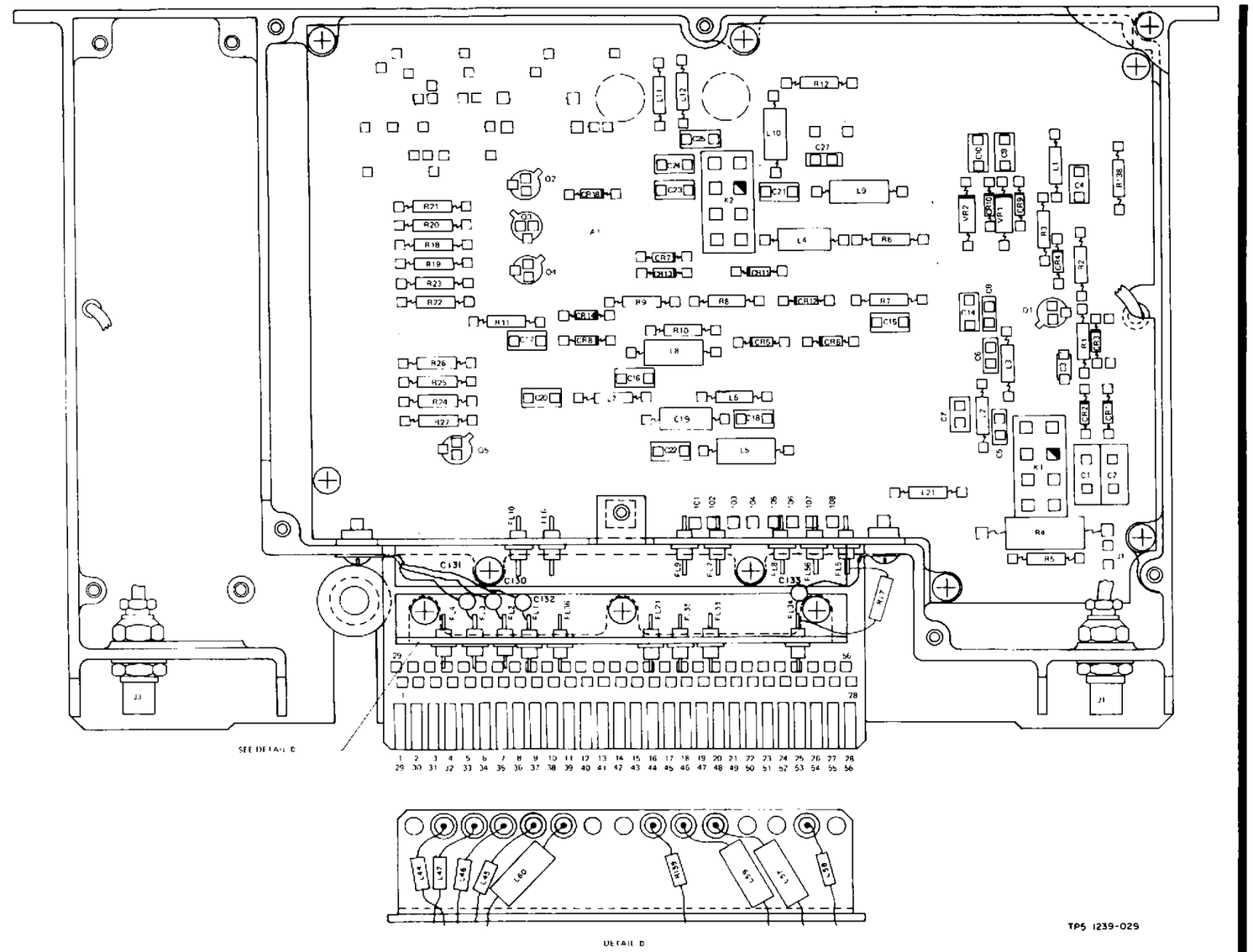
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	RESISTOR, TEST SELECT		
R139	RESISTOR, FXD, CMPSN, 82Ω, 10%, 1/4W	745-0710-000	
R139	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R139	RESISTOR, FXD, CMPSN, 150Ω, 10%, 1/4W	745-0719-000	
R139	RESISTOR, FXD, CMPSN, 180Ω, 10%, 1/4W	745-0722-000	
R139	RESISTOR, FXD, CMPSN, 270Ω, 10%, 1/4W	745-0728-000	
	RF FILTER BOARD A1 635-0780-002		
CR1-CR14	SEMICOND DEVICE, 1N4454	353-3644-010	
CR15-CR17	NOT USED		
CR18	SEMICOND DEVICE, 1N4454	353-3644-010	
C1	CAPACITOR, FXD, MICA DIEL, 180pF, 5%, 500V	912-2834-000	
C2	CAPACITOR, FXD, MICA DIEL, 330pF, 5%, 500V	912-2852-000	
C3	CAPACITOR, FXD, ELCTLT, 4.7μF, 20%, 35V	184-9102-390	
C4	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C5	CAPACITOR, FXD, MICA DIEL, 3pF, ±0.5pF, 300V	912-4141-070	
C6	CAPACITOR, FXD, MICA DIEL, 18pF, ±0.5pF, 100V	912-4141-140	
C7	CAPACITOR, FXD, MICA DIEL, 200pF, 5%, 50V	912-4141-440	
C8	CAPACITOR, FXD, MICA DIEL, 91pF, 5%, 50V	912-4141-360	
C9, C10	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C11-C13	NOT USED		
C14-C17	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C18	CAPACITOR, FXD, CER DIEL, 3300pF, 10%, 100V	913-3281-170	
C19	CAPACITOR, FXD, PLSTC DIEL, 0.015μF, 5%, 150V	933-1084-030	
C20	CAPACITOR, FXD, CER DIEL, 3300pF, 10%, 100V	913-3281-170	
C21, C22	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C23	CAPACITOR, FXD, CER DIEL, 3300pF, 10%, 100V	913-3281-170	
C24	CAPACITOR, FXD, CER DIEL, 1500pF, 10%, 100V	913-3281-140	
C25	CAPACITOR, FXD, CER DIEL, 3300pF, 10%, 100V	913-3281-170	
C26	NOT USED		
C27	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 50V	912-4141-050	
K1, K2	RELAY, AMT	974-1065-090	
L1	COIL, RF, 220μH	240-2723-060	
L2, L3	COIL, RF, 0.33μH	240-2745-010	
L4	COIL, RF, 220μH	240-2524-000	
L5	COIL, RF, 1000μH	240-2540-000	
L6, L7	COIL, RF, 27μH	240-2040-000	
L8, L9	COIL, RF, 1000μH	240-2540-000	
L10	COIL, RF, 220μH	240-2524-000	
L11, L12	COIL, RF, 2.20μH	240-2715-190	
L13-L20	NOT USED		
L21	COIL, RF, 220μH	240-2723-060	
Q1, Q2	TRANSISTOR, 2N2222A	352-0661-020	
Q3-Q5	TRANSISTOR, 2N2907A	352-0551-010	
R1	RESISTOR, FXD, CMPSN, 2.7kΩ, 10%, 1/4W	745-0764-000	
R2	RESISTOR, FXD, CMPSN, 68kΩ, 10%, 1/4W	745-0815-000	
R3	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W	745-0749-000	
R4	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 1W (B2)	745-3366-000	
R4	RESISTOR, FXD, CMPSN, 15kΩ, 10%, 1W	745-3401-000	
R5	RESISTOR, FXD, CMPSN, 47Ω, 10%, 1/4W	745-0701-000	
R6	RESISTOR, FXD, CMPSN, 82Ω, 10%, 1/4W	745-0710-000	
R7	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W	745-0749-000	
R8, R9	RESISTOR, FXD, CMPSN, 27Ω, 10%, 1/4W	745-0692-000	
R10	RESISTOR, FXD, CMPSN, 68Ω, 10%, 1/4W	745-0707-000	
R11	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W	745-0749-000	
R12	RESISTOR, FXD, CMPSN, 82Ω, 10%, 1/4W	745-0710-000	
R13-R17	NOT USED		
R18	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R19	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 1/4W	745-0761-000	
R20	RESISTOR, FXDD° CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R21	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 1/4W	745-0761-000	
R22	RESISTOR, FXD, CMPSN, 3.3kΩ, 10%, 1/4W	745-0767-000	
R23	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R24	RESISTOR, FXD, CMPSN, 1.2kΩ, 10%, 1/4W	745-0752-000	
R25	RESISTOR, FXD, CMPSN, 3.3kΩ, 10%, 1/4W	745-0767-000	
R26	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R27	RESISTOR, FXD, CMPSN, 1.2kΩ, 10%, 1/4W	745-0752-000	
R28-R137	NOT USED		
R138	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
VR1, VR2	SEMICOND DEVICE, 1N753A	353-2714-000	

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	FIRST MIXER BOARD A2 635-0782-002		
CR1-CR18	NOT USED		
CR19, CR20	SEMICOND DEVICE, 1N5767	922-6119-010	
CR21	SEMICOND DEVICE, 1N4001	353-6442-010	
C1-C27	NOT USED		
C28	CAPACITOR, FXD, MICA DIEL, 27pF, 5%, 50V	912-4141-180	
C29	CAPACITOR, FXD, MICA DIEL, 150pF, 5%, 50V	912-4141-400	
C30	CAPACITOR, FXD, MICA DIEL, 12pF, ±0.5pF, 300V	912-4141-120	
C31	CAPACITOR, FXD, MICA DIEL, 36pF, 5%, 50V	912-4141-240	
C32	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C33	CAPACITOR, FXD, MICA DIEL, 240pF, 5%, 50V	912-4141-460	
C34	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C35, C36	CAPACITOR, FXD, CER DIEL, 0.047μF, 10%, 50V	913-5019-280	
C37	CAPACITOR, FXD, MICA DIEL, 180pF, 5%, 50V	912-4141-430	
C38	CAPACITOR, FXD, CER DIEL, 0.047μF, 10%, 50V	913-5019-280	
C39	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C40	CAPACITOR, FXD, MICA DIEL, 180pF, 5%, 50V	912-4141-430	
C41	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C42	CAPACITOR, FXD, MICA DIEL, 22pF, ±0.5pF, 300V	912-4141-030	
C43	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C44	CAPACITOR, FXD, MICA DIEL, 33pF, 2%, 50V	912-4141-210	
C45	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C46	CAPACITOR, FXD, MICA DIEL, 5pF, ±0.5pF, 300V (A10)	912-4141-010	
C46	CAPACITOR, FXD, MICA DIEL, 5pF, ±0.5pF, 300V	912-4141-010	
C47	CAPACITOR, FXD, MICA DIEL, 51pF, 5%, 50V (A10)	912-4141-300	
C47	CAPACITOR, FXD, MICA DIEL, 330pF, 5%, 50V	912-4141-490	
C48, C49	CAPACITOR, FXD, MICA DIEL, 18pF, ±0.5pF, 100V (A5)	912-4141-140	
C48, C49	CAPACITOR, FXD, MICA DIEL, 20pF, ±0.5pF, 100V	912-4141-150	
C50	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C51	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C52	CAPACITOR, FXD, CER DIEL, 470pF, 10%, 200V	913-4014-000	
C53	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C54, C55	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C56	CAPACITOR° FXD, CER DIEL, 1000pF, 20%, 50V	913-3279-030	
C57, C58	(SEE 637-1767-001 OR 637-1768-001)		
C59-C76	NOT USED		
C77	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 100V (A5)	913-4018-000	
C77	CAPACITOR, FXD, CER DIEL, 56pF, 5%, 50V (A10)	912-4141-310	
C77	CAPACITOR, FXD, MICA DIEL, 47pF, 5%, 50V	912-4141-280	
L1-L13	NOT USED		
L14	COIL, RF, 0.22μH	240-2015-000	
L15	COIL, RF, 0.27μH	240-2018-000	
L16	COIL, RF, 220μH	240-2723-060	
L17, L18	COIL, RF, 2.70μH	240-2028-000	
L19, L20	COIL, RF, 1.0μH (A5)	240-2028-000	
L19, L20	COIL, RF, 1.0μH	240-2023-000	
L21	NOT USED		
L22, L23	COIL, RF, 2.70μH	240-2028-000	
L24	COIL, RF, VAR	242-0439-030	
L25	COIL, RF, 0.15μH	240-2013-000	
L26-L39	NOT USED		
L40	COIL, RF, 2.70μH	240-2028-000	
L41-L68	NOT USED		
L69	COIL, RF, 0.15μH (A5)	240-2013-000	
Q1-Q6	NOT USED		
Q7, Q8	TRANSISTOR, FET, U322 (MATCHED SET)	637-9117-001	
Q9, Q10	(SEE 637-1767-001 OR 637-1768-001)		
Q11	TRANSISTOR, 2N5109	352-0766-010	
RT1	RESISTOR, THRM, 40Ω, 10%, 0.5W	714-1725-000	
RT2	RESISTOR, THRM, 100Ω, 10%, 1W	714-1730-000	
R1-29	NOT USED		
R30	RESISTOR, FXD, CMPSN, 68Ω, 10%, 1/4W	745-0707-000	
R31	RESISTOR, VAR, 1kΩ, 5%, 3/4W	381-1853-170	
R32	RESISTOR, FXD, FILM, 226Ω, 1%, 1/8W	705-0965-000	
R33	RESISTOR, FXD, FILM, 681Ω, 1%, 1/8W	705-0988-000	
R34	RESISTOR, FXD, CMPSN, 4.7Ω, 5%, 1/4W	745-4382-000	
R35	RESISTOR, FXD, CMPSN, 3.3kΩ, 10%, 1/4W	745-0767-000	
R36	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/8W	745-2323-000	

RF Translator, Schematic Diagram
Figure 5 (Sheet 2)



RF Translator, Schematic Diagram
Figure 5 (Sheet 3)

PARTS LIST (Cont)

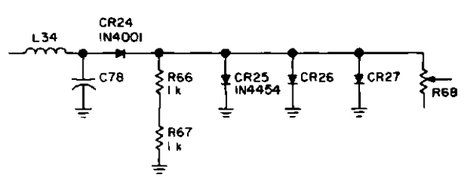
REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
R37	RESISTOR, FXD, CMPSN, 270Ω, 10%, 1/4W	745-0728-000	
R38	RESISTOR, FXD, CMPSN, 27Ω, 10%, 1/4W	745-0692-000	
R39	RESISTOR, FXD, CMPSN, 270Ω, 10%, 1/4W	745-0728-000	
R40	RESISTOR, FXD, CMPSN, 18Ω, 10%, 1/4W	745-0686-000	
R41	RESISTOR, FXD, CMPSN, 270Ω, 10%, 1/4W	745-0728-000	
R42	RESISTOR, FXD, CMPSN, 2.7kΩ, 10%, 1/4W	745-0764-000	
R43	RESISTOR, FXD, CMPSN, 1.5kΩ, 10%, 1/4W	745-0755-000	
R44, R45	RESISTOR, FXD, CMPSN, 18Ω, 10%, 1/8W (A7)	745-2277-000	
R44, R45	RESISTOR, FXD, CMPSN, 22Ω, 5%, 1/8W	745-1863-090	
R46	NOT USED		
R47	RESISTOR, FXD, CMPSN, 82Ω, 10%, 1/8W (A5)	745-2301-000	
R47	RESISTOR, FXD, CMPSN, 68Ω, 10%, 1/8W	745-2298-000	
R48	RESISTOR, FXD, CMPSN, 68Ω, 10%, 1/4W	745-0707-000	
R49	RESISTOR, FXD, CMPSN, 390Ω, 10%, 1/4W	745-0734-000	
R50	RESISTOR, FXD, CMPSN, 27Ω, 10%, 1/4W	745-0692-000	
R51	RESISTOR, FXD, CMPSN, 47Ω, 10%, 1/4W (A5)	745-0701-000	
R51	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R52-R141	NOT USED		
R142	RESISTOR, FXD, CMPSN, 2.2kΩ, 5%, 1/8W (A1)	745-1863-570	
R143	NOT USED		
R144, R145	RESISTOR, FXD, CMPSN, 110Ω, 5%, 1/8W (A5)	745-1863-260	
T1	TRANSFORMER, RF	278-0430-160	
T2	TRANSFORMER, RF	278-0430-190	
T3	TRANSFORMER, RF	278-0431-020	
T4	TRANSFORMER, RF	278-0431-010	
	SECOND MIXER BOARD A3 635-0784-002		
CR1-CR21	NOT USED		
CR22, CR23	SEMICOND DEVICE, 1N5767	922-6119-010	
CR24	SEMICOND DEVICE, 1N4001 (A3)	353-6442-010	
CR25	SEMICOND DEVICE, 1N4454 (A3)	353-3644-010	
CR26, CR27	SEMICOND DEVICE, 1N5767	922-6119-010	
C1-C58	NOT USED		
C59	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C60	CAPACITOR, FXD, MICA DIEL, 36pF, 5%, 50V	912-4141-240	
C61	CAPACITOR, FXD, MICA DIEL, 33pF, 5%, 50V (A4)	912-4141-220	
C61	CAPACITOR, FXD, MICA DIEL, 27pF, 5%, 50V	912-4141-180	
C62	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C63	CAPACITOR, FXD, MICA DIEL, 15pF, ±0.5pF, 300V	912-4141-130	
C64	CAPACITOR, FXD, MICA DIEL, 110pF, 5%, 50V	912-4141-370	
C65	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V (A6)	913-4018-000	
C65	CAPACITOR, FXD, MICA DIEL, 220pF, 5%, 50V	912-4141-450	
C66	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C67	CAPACITOR, FXD, MICA DIEL, 240pF, 5%, 50V	912-4141-460	
C68	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C69	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C70	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C71	CAPACITOR, FXD, MICA DIEL, 62pF, 5%, 50V	912-4141-320	
C72	CAPACITOR, FXD, MICA DIEL, 150pF, 5%, 50V	912-4141-400	
C73	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V (A4)	913-3279-110	
C73	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-180	
C74, C75	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C76	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C77	NOT USED		
C78	CAPACITOR, FXD, MICA DIEL, 24pF, ±0.5pF, 50V	912-4141-160	
C79, C80	NOT USED		
C81	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C82-C122	NOT USED		
C123	CAPACITOR, FXD, MICA DIEL, 27pF, 5%, 50V (A4)	912-4141-180	
C123	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C124	NOT USED		
C125	CAPACITOR, FXD, CER DIEL, 4700pF, 20%, 50V (A4)	913-3279-090	
L1-L25	NOT USED		
L26	COIL, RF, VAR	242-0439-020	
L27	COIL, RF, 2.70μH	240-2028-000	
L28	COIL, RF, 22μH	240-2039-000	

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
L29	COIL, RF, VAR	242-0439-020	
L30	COIL, RF, 2.70μH	240-2028-000	
L31	COIL, RF, 27μH	240-2040-000	
L32, L33	COIL, RF, 0.15μH	240-2013-000	
L34	COIL, RF, 0.39μH (A4)	240-2018-000	
L34	COIL, RF, 0.33μH (A9)	240-2017-000	
L34	COIL, RF, 0.27μH	240-2016-000	
L35	NOT USED		
L36	COIL, RF, 220μH (A4)	240-2723-060	
M1	MIXER, RF	277-0405-010	
Q1-Q11	NOT USED		
Q12	TRANSISTOR, FET, U310	352-1042-010	
Q13	TRANSISTOR, 2N5109	352-0766-010	
Q14	(SEE 637-1767-001)		
RT1, RT2	NOT USED		
RT3	RESISTOR, THRM, 40Ω, 10%, 0.5W	714-1725-000	
R1-R51	NOT USED		
R52	RESISTOR, FXD, CMPSN, 47Ω, 10%, 1/4W	745-0701-000	
R53	RESISTOR, FXD, CMPSN, 68Ω, 10%, 1/4W	745-0707-000	
R54	RESISTOR, FXD, CMPSN, 470Ω, 10%, 1/4W	745-0737-000	
R55	RESISTOR, FXD, CMPSN, 27Ω, 10%, 1/4W	745-0692-000	
R56, R57	RESISTOR, FXD, CMPSN, 2.7kΩ, 10%, 1/4W	745-0764-000	
R58	RESISTOR, FXD, CMPSN, 56Ω, 10%, 1/8W	745-2295-000	
R59	RESISTOR, FXD, CMPSN, 56Ω, 10%, 1/4W	745-0704-000	
R60, R61	RESISTOR, FXD, CMPSN, 2.7kΩ, 10%, 1/4W	745-0764-000	
R62	RESISTOR, FXD, CMPSN, 4.7Ω, 5%, 1/4W	745-4382-000	
R63	RESISTOR, FXD, CMPSN, 15Ω, 10%, 1/4W	745-0683-000	
R64	RESISTOR, FXD, CMPSN, 150Ω, 10%, 1/4W	745-0719-000	
R65	NOT USED		
R66, R67	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W (A3)	745-0749-000	
R68	RESISTOR, VAR, 100Ω, 30%, 1/2W	382-0008-040	
R69	RESISTOR, FXD, CMPSN, 270Ω, 10%, 1/4W	745-0728-000	
R70-R79	NOT USED		
R80	RESISTOR, FXD, CMPSN, 82Ω, 10%, 1/4W (A4)	745-0710-000	
R80	RESISTOR, FXD, CMPSN, 68Ω, 10%, 1/4W	745-0707-000	
R81-R142	NOT USED		
R143	RESISTOR, FXD, CMPSN, 22Ω, 10%, 1/4W (A4)	745-0689-000	
T1-T4	NOT USED		
T5	TRANSFORMER, RF	278-0430-170	
T6	TRANSFORMER, RF	278-0430-150	

MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Added A2R142, 2200 Ω.	635-0782-002, REV E and above
A2	Added C126, test select of 2pF to 6pF.	637-1767-001, REV C and above
A3	Deleted A3CR24, 1N4001; A3CR25, 1N4454; A3R66, 1kΩ; and A3R67, 1kΩ (circuit was as shown below).	635-0784-002, REV C and above



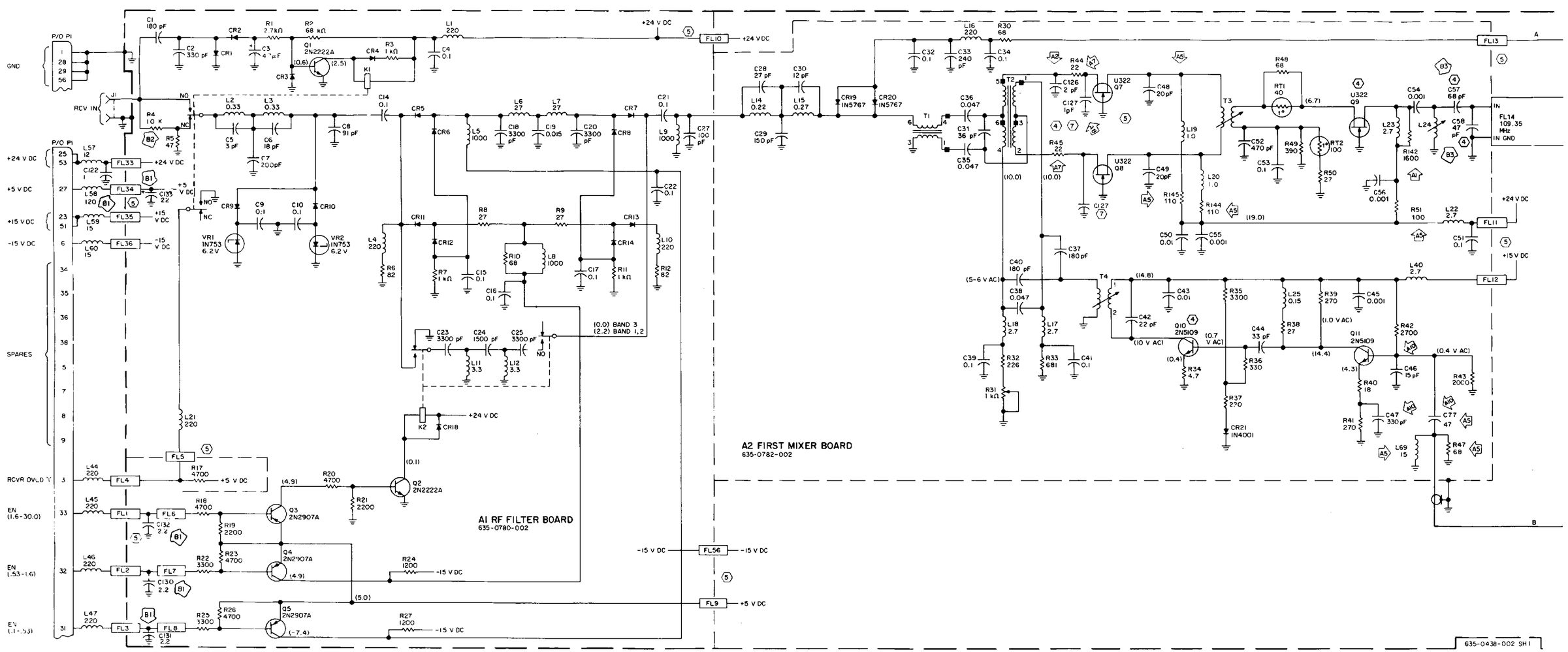
MODIFICATION HISTORY (Cont)

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A4	Deleted A3L36, 220μH (replaced with A3R143). Added A3C125, 4700pF. Added A3R143, 22Ω. Changed: A3C61 from 33pF to 27pF. A3C73 from 0.01μF to 0.1μF. A3L34 from 0.39μH to 0.33μH. A3R80 from 47Ω to 68Ω.	635-0784-002, REV C and above
A5	Added A2L69, 15μH. Added A2R144, 110Ω. Added A2R145, 110Ω. Changed: A2C48 from 18pF to 20pF. A2C49 from 18pF to 20pF. A2C77 from 1000pF to 36pF. A2L19 from 2.7μH to 1.0μH. A2L20 from 2.7μH to 1.0μH. A2R47 from 82Ω to 68Ω. A2R51 from 47Ω to 100Ω.	635-0782-002, REV F and above
A6	Changed A3C65 from 1000pF to 220pF.	635-0784-002, REV D and above
A8	Added C127, test select of 1pF or 2pF.	637-1767-001, REV H and above
A9	Changed A3L34 from 0.33μH to to 0.27 μH.	635-0784-002, REV G and above
A10	Changed: A2C46 from 5pF to 15pF. A2C47 from 51pF to 330pF. A2C77 from 36pF to 47pF.	635-0782-002, REV K and above
B1	Added C130, 2.2μF, electrolytic. Added C131, 2.2μF electrolytic. Added C132, 2.2μF electrolytic. Added C133, 22μF electrolytic. Changed L58 from 4.7μH to 120μH.	637-1767-001 REV K and above.
B2	Changed A1R4 from 2200Ω to 15kΩ.	635-0780-002 REV H and above.
B3	Changed: C57 from 56pF to 68pF. C58 from 56pF to 47pF.	637-1767-001 REV P and above.

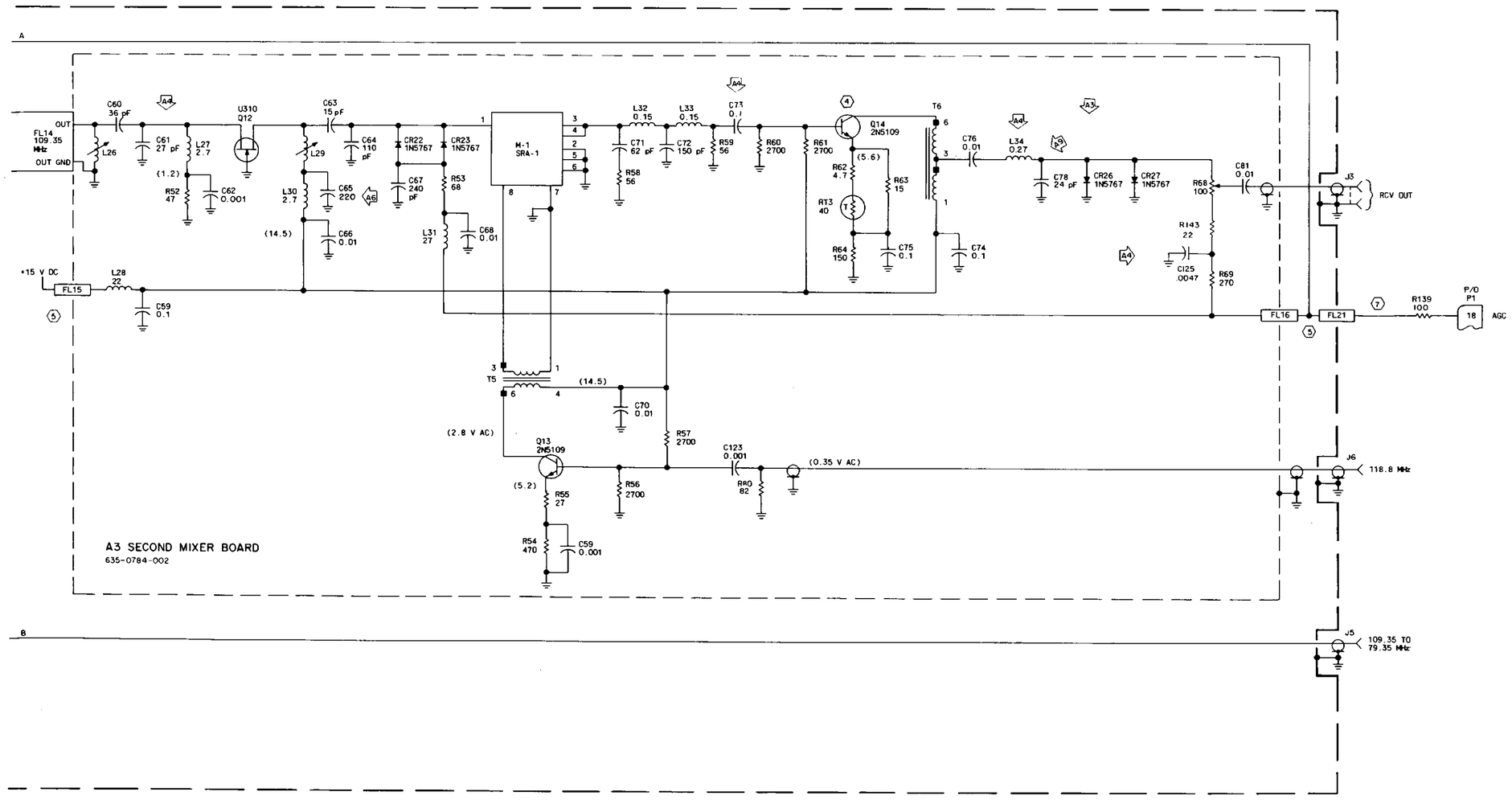
Note

Modification history through REV P has been included in all 637-1767-002 rf translators.

RF Translator, Schematic Diagram
Figure 5 (Sheet 4)



RF Translator, Schematic Diagram
Figure 5 (Sheet 5)



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, AND INDUCTANCE VALUES ARE IN MICROHENRYS.
2. UNLESS OTHERWISE SPECIFIED, DIODES ARE TYPE 1N4454.
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
4. INSTALLED ON NEXT HIGHER ASSEMBLY (637-1767-001).
5. ALL FILTERS ARE 1750 pF, EXCEPT BANDPASS FILTER FL14.
6. U322, A207 AND A208, MATCHED SET.
7. TEST SELECT: R139 FROM 82Ω TO 270Ω. C126 FROM 2pF TO 6pF OR REMOVED (A2) C127 FROM 1pF OR 2pF OR REMOVED (A8)

E35-0438-002 SH 2

RF Translator, Schematic Diagram
Figure 5 (Sheet 6)

RF Translator (1/2-Octave RF Filters) (637-3757-001)

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

523-0769220-001211
1 January 1979

1. DESCRIPTION

RF Translator 637-3757-001, shown in figure 1, is a module enclosed in an rf secure compartment (metal box construction). The rf translator module contains a metal box subassembly with internal shielding between various circuit elements and four 2-layer planar cards. It uses a 56-pin edge-on connector (2 layers, 28 pins each) and four subminiax rf connectors for external connections.

The rf translator module consists of a receive overload circuit, ten 1/2-octave rf filters, and two mixer circuits.

(To Be Supplied)

RF Translator
Figure 1

2. PRINCIPLES OF OPERATION

2.1 General (Refer to figure 2.)

The rf translator converts the 100-kHz (0.100-MHz) to 30.0-MHz receive rf input to a 9.45-MHz receive if frequency.

2.2 Receive Function (Refer to figure 2.)

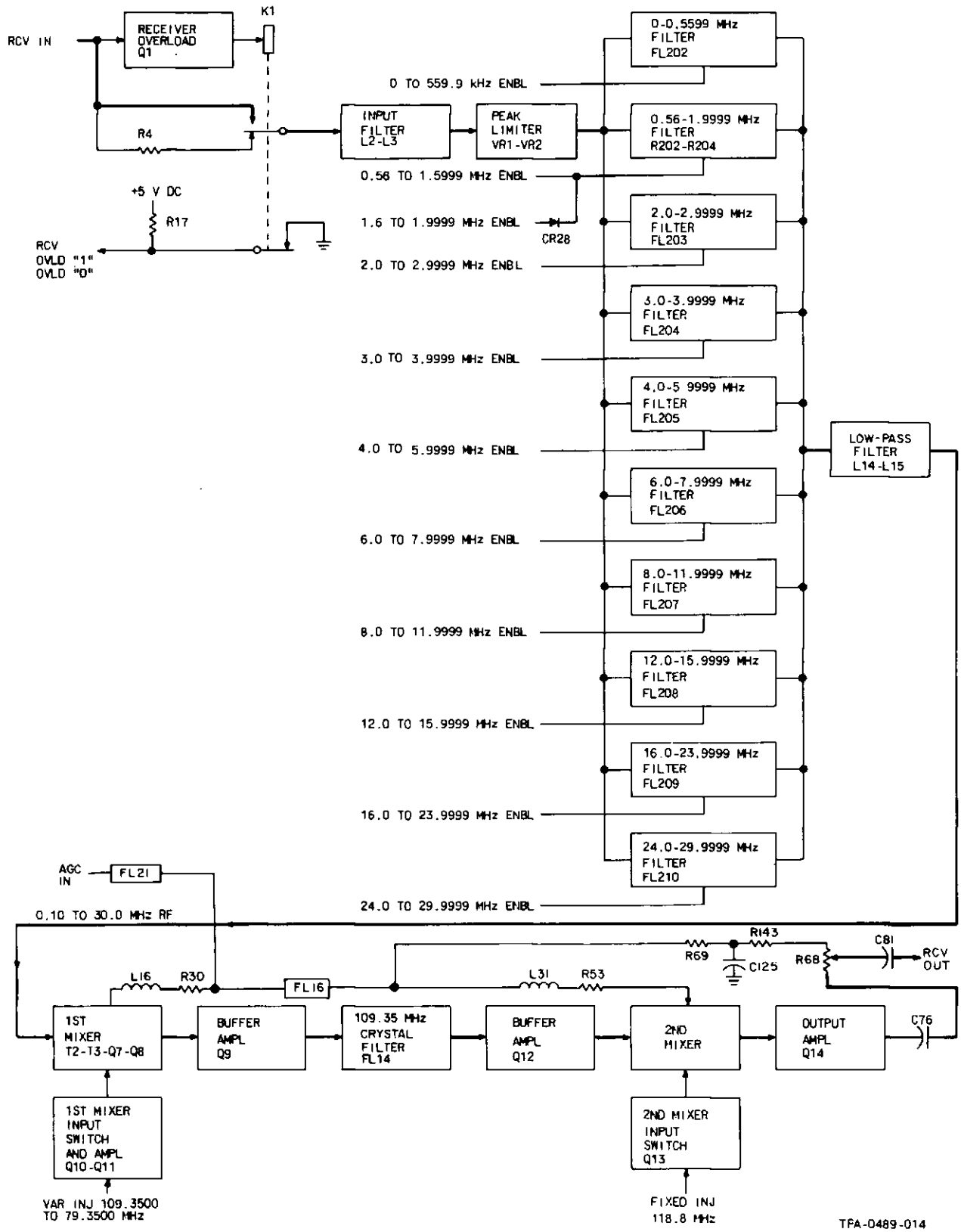
When a receive signal is supplied to the rf translator, it is overload checked and supplied through K1 to the associated 1/2-octave rf filter. If an overload exists, Q1 causes K1 to deenergize, and the receive rf is loaded through R4 and supplied as receive rf through K1 to the associated 1/2-octave rf filter.

The 1/2-octave rf filter is selected by the receiver frequency control. Enable signals from the receiver frequency control enable the applicable filter for the received frequency. Refer to table 1 for received frequency and associated 1/2-octave rf filter.

The signal from K1 is supplied through the selected 1/2-octave rf filter and through low-pass filter L14-L15 to the grounded gate balanced FET first mixer circuit T1-T2, Q7-Q8.

In the first mixer the 0 to 30.0-MHz signal is mixed with a 109.35- to 79.35-MHz variable injection signal to provide a 109.35-MHz if signal. This signal is supplied through FET buffer amplifier Q9, crystal filter FL14, and a second FET buffer amplifier Q12 to the second mixer circuit.

In the second mixer the 109.35-MHz if signal is mixed with a 118.8-MHz fixed injection signal to provide a 9.45-MHz receive if output signal. The receive if output signal is supplied through output amplifier Q14, and output control R68, to the rf translator receive if output.



Block Diagram
Figure 2

Table 1. 1/2-Octave RF Filters Versus Bandwidth.

FREQUENCY	ASSOCIATED FILTER
0 to 559.9 kHz	FL202
560 kHz to 1.9999 MHz	R202 thru R204
2.0 to 2.9999 MHz	FL203
3.0 to 3.9999 MHz	FL204
4.0 to 5.9999 MHz	FL205
6.0 to 7.9999 MHz	FL206
8.0 to 11.9999 MHz	FL207
12.0 to 15.9999 MHz	FL208
16.0 to 23.9999 MHz	FL209
24.0 to 29.9999 MHz	FL210

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the rf translator module are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 2 check total performance of the rf translator module. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

Table 2. RF Translator, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of unit containing the rf translator that is to be tested.		
	b. Remove rf translator. Install rf translator on extender and place it in the unit.		
	c. Set unit LINE SELECTOR switch to 115 V.		
	d. Connect unit to 115 V ac power source and set power on.		
	e. Measure dc voltages between the following pins and ground (P1-1, 28, 29, 56):		
	P1-25 P1-53	+24.0 ±1.0 V dc	Check associated power supply.
	P1-23 P1-51	+15.0 ±1.0 V dc	
	P1-27	+5.0 ±0.2 V dc	
	P1-6	-15.0 ±1.0 V dc	
2. Receiver ssb sensitivity	a. Set front-panel MODE switch to SSB/CW and BANDWIDTH switch to USB.		
	b. Connect an rf signal generator to J1 (RCV ANT jack on rear panel).		
	c. Connect an audio vtvm to A6TP2 (ssb audio).		
(Cont)	d. Set the rf signal generator 101.0 and receiver front panel frequency controls to 100.0 kHz.		

Table 2. RF Translator, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	e. Set the rf signal generator level at 0.00 μV.		
	f. Note noise level on audio vtvm.	Reference.	
	g. Adjust signal generator level to 0.30 μV and note signal level on audio vtvm.	NLT 2 dB above reference.	Check M1, Q14, Q12, FL14, Q9, Q8, Q7, Q5, and associated circuits.
	h. Repeat steps e, f, and g with rf signal generator at each of the following frequencies (receiver front-panel frequency controls set 1000 Hz below each frequency given).		
	250 kHz	NLT 3 dB above reference.	Same as step g.
	500 kHz	NLT 3 dB above reference.	Same as step g.
	1.0 MHz	NLT 3 dB above reference.	Check Q4 and associated circuits.
	1.8 MHz	NLT 10.5 dB above reference.	Check Q2, Q3, K2, and associated circuits.
	2.5 MHz	NLT 10.5 dB above reference.	Same as 1.8 MHz.
	3.5 MHz	NLT 10.5 dB above reference.	
	5.0 MHz	NLT 10.5 dB above reference.	
	7.0 MHz	NLT 10.5 dB above reference.	
	10.0 MHz	NLT 10.5 dB above reference.	
	15.0 MHz	NLT 10.5 dB above reference.	
	20.0 MHz	NLT 10.5 dB above reference.	
	25.0 MHz	NLT 10.5 dB above reference.	
	30.0 MHz	NLT 10.5 dB above reference.	
3. Receiver gain	a. Connect an rf signal generator to J1 (RCV ANT jack on rear panel).		
	b. Connect an rf vtvm (with 50-Ω load) to J3.		
	c. Set the rf signal generator and receiver front-panel frequency controls to 0.500 MHz.		
(Cont)	d. Set the rf signal generator level at -30 dB mW.		

Table 2. RF Translator, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
	e. Note the signal level on the rf vtvm.	NLT -12.0 dB mW.	
	f. Repeat steps d and e at each of the following frequencies:		Same as test 2.
	1.0 MHz	NLT -11.5 dB mW.	
	2.5 MHz	NLT -11.5 dB mW	
	3.5 MHz	NLT -11.5 dB mW	
	5.0 MHz	NLT -11.5 dB mW	
	7.0 MHz	NLT -11.5 kB mW	
	10.0 MHz	NLT -11.5 dB mW	
	15.0 MHz	NLT -10.1 dB mW	
	20.0 MHz	NLT -11.5 dB mW	
	25.0 MHz	NLT -11.5 dB mW	
	29.9 MHz	NLT -11.1 dB mW	
4. Receiver overload protection	a. Connect an rf signal generator to J1 (RCV ANT jack on rear panel).		
	b. Connect a dvm to P1-3. Note voltage.	0 V.	Check Q1, K1, and associated circuits.
	c. Set the rf signal generator and the receiver front-panel frequency controls to 500 kHz.		
	d. Increase the rf signal generator output level until the receive overload relay just clicks.		
	e. Note rf output level of rf signal generator.	1.4 to 1.9 V rms.	Same as step b.
	f. Note dvm reading.	NLT +3.0 V dc.	Check K1 and associated output circuit.
	g. Remove rf signal generator.		
5. Receive agc	a. Remove rf translator from extenders and install it in unit.		
	b. Remove channel A if. Install it on extender card and place it in unit.		
	c. Connect an rf signal generator to J1 (RCV ANT jack on rear panel).		
	d. Connect an rf vtvm (with high impedance probe) to J3 (A8J2).		
	e. Set front-panel AGC switch to OFF.		
	f. Set the rf signal generator and receiver front-panel frequency controls to 15.0000 MHz.		
(Cont)	g. Set the rf signal generator level at -30 dB mW.		

Table 2. RF Translator, Testing and Troubleshooting Procedures (Cont).

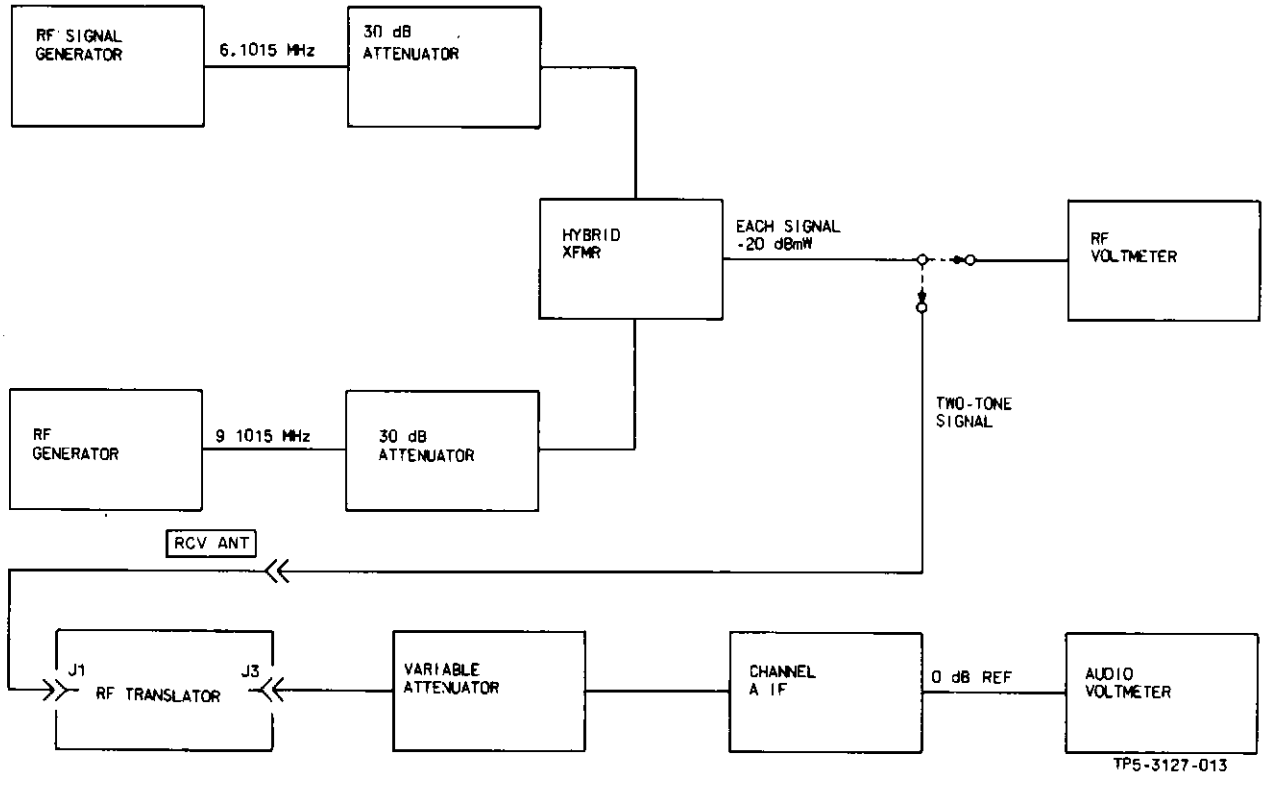
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
	h. Note the signal level on the rf vtvm.	Reference.	
	i. Set front-panel AGC switch to FAST.		
	j. Increase rf signal generator level until reference on rf vtvm is reached.		
	k. Note increase in rf signal generator level.	37 to 43 dB.	Check CR19, CR20, CR22, CR23, CR26, CR27, and associated circuits.
	l. Remove channel A if from extenders and install it in unit.		
	m. Remove rf translator. Install it on extender card and place it in unit.		
6. Filter ripple	a. Connect an rf signal generator to J1 (RCV ANT jack on rear panel).		
	b. Connect an rf vtvm (with 50-Ω load) to J3.		
	c. Set the rf signal generator and receiver front-panel frequency controls to 15.0000 MHz.		
	d. Set the rf signal generator level for -10-dB mW rf vtvm reading.		
	e. Adjust the rf signal generator down to 14.9970 MHz and up to 15.0030 MHz while noting the variation in the rf vtvm reading.	NMT 0.7 dB variation.	Check M1, FL14, and associated circuits.
	f. Adjust the rf signal generator down to 14.9940 MHz and up to 15.0060 MHz while noting the variation in the rf vtvm reading.	NMT 5.0 dB variation.	Same as step e.
7. Receiver intermodulation, 3rd order products	a. Connect two rf signal generators to rf translator as shown in figure 3.		
	b. Set one rf signal generator to 6.1015 MHz.		
	c. Set the second rf signal generator to 9.1015 MHz.		
	d. Using the rf vtvm (with 50-Ω load) connected at the output of the hybrid transformer, independently adjust each rf signal generator for -20 dB mW outputs.		

Table 2. RF Translator, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
7. (Cont)	e. Connect the two-tone signal to J1 (RCV ANT jack on rear panel).		
	f. Set the receiver front-panel frequency controls to 3000.00 kHz.		
	g. Slightly adjust (300 to 2000 Hz) the frequency of the 6.1015-MHz generator for a peak audio output (at A6TP2) as indicated on the audio voltmeter.		
	h. Adjust the variable attenuator for 0-dB reference on the audio voltmeter.	Reference.	
	Note Adjust variable attenuator for a 0-dB reference at point where AGC just begins to effect the audio output.		
	i. Note 6.1015-MHz rf signal generator output.	Reference.	
	j. Set the receiver front-panel frequency controls to 6100.00 kHz.		
	k. Slightly adjust the frequency of the 6.1015-MHz generator for a peak audio output as indicated on the audio voltmeter.		
	l. Adjust the output level of the rf signal generator for 0-dB reference in step h on the audio voltmeter.		
	m. Note the decrease in dB of the rf signal generator output from that referenced in step i.	NLT 83 dB down.	To repair, return to factory.
	n. Repeat steps g through m with the receiver front-panel frequency controls at each of the following settings:		
	12100.00 kHz	NLT 83 dB down.	Same as step m.
	21300.00 kHz	NLT 83 dB down.	
	24300.00 kHz	NLT 83 dB down.	
8. Receiver intermodulation, 2nd order products	a. Connect two rf signal generators to rf translator as shown in figure 3.		
	b. Set one rf signal generator to 6.1015 MHz.		
(Cont)	c. Set the second rf signal generator to 9.1015 MHz.		

Table 2. RF Translator, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
8. (Cont)	d. Using the rf vtvm (with 50-Ω load) connected at the output of the hybrid transformer, independently adjust each rf signal generator for -20-dB mW outputs.		
	e. Connect the two-tone signal to J1 (RCV ANT jack on rear panel).		
	f. Set the receiver front-panel frequency controls to 3000.00 kHz.		
	g. Slightly adjust (300 to 2000 Hz) frequency of the 6.1015-MHz generator for a peak audio output (at A6TP2) as indicated on the audio voltmeter.		
	h. Adjust the variable attenuator for 0-dB reference on the audio voltmeter.	Reference.	
	Note Adjust variable attenuator for a 0-dB reference at point where AGC just begins to effect the audio output.		
	i. Note 6.1015-MHz rf signal generator output.	Reference.	
	j. Set the receiver front-panel frequency controls to 6100.00 kHz.		
	k. Slightly adjust the frequency of the 6.1015-MHz generator for a peak audio output as indicated on the audio voltmeter.		
	l. Adjust the output level on the rf signal generator for 0-dB reference in step h on the audio voltmeter.		
	m. Note the decrease in dB of the rf signal generator output from that referenced in step i.	NLT 70 dB down.	To repair, return to factory.
	n. Repeat steps g through m with the receiver front-panel frequency controls at 15200.00 kHz.	NLT 70 dB down.	Same as step m.



Receive Intermodulation Test Setup
Figure 3

4. ALIGNMENT/ADJUSTMENT

4.1 Receiver Alignment (Adjustment of T3, L24, L26, and L29.)

a. Connect an rf signal generator through a 6-dB load to J1 (RCV ANT jack on rear panel).
b. Connect an rf vtvm (with 50-Ω load) to J3.
c. Set input to J1 at 15.0000 MHz and -30 dB mW.
d. Set front-panel controls for 15 000.0 kHz.
e. Set R68 (receive gain) at full counterclockwise position.
f. Adjust T3, L24, L26, and L29 for maximum output, as indicated by rf vtvm.
g. Perform step f a minimum of three times.

4.2 Mixer Balance (Adjustment of R31.)

a. Use a dvm with 10-μH choke in series with a test probe to measure voltage readings at T2-2 and T2-5 to ground.
b. Adjust R31 for equal voltage reading at T2-2 and T2-5 to ground.

4.3 Injection Level Adjustment (Adjustment of T4.)

a. Connect an rf vtvm (set to 10-V scale) between T2-1 and ground.
b. Vary input frequency from 2.0 to 29.9 MHz and note that voltage varies between 3.0- and 7.0-V rms and that the higher voltage readings occur between 27 and 29.9 MHz.
c. If voltage exceeds the limits of step b or is higher at other than 27 to 29.9 MHz, adjust slug of T4 to achieve the desired levels.

4.4 Translator Gain Adjustment (Adjustment of R68, T1, and T2.)

a. Set the rf signal generator for 15.000 00 MHz at -30 dB mW and the front-panel frequency controls to 15 000.00 kHz.
b. Connect an rf vtvm (with 50-Ω load) to J3.
c. Adjust R68 for -10-dB mW reading on the rf vtvm.
d. Set the rf signal generator for 29.9000 MHz at -30 dB mW and the front-panel frequency controls to 29 900.00 kHz.

e. Using a pointed plastic tool, carefully adjust the leads and windings of T1 and T2 for maximum reading on the rf vtvm.

Note

The objective is to make the output at 29.900 00 MHz as large as possible with an output difference between 29.900 00 and 15.000 00 MHz of not more than 1.0 dB.

f. Repeat steps c, d, and e until no improvement is possible.

4.5 Final Noise Balance (Adjustment of R31.)

a. Set the front-panel frequency controls for 15 000.00 kHz and disconnect the rf signal generator.
b. Connect an audio voltmeter to the channel A if ssb audio output. Reference the background noise level on the audio voltmeter.
c. Adjust R31 (20-turn potentiometer) for a minimum noise level. Make this adjustment very slowly to assure a true minimum.

4.6 T1 and T2 Position Fixing

Note

If T1 and T2 require position fixing it is recommended that the rf translator be returned to the factory. If field repair of T1 and T2 is desired, the following procedures may be used. Do not make these adjustments unless repair has been made to the T1 and/or T2 area of the rf translator.

a. Set the rf signal generator for 29.900 00 MHz at -24 dB mW and the front-panel frequency controls to 29 900.00 kHz.
b. Connect an rf vtvm (with 50-Ω load) to J3. Reference the rf vtvm reading of paragraph 4.4.
c. Using a pipe cleaner, carefully apply a very thin coat of Q-Max to the windings of T1 and T2 and the support rods that hold T1 and T2 in position.
d. After Q-Max is applied, it may be necessary to slightly readjust wires for maximum output. Refer to paragraph 4.4.

5. REPAIR

Repair of the rf translator module is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

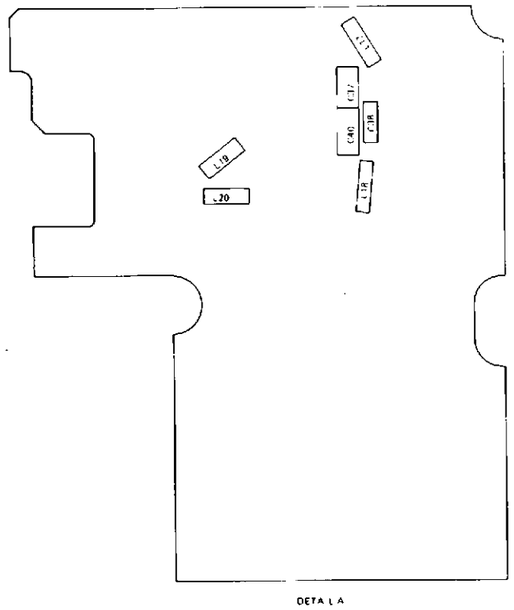
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram, figure 4. The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

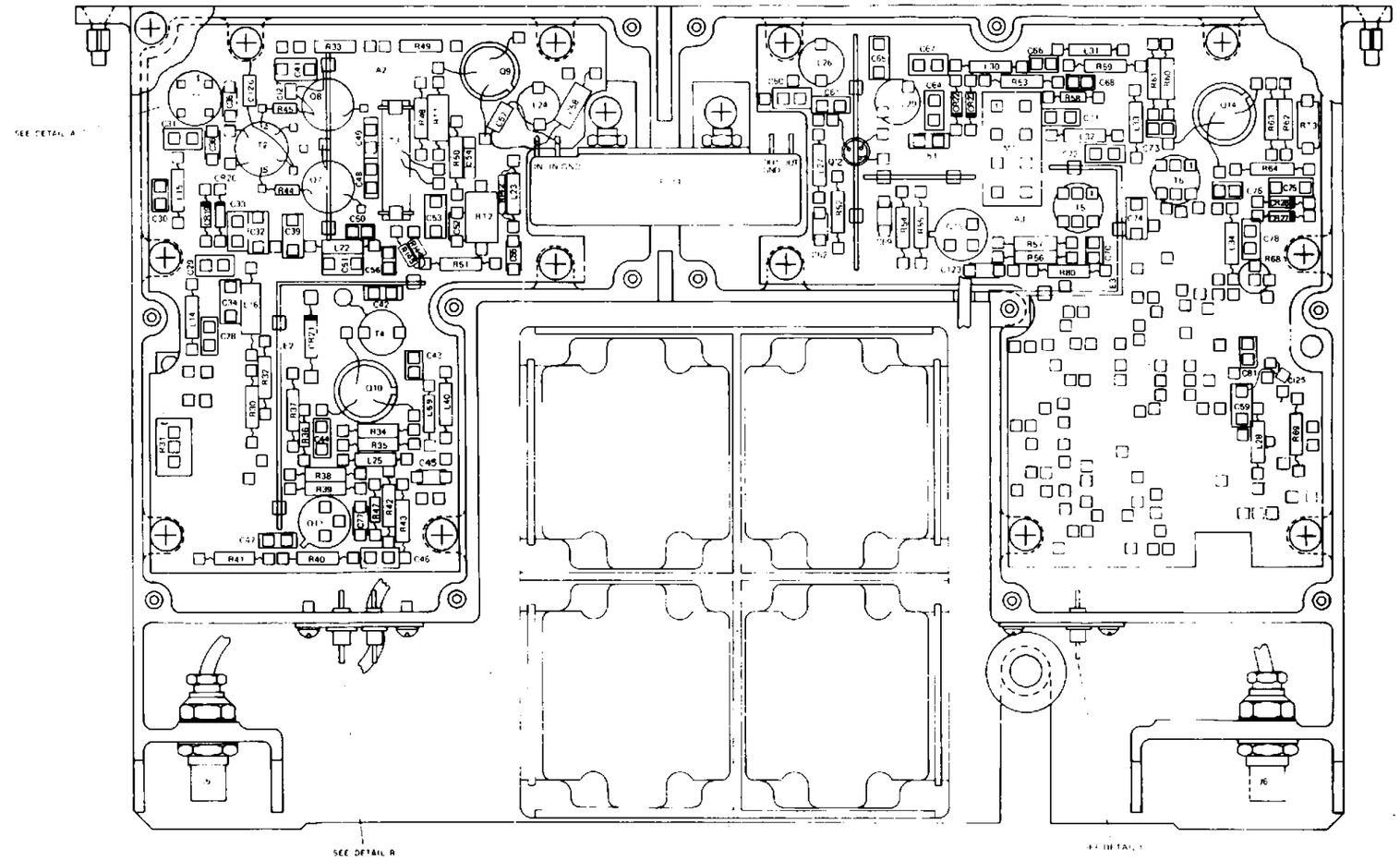
Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

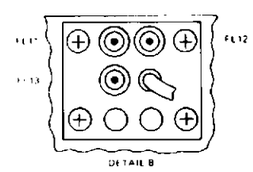
Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points to the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

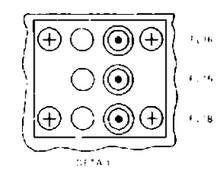
Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Rf translator module	637-3757-001	REV C
Rf filter board A1	638-6099-001	REV B
First mixer board A2	635-0782-003	REV U
Second mixer board A3	635-0784-004	REV N
1/2-Octave filter board A4	606-9880-004	REV —
Diode switching board	778-2934-004	REV H









TPA-1047-028

RF Translator, Schematic Diagram
Figure 4 (Sheet 1 of 6)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
	RF TRANSLATOR	637-3757-001	
A1	RF FILTER BOARD	638-6099-001	
A2	FIRST MIXER BOARD	635-0782-003	
A3	SECOND MIXER BOARD	635-0784-004	
A4	1/2 OCTAVE FILTER BOARD	606-9880-004	
CR1-CR27	NOT USED		
CR28	SEMICOND DEVICE 1N4454	353-3644-010	
C1-C56	NOT USED		
C57	CAPACITOR,FXD MICA DIEL, 68PF, 5%, 50V	912-4141-330	
C58	CAPACITOR,FXD MICA DIEL, 47PF, 5%, 50V	912-4141-280	
C59-C121	NOT USED		
C122	CAPACITOR,FXD ELCTLT, 1UF, 20%, 35V	184-9102-350	
C123-C125	NOT USED		
	CAPACITOR, TEST SELECT		
C126	CAPACITOR,FXD MICA DIEL, 2PF, PORM 0.5PF, 300V	912-4141-540	
C126	CAPACITOR,FXD MICA DIEL, 3PF, PORM 0.5PF, 300V	912-4141-070	
C126	CAPACITOR,FXD MICA DIEL, 4PF, PORM 0.5PF, 300V	912-4141-080	
C126	CAPACITOR,FXD MICA DIEL, 5PF, PORM 0.5PF, 300V	912-4141-010	
C126	CAPACITOR,FXD MICA DIEL, 6PF, PORM 0.5PF, 300V	912-4141-090	
C127, C128	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
FL1,FL2	FILTER,RAD INTR 1750PF	241-5006-010	
FL3	NOT USED		
FL4,FL5	FILTER,RAD INTR 1750PF	241-5006-010	
FL6-FL9	NOT USED		
FL10-FL13	FILTER,RAD INTR 1750PF	241-5006-010	
FL14	FILTER,BP 109.35 MHZ	293-1222-030	
FL15, FL16	FILTER,RAD INTR 1750PF	241-5006-010	
FL17	NOT USED		
FL18	FILTER,RAD INTR 1750PF	241-5006-010	
FL19, FL20	NOT USED		
FL21	FILTER,RAD INTR 1750PF	241-5006-010	
FL22, FL23	NOT USED		
FL24-FL27	FILTER,RAD INTR 1750PF	241-5006-010	
FL28	NOT USED		
FL29-FL46	FILTER,RAD INTR 1750PF	241-5006-010	
J1	CONNECTOR,RCPT ELEC	357-7207-030	
J2	NOT USED		
J3	CONNECTOR,RCPT ELEC	357-7207-030	
J4	NOT USED		
J5,J6	CONNECTOR,RCPT ELEC	357-7207-030	
L1-L43	NOT USED		
L44	COIL,RF 220UH	240-2723-060	
L45-L56	NOT USED		
L57	COIL,RF 12UH	240-1581-000	
L58	COIL,RF 4.70UH	240-2711-210	
L59,L60	COIL,RF 15UH	240-1602-000	
L61	COIL,RF 470UH	240-2715-450	
L62-L70	COIL,RF 100UH	240-2715-370	
Q1-Q8	NOT USED		
Q9	TRANSISTOR, FET U322 (TEST SELECT)	637-9117-002	
Q10	TRANSISTOR 2N5109	352-0766-010	
Q11-Q13	NOT USED		
Q14	TRANSISTOR 2N5109	352-0766-010	
R1-R16	NOT USED		
R17	RESISTOR,FXD CMPSN, 4.7K, 10%, 1/4W	745-0773-000	
R18-R138	NOT USED		
	RESISTOR, TEST SELECT		
R139	RESISTOR,FXD CMPSN, 160 OHMS, 10%, 1/4W	745-0722-000	
R139	RESISTOR,FXD CMPSN, 82 OHMS, 10%, 1/4W	745-0710-000	
R139	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/4W	745-0713-000	
R139	RESISTOR,FXD CMPSN, 150 OHMS, 10%, 1/4W	745-0719-000	
R139	RESISTOR,FXD CMPSN, 270 OHMS, 10%, 1/4W	745-0728-000	
	RF FILTER BOARD A1	638-6099-001	
CR1-CR4	SEMICOND DEVICE 1N4454	353-3644-010	
CR5	SEMICOND DEVICE 1N5711	353-3691-010	
CR6-CR8	NOT USED		
CR9,CR10	SEMICOND DEVICE MPD400	353-3723-030	
C1	CAPACITOR,FXD MICA DIEL, 180PF, 5%, 500V	912-2834-000	
C2	CAPACITOR,FXD MICA DIEL, 330PF, 5%, 500V	912-2852-000	
C3	CAPACITOR,FXD ELCTLT, 4.7UF, 20%, 35V	184-9102-390	
C4	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-200	
C5	CAPACITOR,FXD MICA DIEL, 3PF, PORM 0.5PF, 300V	912-4141-070	
C6	CAPACITOR,FXD MICA DIEL, 18PF, PORM 0.5PF, 100V	912-4141-140	
C7	CAPACITOR,FXD MICA DIEL, 200PF, 5%, 50V	912-4141-440	
C8	CAPACITOR,FXD MICA DIEL, 110PF, 5%, 50V	912-4141-370	
C9,C10	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-200	
C11-C13	NOT USED		
C14	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-200	
C15-C20	NOT USED		
C21	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-200	
K1	RELAY,AMT	974-1065-090	
L1	COIL,RF 220UH	240-2723-060	

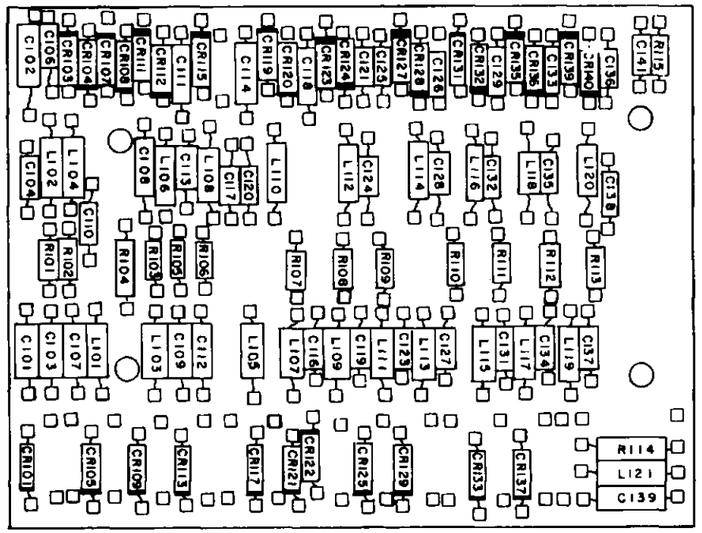
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
L2,L3	COIL,RF 0.33UH	240-2745-010	
L4-L8	NOT USED		
L9	COIL,RF 1000UH	240-2540-000	
L10-L20	NOT USED		
L21	COIL,RF 220UH	240-2723-060	
Q1	TRANSISTOR 2N2222A	352-0661-020	
R1	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/4W	745-0764-000	
R2	RESISTOR,FXD CMPSN, 68K, 10%, 1/4W	745-0815-000	
R3	RESISTOR,FXD CMPSN, 1K, 10%, 1/4W	745-0749-000	
R4	RESISTOR,FXD CMPSN, 2.2K, 10%, 1W	745-3366-000	
R5	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/4W	745-0701-000	
VR1,VR2	SEMICOND DEVICE 1N753A	353-2714-000	
	FIRST MIXER BOARD A2	635-0782-003	
CR1-CR18	NOT USED		
CR19, CR20	SEMICOND DEVICE 1N5767	922-6119-010	
CR21	SEMICOND DEVICE 1N4001	353-6442-010	
C1-C27	NOT USED		
C28	CAPACITOR,FXD MICA DIEL, 27PF, 5%, 50V	912-4141-180	
C29	CAPACITOR,FXD MICA DIEL, 150PF, 5%, 50V	912-4141-400	
C30	CAPACITOR,FXD MICA DIEL, 12PF, PORM 0.5PF, 300V	912-4141-120	
C31	CAPACITOR,FXD MICA DIEL, 36PF, 5%, 50V	912-4141-240	
C32	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-200	
C33	CAPACITOR,FXD MICA DIEL, 240PF, 5%, 50V	912-4141-460	
C34	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-200	
C35,C36	CAPACITOR,FXD CER DIEL, 0.047UF, 10%, 50V	913-5019-280	
C37	CAPACITOR,FXD MICA DIEL, 180PF, 5%, 50V	912-4141-430	
C38	CAPACITOR,FXD CER DIEL, 0.047UF, 10%, 50V	913-5019-280	
C39	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-200	
C40	CAPACITOR,FXD MICA DIEL, 180PF, 5%, 50V	912-4141-430	
C41	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-200	
C42	CAPACITOR,FXD MICA DIEL, 22PF, PORM 0.5PF, 300V	912-4141-030	
C43	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C44	CAPACITOR,FXD MICA DIEL, 33PF, 2%, 50V	912-4141-210	
C45	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C46	CAPACITOR,FXD MICA DIEL, 15PF, PORM 0.5PF, 300V	912-4141-130	
C47	CAPACITOR,FXD MICA DIEL, 330PF, 5%, 50V	912-4141-490	
C48,C49	CAPACITOR,FXD MICA DIEL, 20PF, PORM 0.5PF, 100V	912-4141-150	
C50	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C51	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-200	
C52	CAPACITOR,FXD CER DIEL, 470PF, 10%, 200V	913-4014-000	
C53	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-200	
C54,C55	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C56	CAPACITOR,FXD CER DIEL, 1000PF, 20%, 50V	913-3279-030	
C57-C76	NOT USED		
C77	CAPACITOR,FXD MICA DIEL, 47PF, 5%, 50V	912-4141-280	
L1-L13	NOT USED		
L14	COIL,RF 0.22UH	240-2015-000	
L15	COIL,RF 0.27UH	240-2016-000	
L16	COIL,RF 220UH	240-2723-060	
L17,L18	COIL,RF 2.70UH	240-2028-000	
L19,L20	COIL,RF 1UH	240-2023-000	
L21	NOT USED		
L22,L23	COIL,RF 2.70UH	240-2028-000	
L24	COIL,RF,VAR	242-0439-030	
L25	COIL,RF 0.15UH	240-2013-000	
L26-L39	NOT USED		
L40	COIL,RF 2.70UH	240-2028-000	
L41-L68	NOT USED		
L69	COIL,RF 0.15UH	240-2013-000	
L70-L100	NOT USED		
L101	COIL,RF 27UH	240-2040-000	
Q1-Q6	NOT USED		
Q7,Q8	TRANSISTOR, FET U322 (MATCHED SET)	637-9117-001	
Q9,Q10	NOT USED		
Q11	TRANSISTOR 2N5109	352-0766-010	
RT1	RESISTOR,THRM 40 OHMS, 10%, 0.5W	714-1725-000	
RT2	RESISTOR,THRM 100 OHMS, 10%, 1W	714-1730-000	
R1-R29	NOT USED		
R30	RESISTOR,FXD CMPSN, 68 OHMS, 10%, 1/4W	745-0707-000	
R31	RESISTOR,VAR 1K, 5%, 3/4W	381-1853-170	
R32	RESISTOR,FXD FILM, 226 OHMS, 1%, 1/8W	705-0965-000	
R33	RESISTOR,FXD FILM, 681 OHMS, 1%, 1/8W	705-0988-000	
R34	RESISTOR,FXD CMPSN, 3.3K, 10%, 1/4W	745-0767-000	
R36	RESISTOR,FXD CMPSN, 330 OHMS, 10%, 1/8W	745-2323-000	
R37	RESISTOR,FXD CMPSN, 220 OHMS, 10%, 1/4W	745-0725-000	
R38	RESISTOR,FXD CMPSN, 27 OHMS, 10%, 1/4W	745-0692-000	
R39	RESISTOR,FXD CMPSN, 270 OHMS, 10%, 1/4W	745-0728-000	
R40	RESISTOR,FXD CMPSN, 16 OHMS, 10%, 1/4W	745-0686-000	
R41	RESISTOR,FXD CMPSN, 270 OHMS, 10%, 1/4W	745-0728-000	
R42	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/4W	745-0764-000	
R43	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/4W	745-0761-000	
R44,R45	RESISTOR,FXD CMPSN, 16 OHMS, 5%, 1/8W	745-1863-060	
R46	NOT USED		
R47	RESISTOR,FXD CMPSN, 68 OHMS, 10%, 1/8W	745-2298-000	
R48	RESISTOR,FXD CMPSN, 68 OHMS, 10%, 1/4W	745-0707-000	
R49	RESISTOR,FXD CMPSN, 390 OHMS, 10%, 1/4W	745-0734-000	

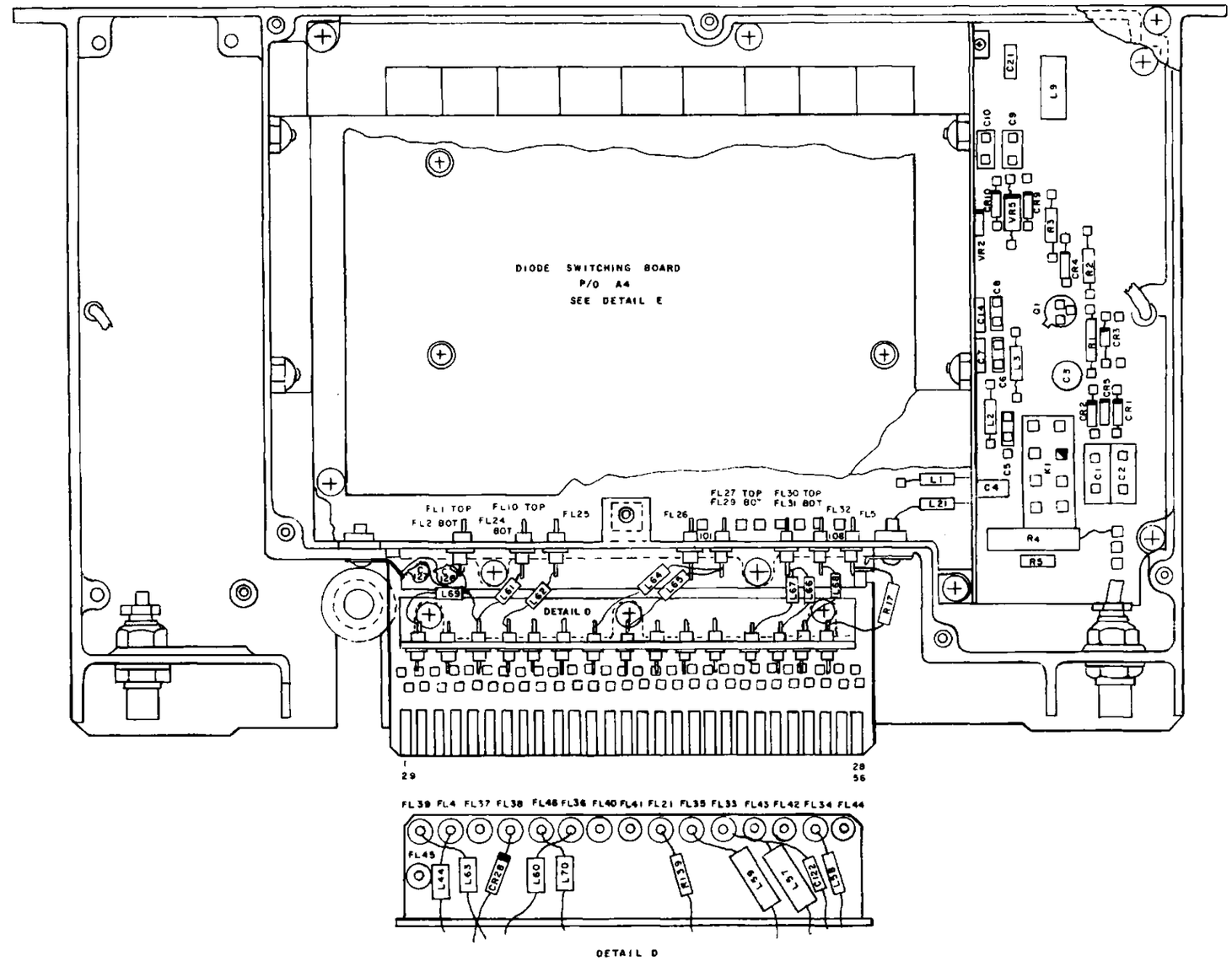
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
R50	RESISTOR,FXD CMPSN, 27 OHMS, 10%, 1/4W	745-0692-000	
R51	RESISTOR,FXD CMPSN, 100 OHMS, 10%, 1/4W	745-0713-000	
R52-R141	NOT USED		
R142	RESISTOR,FXD CMPSN, 1.6K, 5%, 1/8W	745-1863-540	
R143	NOT USED		
R144, R145	RESISTOR,FXD CMPSN, 110 OHMS, 5%, 1/8W	745-1863-260	
T1	TRANSFORMER,RF	278-0430-160	
T2	TRANSFORMER,RF	278-0430-190	
T3	TRANSFORMER,RF	278-0431-020	
T4	TRANSFORMER,RF	278-0431-010	
	SECOND MIXER BOARD A3	635-0784-004	
CR1-CR21	NOT USED		
CR22, CR23	SEMICOND DEVICE 1N5767	922-6119-010	
CR24, CR25	NOT USED		
CR26, CR27	SEMICOND DEVICE 1N5767	922-6119-010	
C1-C58	NOT USED		
C59	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-200	
C60	CAPACITOR,FXD MICA DIEL, 36PF, 5%, 50V	912-4141-240	
C61	CAPACITOR,FXD MICA DIEL, 27PF, 5%, 50V	912-4141-180	
C62	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C63	CAPACITOR,FXD MICA DIEL, 15PF, PORM 0.5PF, 300V	912-4141-130	
C64	CAPACITOR,FXD MICA DIEL, 110PF, 5%, 50V	912-4141-370	
C65	CAPACITOR,FXD MICA DIEL, 220PF, 5%, 50V	912-4141-450	
C66	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C67	CAPACITOR,FXD MICA DIEL, 240PF, 5%, 50V	912-4141-460	
C68	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C69	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C70	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C71	CAPACITOR,FXD MICA DIEL, 62PF, 5%, 50V	912-4141-320	
C72	CAPACITOR,FXD MICA DIEL, 150PF, 5%, 50V	912-4141-400	
C73	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-180	
C74,C75	CAPACITOR,FXD CER DIEL, 0.1UF, 20%, 50V	913-3279-200	
C76	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C77	NOT USED		
C78	CAPACITOR,FXD MICA DIEL, 24PF, PORM 0.5PF, 50V	912-4141-160	
C79,C80	NOT USED		
C81	CAPACITOR,FXD CER DIEL, 0.01UF, 20%, 50V	913-3279-110	
C82-C122	NOT USED		
C123	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C124	NOT USED		
C125	CAPACITOR,FXD CER DIEL, 4700PF, 20%, 50V	913-3279-090	
L1-L25	NOT USED		
L26	COIL,RF,VAR	242-0439-020	
L27	COIL,RF 2.70UH	240-2028-000	
L28	COIL,RF 22UH	240-2039-000	
L29	COIL,RF,VAR	242-0439-020	
L30	COIL,RF 2.70UH	240-2028-000	
L31	COIL,RF 27UH	240-2040-000	
L32,L33	COIL,RF 0.15UH	240-2013-000	
L34	COIL,RF 0.33UH	240-2017-000	
M1	MIXER,RF	277-0405-010	
Q1-Q11	NOT USED		
Q12	TRANSISTOR,FET U310	352-1042-010	
Q13	TRANSISTOR 2N5109	352-0766-010	
RT1,RT2	NOT USED		
RT3	RESISTOR,THRM 40 OHMS, 10%, 0.5W	714-1725-000	
R1-R51	NOT USED		
R52	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/4W	745-0701-000	
R53	RESISTOR,FXD CMPSN, 68 OHMS, 10%, 1/4W	745-0707-000	
R54	RESISTOR,FXD CMPSN, 470 OHMS, 10%, 1/4W	745-0737-000	
R55	RESISTOR,FXD CMPSN, 27 OHMS, 10%, 1/4W	745-0692-000	

RF Translator, Schematic Diagram
Figure 4 (Sheet 2)



DETAIL E



DETAIL D

TPA-1047-028

RF Translator, Schematic Diagram
Figure 4 (Sheet 3)

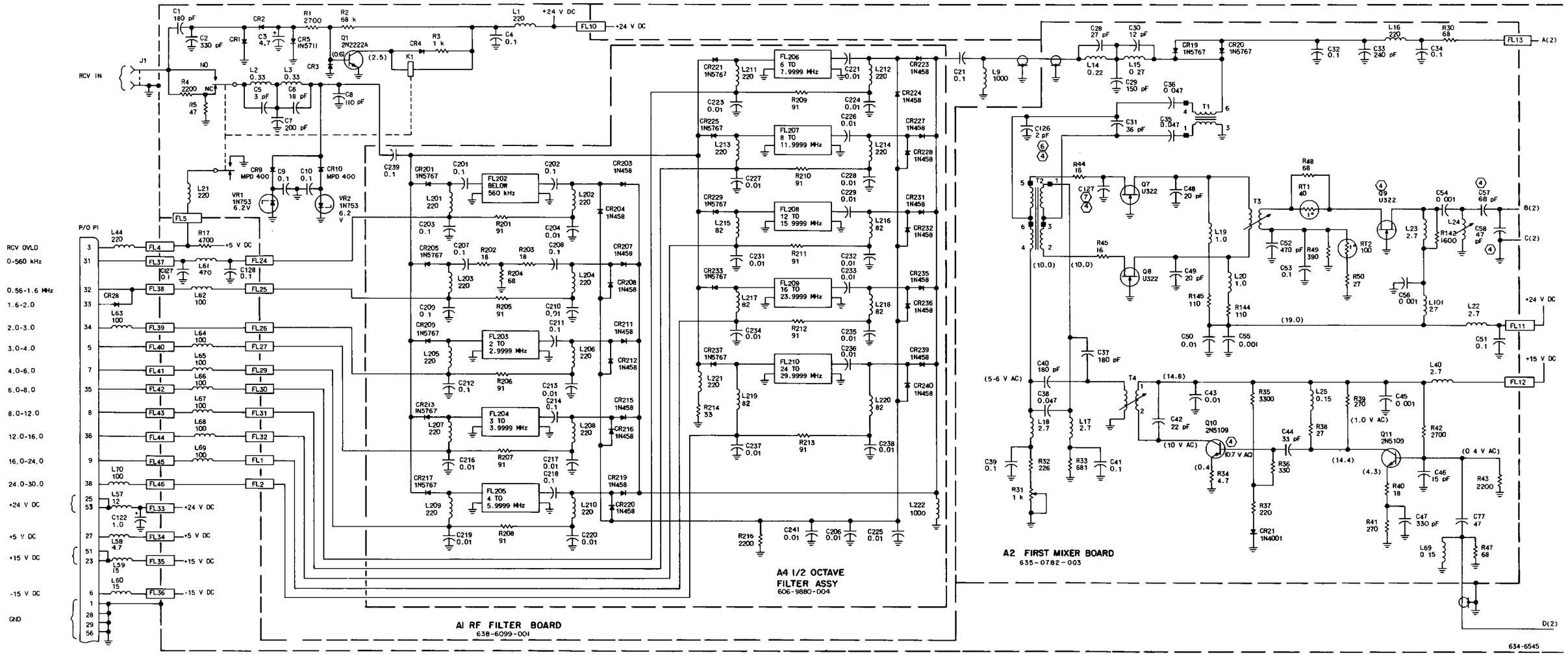
PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
R56,R57	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/4W	745-0764-000	
R58	RESISTOR,FXD CMPSN, 56 OHMS, 10%, 1/8W	745-2295-000	
R54	RESISTOR,FXD CMPSN, 56 OHMS, 10%, 1/4W	745-0704-000	
R60,R61	RESISTOR,FXD CMPSN, 2.7K, 10%, 1/4W	745-0764-000	
R62	RESISTOR,FXD CMPSN, 4.7 OHMS, 5%, 1/4W	745-4382-000	
R63	RESISTOR,FXD CMPSN, 10 OHMS, 10%, 1/4W	745-0677-000	
R64	RESISTOR,FXD CMPSN, 150 OHMS, 10%, 1/4W	745-0719-000	
R65-R67	NOT USED		
R68	RESISTOR,VAR 100 OHMS, 30%, 1/2W	382-0008-040	
R69	RESISTOR,FXD CMPSN, 270 OHMS, 10%, 1/4W	745-0728-000	
R70-R79	NOT USED		
R80	RESISTOR,FXD CMPSN, 68 OHMS, 10%, 1/4W	745-0707-000	
R81-R142	NOT USED		
R143	RESISTOR,FXD CMPSN, 22 OHMS, 10%, 1/4W	745-0689-000	
T1-T4	NOT USED		
T5	TRANSFORMER,RF	278-0430-170	
T6	TRANSFORMER,RF	278-0430-150	
	1/2 OCTAVE FILTER BOARD A4	606-9880-004	
FL1-FL201	NOT USED		
FL202	FILTER,LP	241-0685-010	
FL203	FILTER,BANDPASS	241-0619-010	
FL204	FILTER,BANDPASS	241-0619-020	
FL205	FILTER,BANDPASS	241-0619-030	
FL206	FILTER,BANDPASS	241-0619-040	
FL207	FILTER,BANDPASS	241-0619-050	
FL208	FILTER,BANDPASS	241-0619-060	
FL209	FILTER,BANDPASS	241-0619-070	
FL210	FILTER,BANDPASS	241-0619-080	
	DIODE SWITCHING BOARD (P/O A4)	778-2934-004	
CR1-CR200	NOT USED		
CR201	SEMICOND DEVICE 1N5767	922-6119-010	
CR202	NOT USED		
CR203,CR204	SEMICOND DEVICE 1N458	353-0205-000	
CR205	SEMICOND DEVICE	922-6119-010	
CR206	NOT USED		
CR207,CR208	SEMICOND DEVICE 1N458	353-0205-000	
CR209	SEMICOND DEVICE 1N5767	922-6119-010	
CR210	NOT USED		
CR211,CR212	SEMICOND DEVICE 1N458	353-0205-000	
CR213	SEMICOND DEVICE 1N5767	922-6119-010	
CR214	NOT USED		
CR215	SEMICOND DEVICE 1N458	353-0205-000	
CR216	NOT USED		
CR217	SEMICOND DEVICE 1N5767	922-6119-010	
CR218	NOT USED		
CR219,CR220	SEMICOND DEVICE 1N458	353-0205-000	
CR221	SEMICOND DEVICE 1N5767	922-6119-010	
CR222	NOT USED		
CR223,CR224	SEMICOND DEVICE 1N458	353-0205-000	
CR225	SEMICOND DEVICE 1N5767	922-6119-010	
CR226	NOT USED		
CR227,CR228	SEMICOND DEVICE 1N458	353-0205-000	
CR229	SEMICOND DEVICE 1N5767	922-6119-010	
CR230	NOT USED		
CR231,CR232	SEMICOND DEVICE 1N458	353-0205-000	
CR233	SEMICOND DEVICE 1N5767	922-6119-010	
CR234	NOT USED		
CR235,CR236	SEMICOND DEVICE	353-0205-000	
CR237	SEMICOND DEVICE 1N5767	922-6119-010	
CR238	NOT USED		
CR239,CR240	SEMICOND DEVICE 1N458	353-0205-000	
C1-C200	NOT USED		
C201-C203	CAPACITOR,FXD CER DIEL, 100,000PF, 20%, 50V	913-5661-240	
C204	CAPACITOR,FXD CER DIEL, 10,000PF, 10%, 100V	913-5661-120	
C205	NOT USED		
C206	CAPACITOR,FXD CER DIEL, 10,000PF, 10%, 100V	913-5661-120	
C207-C209	CAPACITOR,FXD CER DIEL, 100,000PF, 20%, 50V	913-5661-240	
C210	CAPACITOR,FXD CER DIEL, 10,000PF, 10%, 100V	913-5661-120	
C211,C212	CAPACITOR,FXD CER DIEL, 100,000PF, 20%, 50V	913-5661-240	
C213	CAPACITOR,FXD CER DIEL, 10,000PF, 10%, 100V	913-5661-120	
C214	CAPACITOR,FXD CER DIEL, 100,000PF, 20%, 50V	913-5661-240	
C215	NOT USED		
C216,C217	CAPACITOR,FXD CER DIEL, 10,000PF, 10%, 100V	913-5661-120	
C218	CAPACITOR,FXD CER DIEL, 100,000PF, 20%, 50V	913-5661-240	
C219-	CAPACITOR,FXD CER DIEL, 10,000PF, 10%, 100V	913-5661-120	

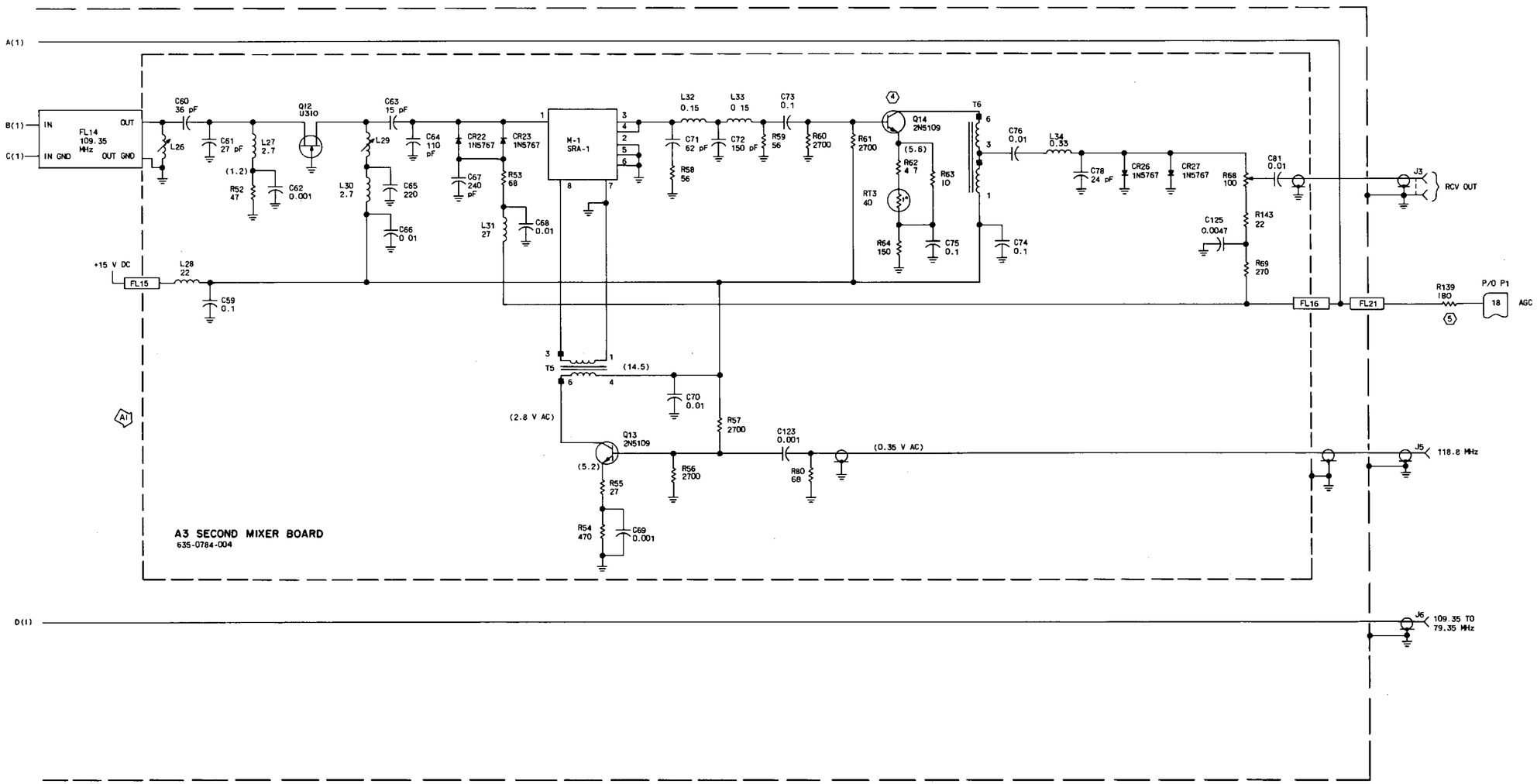
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
C121			
C222	NOT USED		
C223-C229	CAPACITOR,FXD CER DIEL, 10,000PF, 10%, 100V	913-5661-120	
C230	NOT USED		
C231-C238	CAPACITOR,FXD CER DIEL, 10,000PF, 10%, 100V	913-5661-120	
C239	CAPACITOR,FXD CER DIEL, 100,000PF, 20%, 50V	913-5661-240	
C240	NOT USED		
C241	CAPACITOR,FXD CER DIEL, 10,000PF, 10%, 100V	913-5661-120	
L1-L200	NOT USED		
L201-L214	COIL,RF 220UH	240-2524-000	
L215-L220	COIL,RF 82UH	240-2514-000	
L221	COIL,RF 220UH	240-2524-000	
L222	COIL,RF 1000UH	240-2540-000	
R1-R200	NOT USED		
R201	RESISTOR,FXD CMPSN, 91 OHMS, 5%, 1/4W	745-0711-000	
R202,R203	RESISTOR,FXD CMPSN, 18 OHMS, 5%, 1/4W	745-0685-000	
R204	RESISTOR,FXD CMPSN, 68 OHMS, 5%, 1/2W	745-1302-000	
R205-R213	RESISTOR,FXD CMPSN, 91 OHMS, 5%, 1/4W	745-0711-000	
R214	RESISTOR,FXD CMPSN, 33 OHMS, 10%, 1/2W	745-1289-000	
R215	NOT USED		
R216	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/4W	745-0761-000	

RF Translator, Schematic Diagram
Figure 4 (Sheet 4)



RF Translator, Schematic Diagram
Figure 4 (Sheet 5)



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, AND INDUCTANCE VALUES ARE IN MICROHENRYS.
2. UNLESS OTHERWISE SPECIFIED, DIODES ARE TYPE 1N4454
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
4. INSTALLED ON NEXT HIGHER ASSEMBLY (637-3757-001).
5. TEST SELECT (82,100,150,180,270 OHM)
6. TEST SELECT (2,3,4,5,6 pF)
7. TEST SELECT (1,2 pF)

634-6545

RF Translator, Schematic Diagram
Figure 4 (Sheet 6)

Control (638-6065-001)

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

523-0769221-001211
1 January 1979

1. DESCRIPTION

Control 638-6065-001, shown in figure 1, is a 2-layer planar card with a 130-pin edge-on connector (2 layers, 65 pins each).

The control card consists of vbfo/operating frequency variable clock generator, parallel storage registers for the operating frequency signal, bcd parallel frequency band and 1/2-octave control circuits, tune start control circuit, and monitor control circuits.

(To Be Supplied)

Control
Figure 1

2. PRINCIPLES OF OPERATION

2.1 General

The control card:

a. Receives operating frequency rate control information and generates/stores the data for the operating frequency selected.

b. Receives vbfo rate control information and supplies a variable clock signal for the vbfo circuit card.

c. Uses the parallel bcd signals to produce frequency band control outputs.

d. Uses a fault summary circuit to summarize a power supply fault, a synthesizer fault, and a vbfo synthesizer fault to produce a receiver fault indication.

e. Uses an rf overload summary circuit to summarize a preselector rf overload and a receiver rf overload and produce a receive rf overload indication.

f. Receives a preselector fault signal and supplies a buffered/current driven preselector fault indication.

g. Receives a local frequency change signal, a remote frequency change signal, or a change in local enable signal and produces a tune start pulse output.

2.2 Rate Control to Variable Clock Circuit (Refer to figure 2.)

The rate control to variable clock circuit consists of a PROM (programmable read-only memory), a clock generator, a preset divide-by-N counter, and a coarse tune and a fine tune multiplexer/demultiplexer.

The clock generator (U1A, U1B, and U6-Q3 output) provides a tuning clock of 13 250 Hz. Binary counter/divider U6 provides outputs which are binary multiples of the clock generator output. The selected change rate is determined by the bcd rate input, PROM U25, and the coarse tune and fine tune multiplexer/demultiplexers (U24, U7). Note that PROM U25 has 8 address inputs. Address inputs 0 through 4 are rate code inputs. Address inputs 5 through 7 are control functions. Table 1 shows the input address for the control functions. Tables 2 through 9 show the input address for the rate code inputs and the associated output division ratios-from the multiplexer/demultiplexer circuit.

2.3 Vbfo Clock Output

The vbfo clock output is supplied when a vbfo tune input is applied (logic 1) and rate control inputs are applied. AND gate U11D is enabled and the variable clock is supplied through U11D and U11C to the vbfo clock out at P1-85.

Note the $\overline{\text{clock inhibit}}$ (logic 1) must be applied to enable gate U11C.

2.4 Bcd Frequency Control Outputs (Refer to figure 2.)

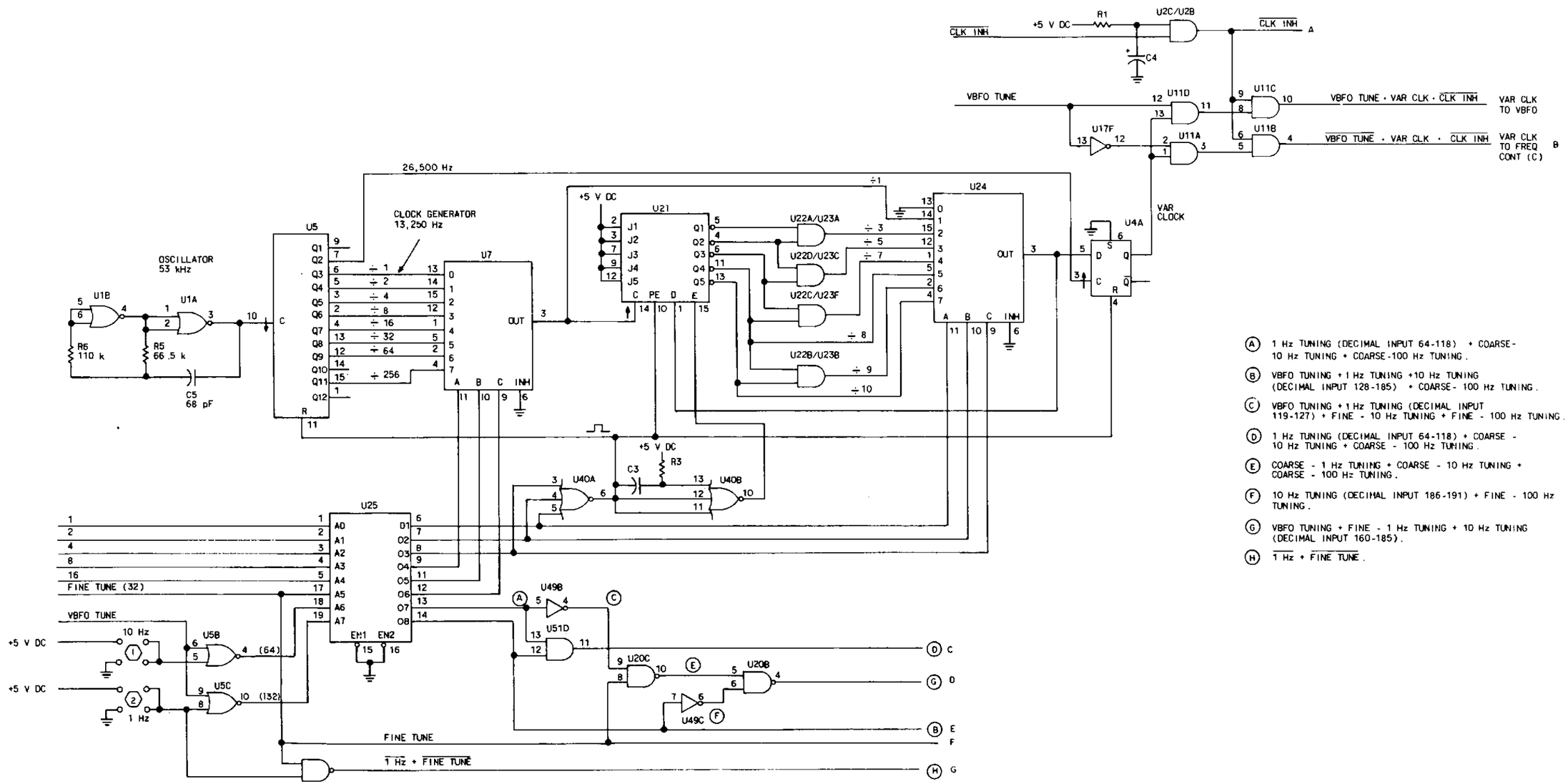
The frequency control circuits are rate-of-change frequency control input signals to parallel bcd frequency control output signals. Bcd output signals for 1 Hz to 30 MHz in 1-Hz steps are provided when used with the correct rate inputs and strapping. Current driven outputs for 1 kHz to 30 MHz are also supplied to be used with an associated preselector. Band control output circuits or 1/2-octave control outputs are also provided when used with the appropriate strapping and associated rf translator.

2.4.1 Band Control Output Circuits (Refer to figure 3.)

When strapped for standard filter control (SF), the band control output circuits receive parallel bcd input control signals (from storage registers U29-U36) and converts them to one-of-three band control output signals. Frequency ranges of the bands are as follows: band 1 - 0 to 539 kHz, band 2 - 540 kHz to 1.59 MHz, and band 3 - 1.60 to 29.99 MHz. Refer to figure 3 and note that any bcd frequency input that is between the low frequency of one band and the low frequency of the next higher band provides the associated band output control signal (logic 0 = enabled).

Table 1. PROM U25, Address Inputs for Control Functions.

CONTROL FUNCTION	LOGIC INPUTS		
	5	6	7
Vbfo -- coarse tuning	0	0	0
Vbfo -- fine tuning	1	0	0
Frequency -- coarse 1-Hz tuning	0	1	0
Frequency -- fine 1-Hz tuning	1	1	0
Frequency -- coarse 10-Hz tuning	0	0	1
Frequency -- fine 10-Hz tuning	1	0	1
Frequency -- coarse 100-Hz tuning	0	1	1
Frequency -- fine 100-Hz tuning	1	1	1



(A) 1 Hz TUNING (DECIMAL INPUT 64-118) + COARSE - 10 Hz TUNING + COARSE -100 Hz TUNING.

(B) VBFO TUNING + 1 Hz TUNING +10 Hz TUNING (DECIMAL INPUT 128-185) + COARSE - 100 Hz TUNING.

(C) VBFO TUNING + 1 Hz TUNING (DECIMAL INPUT 119-127) + FINE - 10 Hz TUNING + FINE - 100 Hz TUNING.

(D) 1 Hz TUNING (DECIMAL INPUT 64-118) + COARSE - 10 Hz TUNING + COARSE - 100 Hz TUNING.

(E) COARSE - 1 Hz TUNING + COARSE - 10 Hz TUNING + COARSE - 100 Hz TUNING.

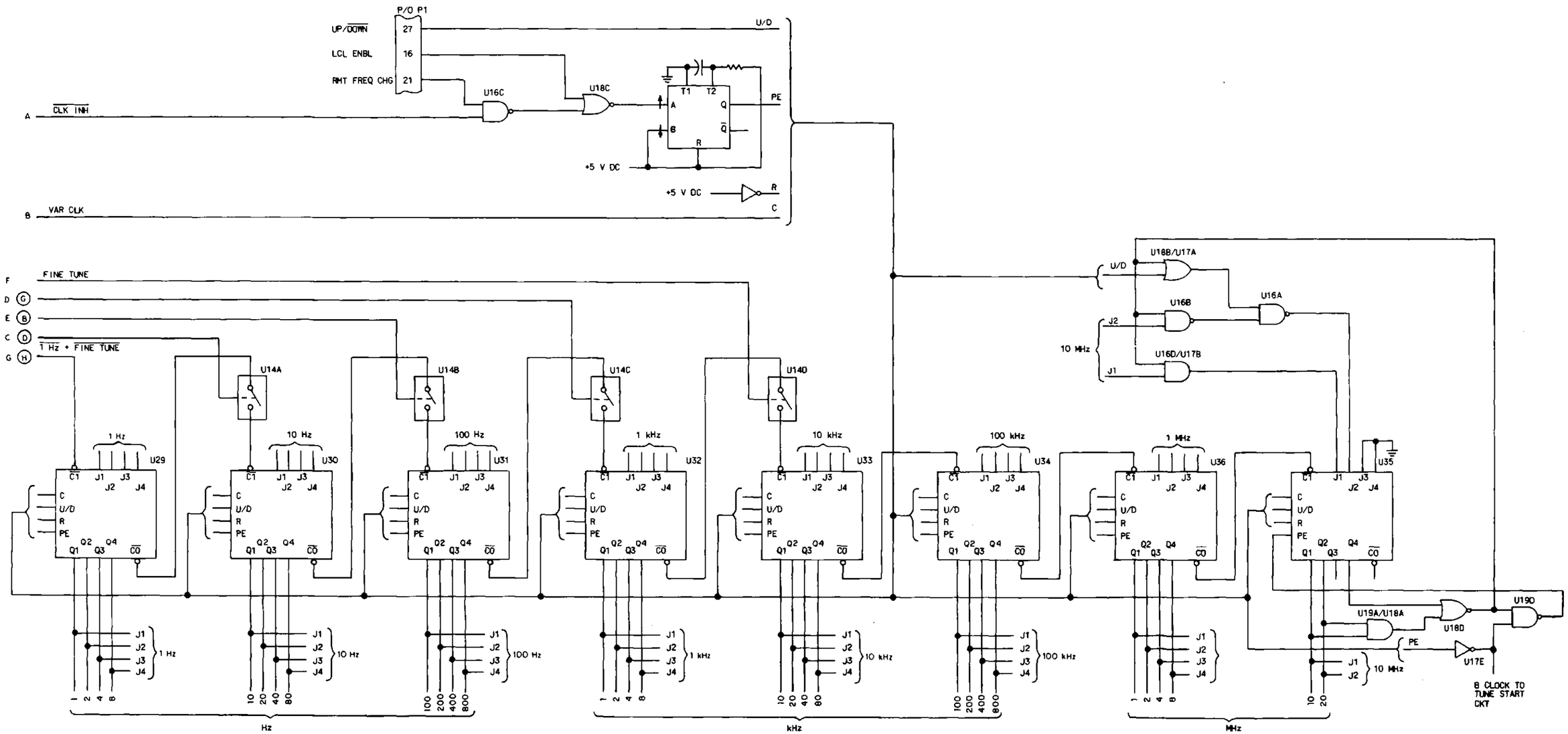
(F) 10 Hz TUNING (DECIMAL INPUT 186-191) + FINE - 100 Hz TUNING.

(G) VBFO TUNING + FINE - 1 Hz TUNING + 10 Hz TUNING (DECIMAL INPUT 160-185).

(H) $\overline{1\ Hz}$ + $\overline{FINE\ TUNE}$.

TPA-1257-024

Rate Control to Variable Clock and Frequency Control Circuit
Figure 2 (Sheet 1 of 2)



TPA-1257-024

Rate Control to Variable Clock and Frequency Control Circuit
Figure 2 (Sheet 2)

Table 2. PROM U25, VBFO — Coarse Tuning.

DECIMAL INPUT	PROM U25																U7				U24				DIVISION RATIO	APPROX VARIABLE CLOCK FREQ (Hz)
	RATE					FINE TUNE	VBFO		OUTPUTS								IN			OUT CH	IN			OUT CH		
	1	2	4	8	16		10 Hz	1 Hz																		
	0	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8	A	B	C		A	B	C			
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1	7	0	0	0	0	NONE	0
1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1	1	1	7	1	1	1	7	2560	5
2	0	1	0	0	0	0	0	0	1	1	1	0	1	1	0	1	0	1	1	6	1	1	1	7	640	21
3	1	1	0	0	0	0	0	0	1	1	1	1	0	1	0	1	1	0	1	5	1	1	1	7	320	41
4	0	0	1	0	0	0	0	0	0	0	1	1	0	1	0	1	1	0	1	5	0	0	1	4	224	59
5	1	0	1	0	0	0	0	0	1	1	1	0	0	1	0	1	0	0	1	4	1	1	1	7	160	83
6	0	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	0	1	4	1	0	1	5	128	104
7	1	1	1	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	1	4	0	0	1	4	112	118
8	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1	1	0	1	5	0	1	0	2	96	138
9	1	0	0	1	0	0	0	0	1	1	1	1	1	0	0	1	1	1	0	3	1	1	1	7	80	166
10	0	1	0	1	0	0	0	0	0	1	1	1	1	0	0	1	1	1	0	3	0	1	1	6	72	184
11	1	1	0	1	0	0	0	0	1	0	1	1	1	0	0	1	1	1	0	3	1	0	1	5	64	207
12	0	0	1	1	0	0	0	0	0	0	1	1	1	0	0	1	1	1	0	3	0	0	1	4	56	237
13	1	0	1	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	1	4	0	1	0	2	48	276
14	0	1	1	1	0	0	0	0	1	1	1	0	1	0	0	1	0	1	0	2	1	1	1	7	40	331
15	1	1	1	1	0	0	0	0	0	1	1	0	1	0	0	1	0	1	0	2	0	1	1	6	36	368
16	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	1	0	1	0	2	1	0	1	5	32	414
17	1	0	0	0	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	2	0	0	1	4	28	473
18	0	1	0	0	1	0	0	0	0	1	0	1	1	0	0	1	1	1	0	3	0	1	0	2	24	552
19	1	1	0	0	1	0	0	0	0	1	0	1	1	0	0	1	1	1	0	3	0	1	0	2	24	552
20	0	0	1	0	1	0	0	0	1	1	1	1	0	0	0	1	1	0	0	1	1	1	1	7	20	663
21	1	0	1	0	1	0	0	0	0	1	1	1	0	0	0	1	1	0	0	1	0	1	1	6	18	736
22	0	1	1	0	1	0	0	0	1	0	1	1	0	0	0	1	1	0	0	1	1	0	1	5	16	828
23	1	1	1	0	1	0	0	0	0	0	1	1	0	0	0	1	1	0	0	1	0	0	1	4	14	946
24	0	0	0	1	1	0	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
25	1	0	0	1	1	0	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
26	0	1	0	1	1	0	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
27	1	1	0	1	1	0	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
28	0	0	1	1	1	0	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
29	1	0	1	1	1	0	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
30	0	1	1	1	1	0	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
31	1	1	1	1	1	0	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104

Table 3. PROM U25, VBFO — Fine Tuning.

DECIMAL INPUT	PROM U25																U7				U24				DIVISION RATIO	APPROX VARIABLE CLOCK FREQ (Hz)
	RATE					FINE TUNE	VBFO		OUTPUTS								IN			OUT CH	IN			OUT CH		
	1	2	4	8	16		10 Hz	1 Hz																		
	0	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8	A	B	C		A	B	C			
32	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	1	1	1	1	7	0	0	0	0	NONE	0
33	1	0	0	0	0	1	0	0	1	1	1	1	1	1	0	1	1	1	1	7	1	1	1	7	2560	5
34	0	1	0	0	0	1	0	0	1	1	1	0	1	1	0	1	0	1	1	6	1	1	1	7	640	21
35	1	1	0	0	0	1	0	0	1	1	1	1	0	1	0	1	1	0	1	5	1	1	1	7	320	41
36	0	0	1	0	0	1	0	0	0	0	1	1	0	1	0	1	1	0	1	5	0	0	1	4	224	59
37	1	0	1	0	0	1	0	0	1	1	1	0	0	1	0	1	0	0	1	4	1	1	1	7	160	83
38	0	1	1	0	0	1	0	0	1	0	1	0	0	1	0	1	0	0	1	4	1	0	1	5	128	104
39	1	1	1	0	0	1	0	0	0	0	1	0	0	1	0	1	0	0	1	4	0	0	1	4	112	118
40	0	0	0	1	0	1	0	0	0	1	0	1	0	1	0	1	1	0	1	5	0	1	0	2	96	138
41	1	0	0	1	0	1	0	0	1	1	1	1	1	0	0	1	1	1	0	3	1	1	1	7	80	166
42	0	1	0	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	0	3	0	1	1	6	72	184
43	1	1	0	1	0	1	0	0	1	0	1	1	1	0	0	1	1	1	0	3	1	0	1	5	64	207
44	0	0	1	1	0	1	0	0	0	0	1	1	1	0	0	1	1	1	0	3	0	0	1	4	56	237
45	1	0	1	1	0	1	0	0	0	1	0	0	0	1	0	1	0	0	1	4	0	1	0	2	48	276
46	0	1	1	1	0	1	0	0	1	1	1	0	1	0	0	1	0	1	0	2	1	1	1	7	40	331
47	1	1	1	1	0	1	0	0	0	1	1	0	1	0	0	1	0	1	0	2	0	1	1	6	36	368
48	0	0	0	0	1	1	0	0	1	0	1	0	1	0	0	1	0	1	0	2	1	0	1	5	32	414
49	1	0	0	0	1	1	0	0	0	0	1	0	1	0	0	1	0	1	0	2	0	0	1	4	28	473
50	0	1	0	0	1	1	0	0	0	1	0	1	1	0	0	1	1	1	0	3	0	1	0	2	24	552
51	1	1	0	0	1	1	0	0	0	1	0	1	1	0	0	1	1	1	0	3	0	1	0	2	24	552
52	0	0	1	0	1	1	0	0	1	1	1	1	0	0	0	1	1	0	0	1	1	1	1	7	20	663
53	1	0	1	0	1	1	0	0	0	1	1	1	0	0	0	1	1	0	0	1	0	1	1	6	18	736
54	0	1	1	0	1	1	0	0	1	0	1	1	0	0	0	1	1	0	0	1	1	0	1	5	16	828
55	1	1	1	0	1	1	0	0	0	0	1	1	0	0	0	1	1	0	0	1	0	0	1	4	14	946
56	0	0	0	1	1	1	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
57	1	0	0	1	1	1	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
58	0	1	0	1	1	1	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
59	1	1	0	1	1	1	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
60	0	0	1	1	1	1	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
61	1	0	1	1	1	1	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
62	0	1	1	1	1	1	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
63	1	1	1	1	1	1	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104

Table 4. PROM U25, Frequency — Coarse 1-Hz Tuning.

DECIMAL INPUT	PROM U25																U7				U24				DIVISION RATIO	APPROX VARIABLE CLOCK FREQ (Hz)
	RATE					FINE TUNE	VBFO		OUTPUTS								IN			OUT CH	IN			OUT CH		
	1	2	4	8	16		10 Hz	1 Hz																		
	0	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8	A	B	C		A	B	C			
64	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	7	0	0	0	0	NONE	0
65	1	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	7	1	1	1	7	2560	5
66	0	1	0	0	0	0	1	0	1	1	1	0	1	1	1	1	0	1	1	6	1	1	1	7	640	21
67	1	1	0	0	0	0	1	0	1	1	1	1	0	1	1	1	1	0	1	5	1	1	1	7	320	41
68	0	0	1	0	0	0	1	0	0	0	1	1	0	1	1	1	1	0	1	5	0	0	1	4	224	59
69	1	0	1	0	0	0	1	0	1	1	1	0	0	1	1	1	0	0	1	4	1	1	1	7	160	83
70	0	1	1	0	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	4	1	0	1	5	128	104
71	1	1	1	0	0	0	1	0	0	0	1	0	0	1	1	1	0	0	1	4	0	0	1	4	112	118
72	0	0	0	1	0	0	1	0	0	1	0	1	0	1	1	1	1	0	1	5	0	1	0	2	96	138
73	1	0	0	1	0	0	1	0	1	1	1	1	1	0	1	1	1	1	0	3	1	1	1	7	80	166
74	0	1	0	1	0	0	1	0	0	1	1	1	1	0	1	1	1	1	0	3	0	1	1	6	72	184
75	1	1	0	1	0	0	1	0	1	0	1	1	1	0	1	1	1	1	0	3	1	0	1	5	64	207
76	0	0	1	1	0	0	1	0	0	0	1	1	1	0	1	1	1	1	0	3	0	0	1	4	56	237
77	1	0	1	1	0	0	1	0	0	1	0	0	0	1	1	1	0	0	1	4	0	1	0	2	48	276
78	0	1	1	1	0	0	1	0	1	1	1	0	1	0	1	1	0	1	0	2	1	1	1	7	40	331
79	1	1	1	1	0	0	1	0	0	1	1	0	1	0	1	1	0	1	0	2	0	1	1	6	36	368
80	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	1	0	1	0	2	1	0	1	5	32	414
81	1	0	0	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	2	0	0	1	4	28	473
82	0	1	0	0	1	0	1	0	0	1	0	1	1	0	1	1	1	1	0	3	0	1	0	2	24	552
83	1	1	0	0	1	0	1	0	0	1	0	1	1	0	1	1	1	1	0	3	0	1	0	2	24	552
84	0	0	1	0	1	0	1	0	1	1	1	1	0	0	1	1	1	0	0	1	1	1	1	7	20	663
85	1	0	1	0	1	0	1	0	0	1	1	1	0	0	1	1	1	0	0	1	0	1	1	6	18	736
86	0	1	1	0	1	0	1	0	1	0	1	1	0	0	1	1	1	0	0	1	1	0	1	5	16	828
87	1	1	1	0	1	0	1	0	0	0	1	1	0	0	1	1	1	0	0	1	0	0	1	4	14	946
88	0	0	0	1	1	0	1	0	0	1	0	0	1	0	1	1	0	1	0	2	0	1	0	2	12	1104
89	1	0	0	1	1	0	1	0	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0	3	10	1325
90	0	1	0	1	1	0	1	0	1	0	0	1	1	0	1	1	1	1	0	3	1	0	0	1	8	1656
91	1	1	0	1	1	0	1	0	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
92	0	0	1	1	1	0	1	0	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
93	1	0	1	1	1	0	1	0	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
94	0	1	1	1	1	0	1	0	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
95	1	1	1	1	1	0	1	0	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208

Table 5. PROM U25, Frequency — Fine 1-Hz Tuning.

DECIMAL INPUT	PROM U25																U7				U24				DIVISION RATIO	APPROX VARIABLE CLOCK FREQ (Hz)
	RATE					FINE TUNE	VBFO		OUTPUTS								IN			OUT CH	IN			OUT CH		
	1	2	4	8	16		10 Hz	1 Hz																		
	0	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8	A	B	C		A	B	C			
96	0	0	0	0	0	1	1	0	0	0	0	1	1	1	1	1	1	1	1	7	0	0	0	0	NONE	0
97	1	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	7	1	1	1	7	2560	5
98	0	1	0	0	0	1	1	0	1	1	1	0	1	1	1	1	0	1	1	6	1	1	1	7	640	21
99	1	1	0	0	0	1	1	0	1	1	1	1	0	1	1	1	1	0	1	5	1	1	1	7	320	41
100	0	0	1	0	0	1	1	0	0	0	1	1	0	1	1	1	1	0	1	5	0	0	1	4	224	59
101	1	0	1	0	0	1	1	0	1	1	1	0	0	1	1	1	0	0	1	4	1	1	1	7	160	83
102	0	1	1	0	0	1	1	0	1	0	1	0	0	1	1	1	0	0	1	4	1	0	1	5	128	104
103	1	1	1	0	0	1	1	0	0	0	1	0	0	1	1	1	0	0	1	4	0	0	1	4	112	118
104	0	0	0	1	0	1	1	0	0	1	0	1	0	1	1	1	1	0	1	5	0	1	0	2	96	138
105	1	0	0	1	0	1	1	0	1	1	1	1	1	0	1	1	1	1	0	3	1	1	1	7	80	166
106	0	1	0	1	0	1	1	0	0	1	1	1	1	0	1	1	1	1	0	3	0	1	1	6	72	184
107	1	1	0	1	0	1	1	0	1	0	1	1	1	0	1	1	1	1	0	3	1	0	1	5	64	207
108	0	0	1	1	0	1	1	0	0	0	1	1	1	0	1	1	1	1	0	3	0	0	1	4	56	237
109	1	0	1	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0	1	4	0	1	0	2	48	276
110	0	1	1	1	0	1	1	0	1	1	1	0	1	0	1	1	0	1	0	2	1	1	1	7	40	331
111	1	1	1	1	0	1	1	0	0	1	1	0	1	0	1	1	0	1	0	2	0	1	1	6	36	368
112	0	0	0	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	0	2	1	0	1	5	32	414
113	1	0	0	0	1	1	1	0	0	0	1	0	1	0	1	1	0	1	0	2	0	0	1	4	28	473
114	0	1	0	0	1	1	1	0	0	1	0	1	1	0	1	1	1	1	0	3	0	1	0	2	24	552
115	1	1	0	0	1	1	1	0	1	1	1	1	0	0	1	1	1	0	0	1	1	1	1	7	20	663
116	0	0	1	0	1	1	1	0	1	0	1	1	0	0	1	1	1	0	0	1	1	0	1	5	16	828
117	1	0	1	0	1	1	1	0	0	0	1	1	0	0	1	1	1	0	0	1	0	0	1	4	14	946
118	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0	3	10	1325
119	1	1	1	0	1	1	1	0	1	1	1	1	1	0	0	1	1	1	0	3	1	1	1	7	80	166
120	0	0	0	1	1	1	1	0	1	0	1	1	1	0	0	1	1	1	0	3	1	0	1	5	64	207
121	1	0	0	1	1	1	1	0	0	1	0	0	0	1	0	1	0	0	1	4	0	1	0	2	48	276
122	0	1	0	1	1	1	1	0	0	1	1	0	1	0	0	1	0	1	0	2	0	1	1	6	36	368
123	1	1	0	1	1	1	1	0	0	1	0	1	1	0	0	1	1	1	0	3	0	1	0	2	24	552
124	0	0	1	1	1	1	1	0	0	1	1	1	0	0	0	1	1	0	0	1	0	1	1	6	18	736
125	1	0	1	1	1	1	1	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
126	0	1	1	1	1	1	1	0	1	0	0	1	1	0	0	1	1	1	0	3	1	0	0	1	8	1656
127	1	1	1	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	1	0	1	0	2	6	2208

Table 6. PROM U25, Frequency — Coarse 10-Hz Tuning.

DECIMAL INPUT	PROM U25																U7				U24				DIVISION RATIO	APPROX VARIABLE CLOCK FREQ (Hz)
	RATE					FINE TUNE	VBFO		OUTPUTS								IN			OUT CH	IN			OUT CH		
	1	2	4	8	16		10 Hz	1 Hz																		
	0	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8	A	B	C		A	B	C			
128	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	7	0	0	0	0	NONE	0
129	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	7	1	1	1	7	2560	5
130	0	1	0	0	0	0	0	1	1	1	1	0	1	1	1	1	0	1	1	6	1	1	1	7	640	21
131	1	1	0	0	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	5	1	1	1	7	320	41
132	0	0	1	0	0	0	0	1	0	0	1	1	0	1	1	1	1	0	1	5	0	0	1	4	224	59
133	1	0	1	0	0	0	0	1	1	1	1	0	0	1	1	1	0	0	1	4	1	1	1	7	160	83
134	0	1	1	0	0	0	0	1	1	0	1	0	0	1	1	1	0	0	1	4	1	0	1	5	128	104
135	1	1	1	0	0	0	0	1	0	0	1	0	0	1	1	1	0	0	1	4	0	0	1	4	112	118
136	0	0	0	1	0	0	0	1	0	1	0	1	0	1	1	1	1	0	1	5	0	1	0	2	96	138
137	1	0	0	1	0	0	0	1	1	1	1	1	1	0	1	1	1	1	0	3	1	1	1	7	80	166
138	0	1	0	1	0	0	0	1	0	1	1	1	1	0	1	1	1	1	0	3	0	1	1	6	72	184
139	1	1	0	1	0	0	0	1	1	0	1	1	1	0	1	1	1	1	0	3	1	0	1	5	64	207
140	0	0	1	1	0	0	0	1	0	0	1	1	1	0	1	1	1	1	0	3	0	0	1	4	56	237
141	1	0	1	1	0	0	0	1	0	1	0	0	0	1	1	1	0	0	1	4	0	1	0	2	48	276
142	0	1	1	1	0	0	0	1	1	1	1	0	1	0	1	1	0	1	0	2	1	1	1	7	40	331
143	1	1	1	1	0	0	0	1	0	1	1	0	1	0	1	1	0	1	0	2	0	1	1	6	36	368
144	0	0	0	0	1	0	0	1	1	0	1	0	1	0	1	1	0	1	0	2	1	0	1	5	32	414
145	1	0	0	0	1	0	0	1	0	0	1	0	1	0	1	1	0	1	0	2	0	0	1	4	28	473
146	0	1	0	0	1	0	0	1	0	1	0	1	1	0	1	1	1	1	0	3	0	1	0	2	24	552
147	1	1	0	0	1	0	0	1	0	1	0	1	1	0	1	1	1	1	0	3	0	1	0	2	24	552
148	0	0	1	0	1	0	0	1	1	1	1	1	0	0	1	1	1	0	0	1	1	1	1	7	20	663
149	1	0	1	0	1	0	0	1	0	1	1	1	0	0	1	1	1	0	0	1	0	1	1	6	18	736
150	0	1	1	0	1	0	0	1	1	0	1	1	0	0	1	1	1	0	0	1	1	0	1	5	16	828
151	1	1	1	0	1	0	0	1	0	0	1	1	0	0	1	1	1	0	0	1	0	0	1	4	14	946
152	0	0	0	1	1	0	0	1	0	1	0	0	1	0	1	1	0	1	0	2	0	1	0	2	12	1104
153	1	0	0	1	1	0	0	1	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0	3	10	1325
154	0	1	0	1	1	0	0	1	1	0	0	1	1	0	1	1	1	1	0	3	1	0	0	1	8	1656
155	1	1	0	1	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
156	0	0	1	1	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
157	1	0	1	1	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
158	0	1	1	1	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
159	1	1	1	1	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208

Table 7. PROM U25, Frequency — Fine 10-Hz Tuning.

DECIMAL INPUT	PROM U25																U7				U24				DIVISION RATIO	APPROX VARIABLE CLOCK FREQ (Hz)
	RATE					FINE TUNE	VBFO		OUTPUTS								IN			OUT CH	IN			OUT CH		
	1	2	4	8	16		10 Hz	1 Hz																		
	0	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8	A	B	C		A	B	C			
160	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	1	1	1	1	7	0	0	0	0	NONE	0
161	1	0	0	0	0	1	0	1	1	1	1	1	1	1	0	1	1	1	1	7	1	1	1	7	2560	5
162	0	1	0	0	0	1	0	1	1	1	1	0	1	1	0	1	0	1	1	6	1	1	1	7	640	21
163	1	1	0	0	0	1	0	1	1	1	1	1	0	1	0	1	1	0	1	5	1	1	1	7	320	41
164	0	0	1	0	0	1	0	1	0	0	1	1	0	1	0	1	1	0	1	5	0	0	1	4	224	59
165	1	0	1	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	1	4	1	1	1	7	160	83
166	0	1	1	0	0	1	0	1	1	0	1	0	0	1	0	1	0	0	1	4	1	0	1	5	128	104
167	1	1	1	0	0	1	0	1	0	0	1	0	0	1	0	1	0	0	1	4	0	0	1	4	112	118
168	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	1	5	0	1	0	2	96	138
169	1	0	0	1	0	1	0	1	1	1	1	1	1	0	0	1	1	1	0	3	1	1	1	7	80	166
170	0	1	0	1	0	1	0	1	0	1	1	1	1	0	0	1	1	1	0	3	0	1	1	6	72	184
171	1	1	0	1	0	1	0	1	1	0	1	1	1	0	0	1	1	1	0	3	1	0	1	5	64	207
172	0	0	1	1	0	1	0	1	0	0	1	1	1	0	0	1	1	1	0	3	0	0	1	4	56	237
173	1	0	1	1	0	1	0	1	0	1	0	0	0	1	0	1	0	0	1	4	0	1	0	2	48	276
174	0	1	1	1	0	1	0	1	1	1	1	0	1	0	0	1	0	1	0	2	1	1	1	7	40	331
175	1	1	1	1	0	1	0	1	0	1	1	0	1	0	0	1	0	1	0	2	0	1	1	6	36	368
176	0	0	0	0	1	1	0	1	1	0	1	0	1	0	0	1	0	1	0	2	1	0	1	5	32	414
177	1	0	0	0	1	1	0	1	0	0	1	0	1	0	0	1	0	1	0	2	0	0	1	4	28	473
178	0	1	0	0	1	1	0	1	0	1	0	1	1	0	0	1	1	1	0	3	0	1	0	2	24	552
179	1	1	0	0	1	1	0	1	0	1	0	1	1	0	0	1	1	1	0	3	0	1	0	2	24	552
180	0	0	1	0	1	1	0	1	1	1	1	1	0	0	0	1	1	0	0	1	1	1	1	7	20	663
181	1	0	1	0	1	1	0	1	0	1	1	1	0	0	0	1	1	0	0	1	0	1	1	6	18	736
182	0	1	1	0	1	1	0	1	1	0	1	1	0	0	0	1	1	0	0	1	1	0	1	5	16	828
183	1	1	1	0	1	1	0	1	0	0	1	1	0	0	0	1	1	0	0	1	0	0	1	4	14	946
184	0	0	0	1	1	1	0	1	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
185	1	0	0	1	1	1	0	1	1	1	0	1	0	0	0	1	1	0	0	1	1	1	0	3	10	1325
186	0	1	0	1	1	1	0	1	1	1	1	1	1	0	0	0	1	1	0	3	1	1	1	7	80	166
187	1	1	0	1	1	1	0	1	1	0	1	1	1	0	0	0	1	1	0	3	1	0	1	5	64	207
188	0	0	1	1	1	1	0	1	0	1	0	0	0	1	0	0	0	0	1	4	0	1	0	2	48	276
189	1	0	1	1	1	1	0	1	1	1	1	0	1	0	0	0	0	1	0	2	1	1	1	7	40	331
190	0	1	1	1	1	1	0	1	0	1	1	0	1	0	0	0	0	1	0	2	0	1	1	6	36	368
191	1	1	1	1	1	1	0	1	1	0	1	0	1	0	0	0	0	1	0	2	1	0	1	5	32	414

Table 8. PROM U25, Frequency — Coarse 100-Hz Tuning.

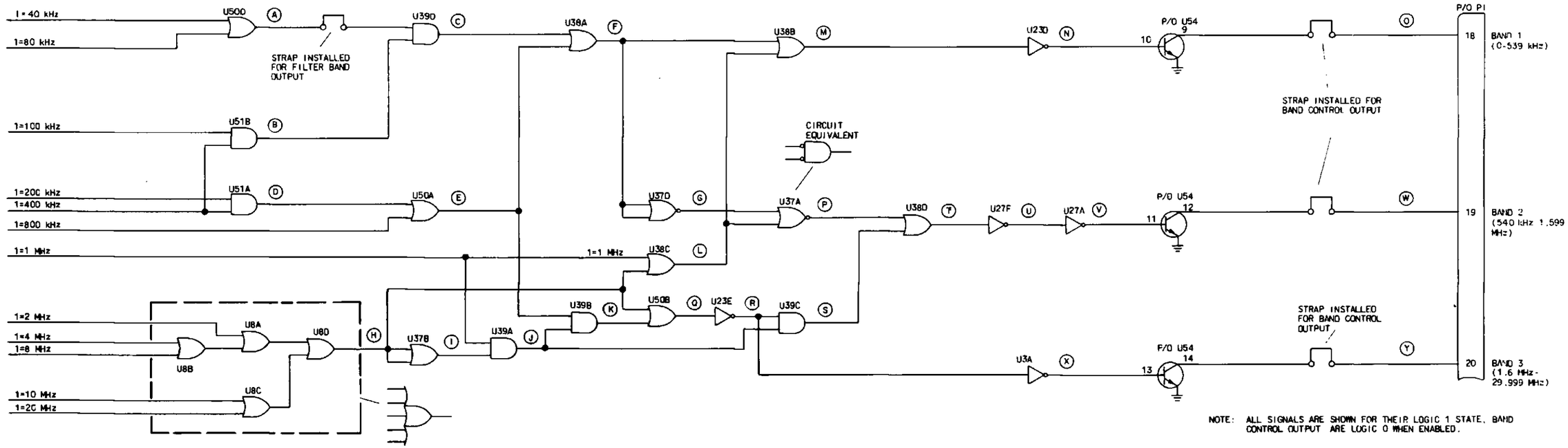
DECIMAL INPUT	PROM U25																U7				U24				DIVISION RATIO	APPROX VARIABLE CLOCK FREQ (Hz)
	RATE					FINE TUNE	VBFO		OUTPUTS								IN			OUT CH	IN			OUT CH		
	1	2	4	8	16		10 Hz	1 Hz																		
	0	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8	A	B	C		A	B	C			
192	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1	1	1	1	7	0	0	0	0	NONE	0
193	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	7	1	1	1	7	2560	5
194	0	1	0	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	6	1	1	1	7	640	21
195	1	1	0	0	0	0	1	1	1	1	1	1	0	1	1	1	1	0	1	5	1	1	1	7	320	41
196	0	0	1	0	0	0	1	1	0	0	1	1	0	1	1	1	1	0	1	5	0	0	1	4	224	59
197	1	0	1	0	0	0	1	1	1	1	1	0	0	1	1	1	0	0	1	4	1	1	1	7	160	83
198	0	1	1	0	0	0	1	1	1	0	1	0	0	1	1	1	0	0	1	4	1	0	1	5	128	104
199	1	1	1	0	0	0	1	1	0	0	1	0	0	1	1	1	0	0	1	4	0	0	1	4	112	118
200	0	0	0	1	0	0	1	1	0	1	0	1	0	1	1	1	1	0	1	5	0	1	0	2	96	138
201	1	0	0	1	0	0	1	1	1	1	1	1	1	0	1	1	1	1	0	3	1	1	1	7	80	166
202	0	1	0	1	0	0	1	1	0	1	1	1	1	0	1	1	1	1	0	3	0	1	1	6	72	184
203	1	1	0	1	0	0	1	1	1	0	1	1	1	0	1	1	1	1	0	3	1	0	1	5	64	207
204	0	0	1	1	0	0	1	1	0	0	1	1	1	0	1	1	1	1	0	3	0	0	1	4	56	237
205	1	0	1	1	0	0	1	1	0	1	0	0	0	1	1	1	0	0	1	4	0	1	0	2	48	276
206	0	1	1	1	0	0	1	1	1	1	1	0	1	0	1	1	0	1	0	2	1	1	1	7	40	331
207	1	1	1	1	0	0	1	1	0	1	1	0	1	0	1	1	0	1	0	2	0	1	1	6	36	368
208	0	0	0	0	1	0	1	1	1	0	1	0	1	0	1	1	0	1	0	2	1	0	1	5	32	414
209	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	1	0	1	0	2	0	0	1	4	28	473
210	0	1	0	0	1	0	1	1	0	1	0	1	1	0	1	1	1	1	0	3	0	1	0	2	24	552
211	1	1	0	0	1	0	1	1	0	1	0	1	1	0	1	1	1	1	0	3	0	1	0	2	24	552
212	0	0	1	0	1	0	1	1	1	1	1	1	0	0	1	1	1	0	0	1	1	1	1	7	20	663
213	1	0	1	0	1	0	1	1	0	1	1	1	0	0	1	1	1	0	0	1	0	1	1	6	18	736
214	0	1	1	0	1	0	1	1	1	0	1	1	0	0	1	1	1	0	0	1	1	0	1	5	16	828
215	1	1	1	0	1	0	1	1	0	0	1	1	0	0	1	1	1	0	0	1	0	0	1	4	14	946
216	0	0	0	1	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0	2	0	1	0	2	12	1104
217	1	0	0	1	1	0	1	1	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0	3	10	1325
218	0	1	0	1	1	0	1	1	1	0	0	1	1	0	1	1	1	1	0	3	1	0	0	1	8	1656
219	1	1	0	1	1	0	1	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
220	0	0	1	1	1	0	1	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
221	1	0	1	1	1	0	1	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
222	0	1	1	1	1	0	1	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
223	1	1	1	1	1	0	1	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208

Table 9. PROM U25, Frequency — Fine 100-Hz Tuning.

DECIMAL INPUT	PROM U25																U7				U24				DIVISION RATIO	APPROX VARIABLE CLOCK FREQ (Hz)
	RATE					FINE TUNE	VBFO		OUTPUTS								IN			OUT CH	IN			OUT CH		
	1	2	4	8	16		10 Hz	1 Hz																		
	0	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8	A	B	C		A	B	C			
224	0	0	0	0	0	1	1	1	0	0	0	1	1	1	0	0	1	1	1	7	0	0	0	0	NONE	0
225	1	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	1	1	1	7	1	1	1	7	2560	5
226	0	1	0	0	0	1	1	1	1	1	1	0	1	1	0	0	0	1	1	6	1	1	1	7	640	21
227	1	1	0	0	0	1	1	1	1	1	1	1	0	1	0	0	1	0	1	5	1	1	1	7	320	41
228	0	0	1	0	0	1	1	1	0	0	1	1	0	1	0	0	1	0	1	5	0	0	1	4	224	59
229	1	0	1	0	0	1	1	1	1	1	1	0	0	1	0	0	0	0	1	4	1	1	1	7	160	83
230	0	1	1	0	0	1	1	1	1	0	1	0	0	1	0	0	0	0	1	4	1	0	1	5	128	104
231	1	1	1	0	0	1	1	1	0	0	1	0	0	1	0	0	0	0	1	4	0	0	1	4	112	118
232	0	0	0	1	0	1	1	1	0	1	0	1	0	1	0	0	1	0	1	5	0	1	0	2	96	138
233	1	0	0	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	0	3	1	1	1	7	80	166
234	0	1	0	1	0	1	1	1	0	1	1	1	1	0	0	0	1	1	0	3	0	1	1	6	72	184
235	1	1	0	1	0	1	1	1	1	0	1	1	1	0	0	0	1	1	0	3	1	0	1	5	64	207
236	0	0	1	1	0	1	1	1	0	0	1	1	1	0	0	0	1	1	0	3	0	0	1	4	56	237
237	1	0	1	1	0	1	1	1	0	1	0	0	0	1	0	0	0	0	1	4	0	1	0	2	48	276
238	0	1	1	1	0	1	1	1	0	1	0	0	0	1	0	0	0	0	1	4	0	1	0	2	48	276
239	1	1	1	1	0	1	1	1	1	1	1	0	1	0	0	0	0	1	0	2	1	1	1	7	40	331
240	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0	0	0	1	0	2	1	1	1	7	40	331
241	1	0	0	0	1	1	1	1	0	1	1	0	1	0	0	0	0	1	0	2	0	1	1	6	36	368
242	0	1	0	0	1	1	1	1	0	1	1	0	1	0	0	0	0	1	0	2	0	1	1	6	36	368
243	1	1	0	0	1	1	1	1	1	0	1	0	1	0	0	0	0	1	0	2	1	0	1	5	32	414
244	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	0	1	0	2	0	0	1	4	28	473
245	1	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	0	1	0	2	0	0	1	4	28	473
246	0	1	1	0	1	1	1	1	0	1	0	1	1	0	0	0	1	1	0	3	0	1	0	2	24	552
247	1	1	1	0	1	1	1	1	0	1	0	1	1	0	0	0	1	1	0	3	0	1	0	2	24	552
248	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	0	1	1	1	1	7	20	663
249	1	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	0	1	1	1	1	7	20	663
250	0	1	0	1	1	1	1	1	0	1	1	1	0	0	0	0	1	0	0	1	0	1	1	6	18	736
251	1	1	0	1	1	1	1	1	1	0	1	1	0	0	0	0	1	0	0	1	1	0	1	5	16	828
252	0	0	1	1	1	1	1	1	1	0	1	1	0	0	0	0	1	0	0	1	1	0	1	5	16	828
253	1	0	1	1	1	1	1	1	0	0	1	1	0	0	0	0	1	0	0	1	0	0	1	4	14	946
254	0	1	1	1	1	1	1	1	0	0	1	1	0	0	0	0	1	0	0	1	0	0	1	4	14	946
255	1	1	1	1	1	1	1	1	0	1	0	0	1	0	0	0	0	1	0	2	0	1	0	2	12	1104

2.4.2 1/2-Octave Control Output Circuits (Refer to figure 4.)

When strapped for 1/2-octave filter control (OF), the 1/2-octave control output circuits receive parallel bcd input control signals (from storage registers U29-U36) and convert them to one-of-eleven 1/2-octave control output signals. Frequency ranges of the bands and PROM U10 decoding are shown in table 10.



CIRCUIT EQUIVALENT

	BCD LOGIC FORMULA	FREQUENCY RANGE
(A)	$40 + 80$	=40 THROUGH 99 kHz
(B)	$100 \cdot 400$	=500 THROUGH 599 kHz
(C)	$[40 + 80]\ [100 \cdot 400]$	=540 THROUGH 599 kHz
(D)	$200 \cdot 400$	=600 THROUGH 799 kHz
(E)	$(200 \cdot 400) + 800$	=600 THROUGH 999 kHz
(F)	$([40 + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) + 800$	=540 THROUGH 999 kHz
(G)	$\overline{([40 + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) + 800}$	$=\overline{\text{540 THROUGH 999 kHz}}$
(H)	$2 + 4 + 8 + 10 + 20$	=2 THROUGH 29.999 MHz
(I)	$\overline{2 + 4 + 8 + 10 + 20}$	$=\overline{\text{2 THROUGH 29.999 MHz}}$
(J)	$1 \cdot (\overline{2 + 4 + 8 + 10 + 20})$	=1 THROUGH 1.999 MHz
(K)	$[(200 \cdot 400) + 800] \cdot [1 \cdot (\overline{2 + 4 + 8 + 10 + 20})]$	=1.600 THROUGH 1.999 MHz
(L)	$1 + 2 + 4 + 8 + 10 + 20$	=1 THROUGH 29.999 MHz

	BCD LOGIC FORMULA	FREQUENCY RANGE
(M)	$([40 + 80] \cdot [100 + 400]) + (200 \cdot 400) + 800 + 1 + 2 + 4 + 8 + 10 + 20$	=540 kHz THROUGH 29.999 MHz
(N)	$\overline{([40 + 80] \cdot [100 + 400]) + (200 \cdot 400) + 800 + 1 + 2 + 4 + 8 + 10 + 20}$	$=\overline{\text{540 kHz THROUGH 29.999 MHz}}$
(O)	SAME AS (M)	$=\overline{\text{0 THROUGH 539 kHz}}$ (BAND 1)
(P)	$[([40 + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) + 800] \cdot (\overline{1 + 2 + 4 + 8 + 10 + 20})$	=540 THROUGH 999 kHz
(Q)	$([(200 \cdot 400) + 800] \cdot [1 \cdot (\overline{2 + 4 + 8 + 10 + 20})]) + 2 + 4 + 8 + 10 + 20$	=1.600 THROUGH 29.999 MHz
(R)	$\overline{([(200 \cdot 400) + 800] \cdot [1 \cdot (\overline{2 + 4 + 8 + 10 + 20})]) + 2 + 4 + 8 + 10 + 20}$	$=\overline{\text{1.600 THROUGH 29.999 MHz}}$
(S)	$[1 \cdot (\overline{2 + 4 + 8 + 10 + 20})] \cdot \overline{[([(200 \cdot 400) + 800] \cdot [1 \cdot (\overline{2 + 4 + 8 + 10 + 20})]) + 2 + 4 + 8 + 10 + 20]}$	=1.000 THROUGH 1.599 MHz
(T)	$([([40 + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) + 800] \cdot [\overline{1 + 2 + 4 + 8 + 10 + 20}]) +$ $([1 \cdot (\overline{2 + 4 + 8 + 10 + 20})] \cdot \overline{[([(200 \cdot 400) + 800] \cdot [1 \cdot (\overline{2 + 4 + 8 + 10 + 20})]) + 2 + 4 + 8 + 10 + 20]})$	=540 kHz THROUGH 1.599 MHz
(U)	$\overline{([([40 + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) \cdot 800] \cdot [\overline{1 + 2 + 4 + 8 + 10 + 20}]) +}$ $\overline{([1 \cdot (\overline{2 + 4 + 8 + 10 + 20})] \cdot \overline{[([(200 \cdot 400) + 800] \cdot [1 \cdot (\overline{2 + 4 + 8 + 10 + 20})]) + 2 + 4 + 8 + 10 + 20]})}$	$=\overline{\text{540 kHz THROUGH 1.599 MHz}}$
(V)	SAME AS (T)	=540 kHz THROUGH 1.599 MHz
(W)	SAME AS (U)	$=\overline{\text{540 kHz THROUGH 1.599 MHz}}$ (BAND 2)
(X)	$([(200 \cdot 400) + 800] \cdot [1 \cdot (\overline{2 + 4 + 8 + 10 + 20})]) + 2 + 4 + 8 + 10 + 20$	=1.600 THROUGH 29.999 MHz
(Y)	SAME AS (R)	$=\overline{\text{1.600 THROUGH 29.999 MHz}}$ (BAND 3)

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Band Control Output Circuits
Figure 3

Table 10. PROM U10, 1/2-Octave Control.

BAND	BAND FREQ RANGE (MHz)	HEXADECIMAL INPUTS	HEXADECIMAL INPUTS								OUTPUTS							
			1	2	4	8	10	20	40	80	1	2	3	4	5	6	7	8
			ADDRESS INPUTS															
			0	1	2	3	4	5	6	7								
*1	0-0.559	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
*2	0.560-1.599	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
*3	1.600-1.999	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	2.000-2.999	2	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
5	3.000-3.999	3	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
6	4.000-5.999	4	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
		5	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
7	6.000-7.999	6	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0
		7	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0
8	8.000-11.999	8	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
		9	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
		10	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
		11	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
9	12.000-15.999	12	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0
		13	1	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0
		14	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0
		15	1	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0
10	16.000-23.999	16	0	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0
		17	1	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0
		18	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0
		19	1	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0
		20	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0
		21	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0
		22	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1	0
		23	1	1	0	0	0	1	0	0	0	0	0	0	0	0	1	0
11	24.000-29.999	24	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1
		25	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1
		26	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	1
		27	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	1
		28	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1
		29	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1

*Bands 1, 2, and 3 not selected by PROM.

Refer to figure 4 and table 10 and note that any bcd frequency that lies between the low frequency of one band and the low frequency of the next higher band provides the associated 1/2-octave control output signal (logic 1 = enabled).

2.5 Fault and Monitor Circuits (Refer to figure 5.)

The following fault and monitor circuits are included in this control card:

a. Receiver fault signal (logic 1 = fault) is generated by a power supply fault (logic 1), a vbfo synthesizer fault (logic 1), or a synthesizer fault (logic 1). A power-on (restored) condition or a power supply fault input causes the receiver fault to be latched in the fault mode. The power supply fault is cleared by changing frequency. The synthesizer and vbfo synthesizer faults are cleared when the fault is removed.
b. Receive rf overload indication (logic 1 = overload) is generated by a preselector rf overload (logic 1) or a receive rf overload (logic 1) input. The +5 V dc connected through the diode in the preselector rf overload input line is a high-level protector that prevents any signal in excess of +5 V dc from being applied to NOR gate U37C.
c. Preselector fault indication (logic 1 = fault) is generated by a preselector fault (logic 1) input. The +5 V dc connected through the diode in the preselector fault input line is a high-level protector that prevents any signal in excess of +5 V dc from being applied to buffer/driver U3C.
d. 450-kHz enable (logic 1 = enable) is generated by an SSB mode (logic 1) input.

2.6 Tune Start Circuit (Refer to figure 6.)

The tune start pulse (ground pulse at P1-99) is initiated by making an operating frequency change and/or a change in local-remote status.

Tune start pulser U15A is a retriggerable, monostable multivibrator and holds P1-99 (through Q14) at ground as long as input U15A-4 is constantly changing. Tune start pulse width is a function of R32, C2, and the frequency of triggers applied at U15A-4.

When a local enable signal is initially applied, a tune start pulse is supplied at P1-99. The same is true when the local enable signal is initially removed.

When a local enable signal is not applied (logic 0 applied), $\overline{\text{clock inhibit}}$ is applied (logic 1), and a remote frequency change signal is applied; U16C is NANDed and supplies a logic 0 to U18C where it is ANDed and supplies a logic 1 to U15B-12. The logic 1 at U15B-12 causes a single pulse output. The pulse from U15B is applied to U15A-5 which supplies a tune start pulse output at P1-99.

When $\overline{\text{clock inhibit}}$ is applied (logic 1) and vbfo tune is not applied (logic 0 applied), a change of the front-panel tune control produces a local frequency change. The movement of the front-panel tune control causes the variable clock to be applied to U11A-1. The variable clock is ANDed by U11A, applied to and ANDed by U11B, and supplied as clock pulses through U13D to U15A-4. U15A produces a tune start pulse whose duration is controlled by R32, C2, and the continuous application of variable clock pulses (these continue to be applied until turning of the knob is stopped).

When $\overline{\text{clock inhibit}}$ is logic 0, U2C output is logic 1 and U2B output is logic 0 inhibiting U16C, U18C, and U15B. The logic 0 from U2B also inhibits U11B.

2.7 VBFO Tune Circuit (Refer to figure 6.)

When vbfo tune is logic 1, U17F output is logic 0 and U11A output is logic 0 inhibiting U11B. With vbfo at logic 1 and $\overline{\text{clock inhibit}}$ at logic 1, U11D and U11C are enabled and variable clock pulses applied at U11D-13 are supplied as vbfo clock pulses out at P1-85.

When vbfo tune is logic 1, a logic 1 output is supplied as WD1G at P1-69, and with no WD4 strobe applied a logic 0 output is supplied as WD3G at P1-68.

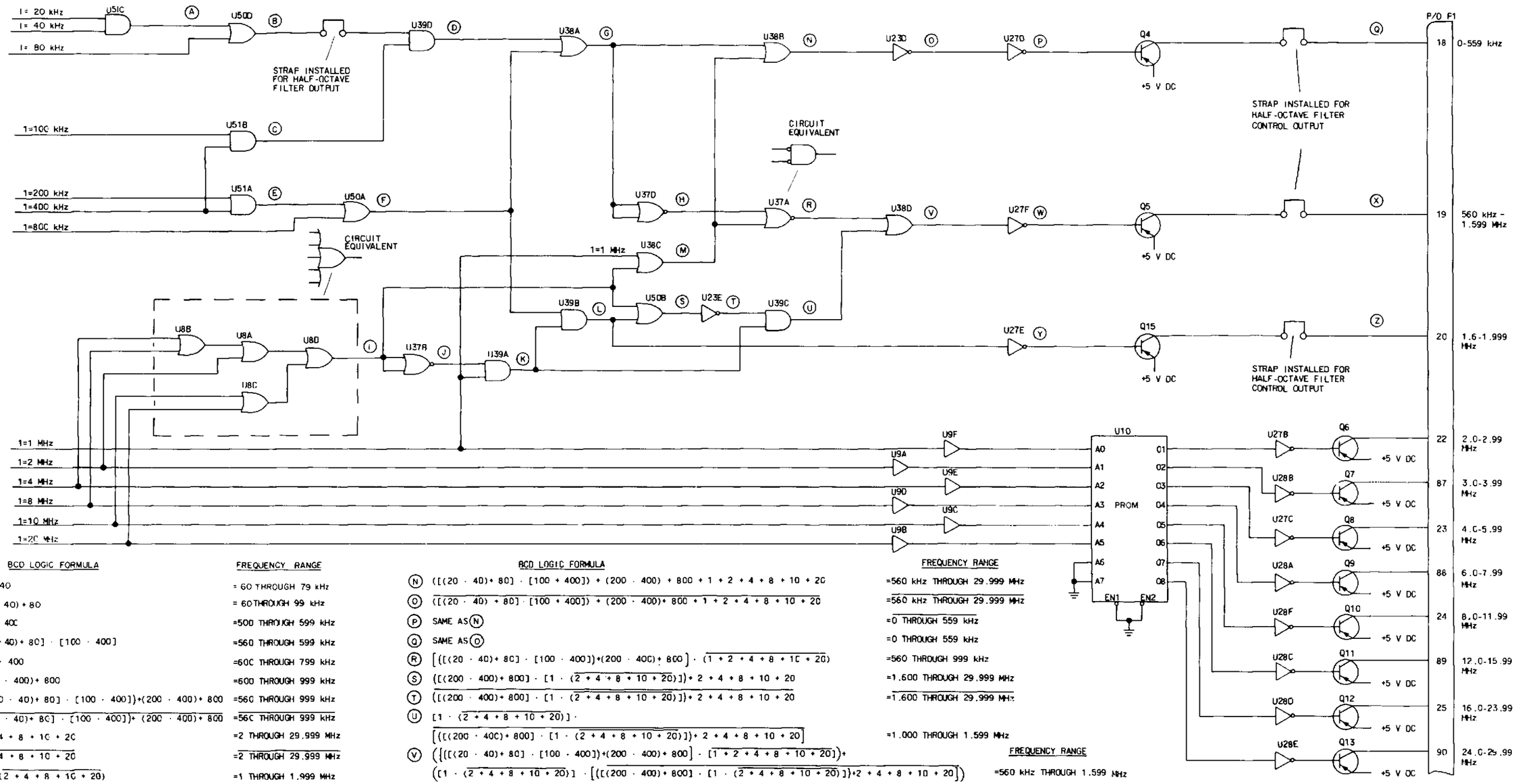
3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the control card are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 11 check total performance of the control card. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.



BCD LOGIC FORMULA	FREQUENCY RANGE
(A) 20 40	= 60 THROUGH 79 kHz
(B) (20 40) + 80	= 60 THROUGH 99 kHz
(C) 100 · 400	=500 THROUGH 599 kHz
(D) [(20 · 40) + 80] · [100 · 400]	=560 THROUGH 599 kHz
(E) 200 · 400	=600 THROUGH 799 kHz
(F) (200 · 400) + 800	=600 THROUGH 999 kHz
(G) ([(20 · 40) + 80] · [100 · 400]) + (200 · 400) + 800	=560 THROUGH 999 kHz
(H) $\overline{[(20 \cdot 40) + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) + 800}$	=560 THROUGH 999 kHz
(I) 2 + 4 + 8 + 10 + 20	=2 THROUGH 29.999 MHz
(J) $\overline{2 + 4 + 8 + 10 + 20}$	=2 THROUGH 29.999 MHz
(K) 1 · $\overline{(2 + 4 + 8 + 10 + 20)}$	=1 THROUGH 1.999 MHz
(L) [(200 · 400) + 800] · [1 · $\overline{(2 + 4 + 8 + 10 + 20)}$]	=1.600 THROUGH 1.999 MHz
(M) 1 + 2 + 4 + 8 + 10 + 20	=1 THROUGH 29.999 MHz

BCD LOGIC FORMULA	FREQUENCY RANGE
(N) ([(20 · 40) + 80] · [100 + 400]) + (200 · 400) + 800 + 1 + 2 + 4 + 8 + 10 + 20	=560 kHz THROUGH 29.999 MHz
(O) $\overline{([(20 \cdot 40) + 80] \cdot [100 + 400]) + (200 \cdot 400) + 800 + 1 + 2 + 4 + 8 + 10 + 20}$	=560 kHz THROUGH 29.999 MHz
(P) SAME AS (N)	=0 THROUGH 559 kHz
(Q) SAME AS (O)	=0 THROUGH 559 kHz
(R) $\left[([(20 \cdot 40) + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) + 800\right] \cdot \overline{(1 + 2 + 4 + 8 + 10 + 20)}$	=560 THROUGH 999 kHz
(S) $([(200 \cdot 400) + 800] \cdot [1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}]) + 2 + 4 + 8 + 10 + 20$	=1.600 THROUGH 29.999 MHz
(T) $\overline{([(200 \cdot 400) + 800] \cdot [1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}]) + 2 + 4 + 8 + 10 + 20}$	=1.600 THROUGH 29.999 MHz
(U) $[1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}] \cdot \overline{\left[([(200 \cdot 400) + 800] \cdot [1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}]) + 2 + 4 + 8 + 10 + 20\right]}$	=1.000 THROUGH 1.599 MHz
(V) $\left(\left\{\left[([(20 \cdot 40) + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) + 800\right] \cdot \overline{[1 + 2 + 4 + 8 + 10 + 20]}\right\} + \left([1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}] \cdot \left[([(200 \cdot 400) + 800] \cdot [1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}]) + 2 + 4 + 8 + 10 + 20\right]\right)$	=560 kHz THROUGH 1.599 MHz
(W) $\left(\left[([(20 \cdot 40) + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) + 800\right] \cdot \overline{[1 + 2 + 4 + 8 + 10 + 20]}\right) + \left([1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}] \cdot \left[([(200 \cdot 400) + 800] \cdot [1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}]) + 2 + 4 + 8 + 10 + 20\right]\right)$	=560 kHz THROUGH 1.599 MHz
(X) SAME AS (V)	=560 kHz THROUGH 1.599 MHz
(Y) $\overline{[(200 \cdot 400) + 800] \cdot [1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}]}$	=1.600 THROUGH 1.999 MHz
(Z) SAME AS (L)	=1.600 THROUGH 1.999 MHz

NOTE

(1) ALL SIGNALS ARE SHOWN FOR THEIR LOGIC 1 STATE. HALF-OCTAVE FILTER CONTROL OUTPUTS ARE LOGIC 1 WHEN ENABLED.

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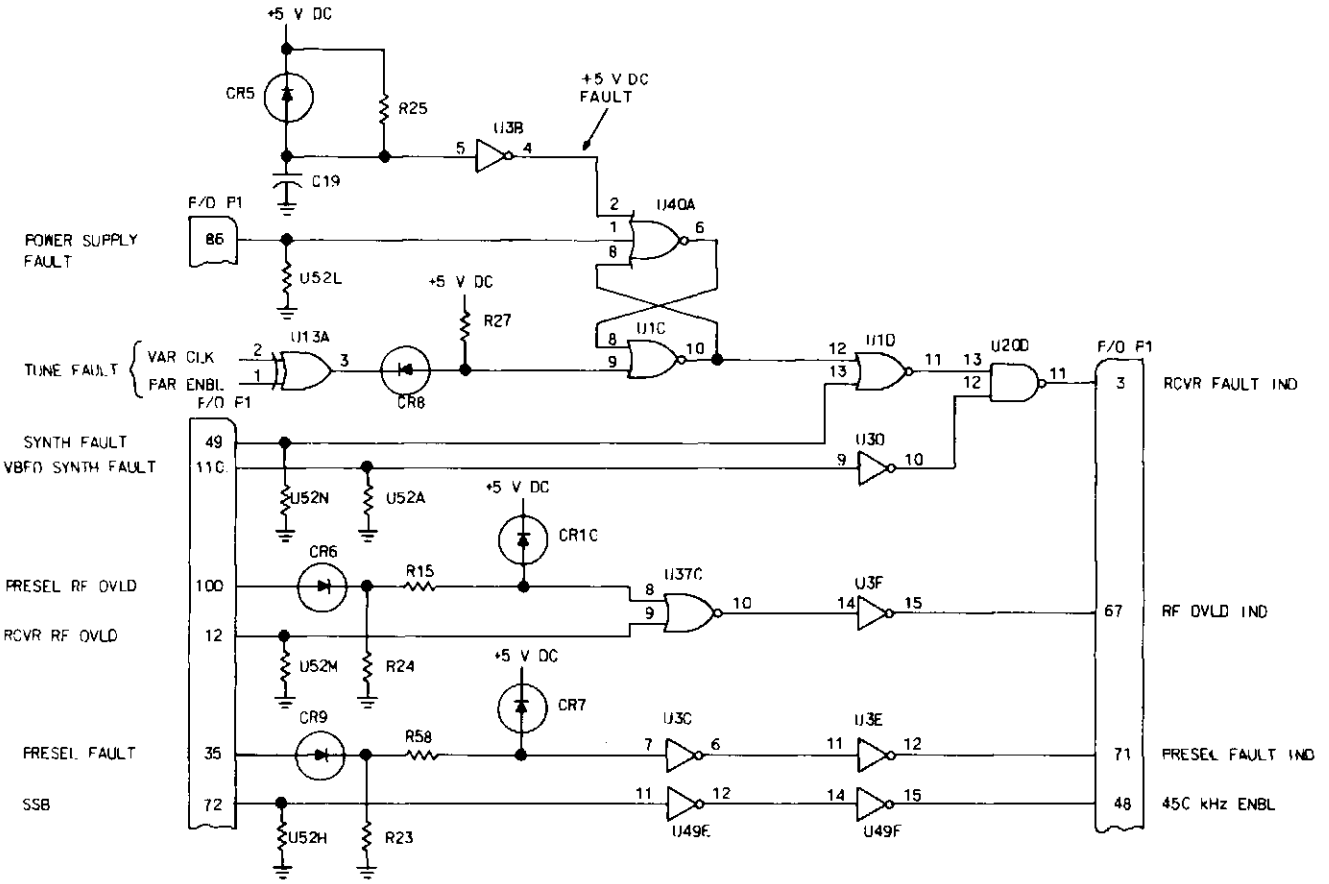
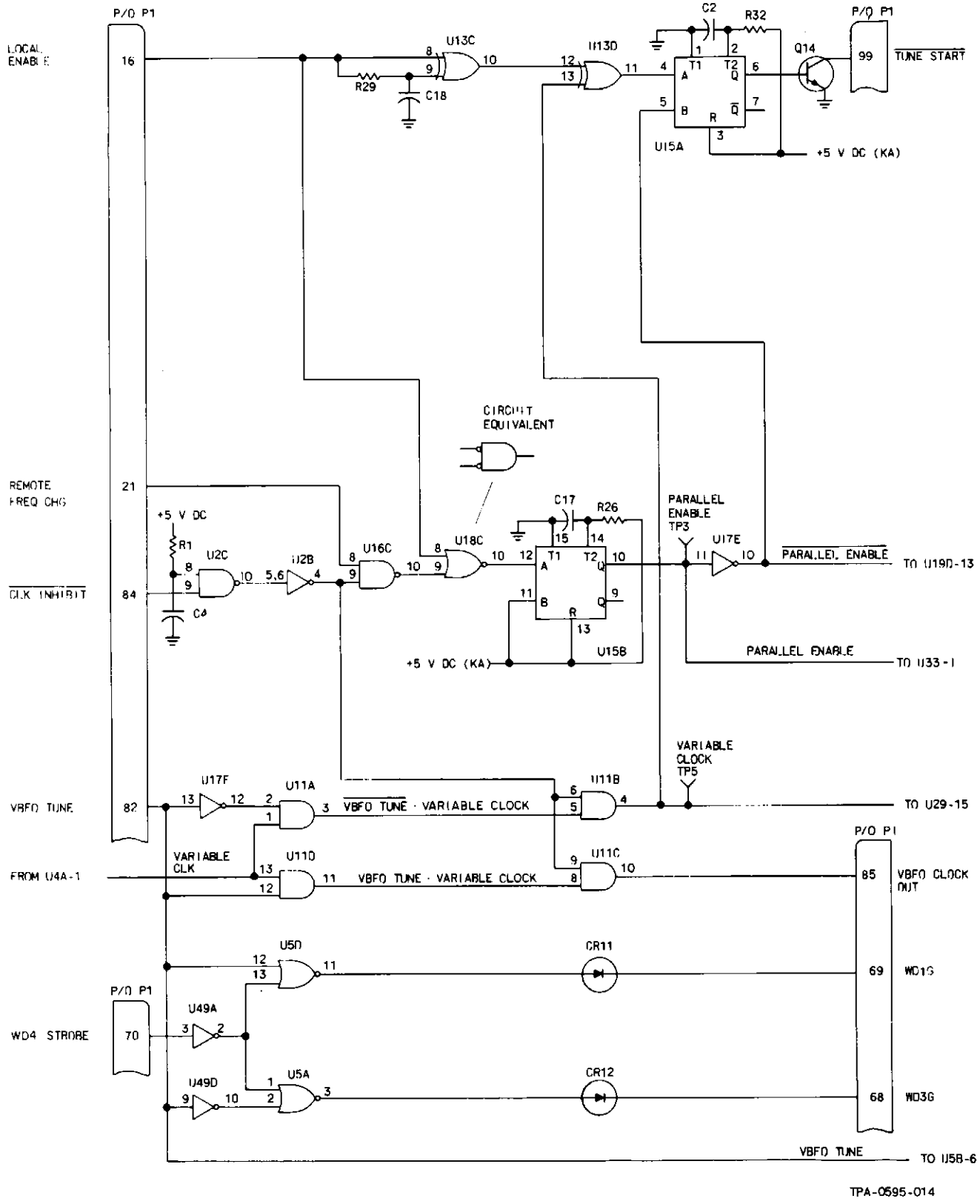
1/2-Octave Filter Control Output Circuits
Figure 4



Control and Fault Indications
Figure 5



Tune Start and Vbfo Control
Figure 6

Table 11. Control, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of unit containing the control that is to be tested. b. If installed, remove parallel input, parallel output, and serial interface. Note If removed, upon completion of control testing, reinstall parallel input, parallel output, and serial interface. c. Remove control. Install it on extender and place it in the unit. d. Set unit LINE SELECTOR for power source available (100/115/215/230 V ac). Note Ensure that proper fuse is installed for power source used. e. Connect unit to available power source. Caution In the following procedures, when applying +5-V dc or 0-V dc (ground) to the indicated points, apply these levels through a 100-ohm or more series limiting resistor. The +5-V dc source should be obtained from the receiver power supply so that the integrated circuit supply voltages are not exceeded by the applied levels.		
2. Initial outputs (Cont)	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to any. BANDWIDTH to any. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw.		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	b. Measure dc voltages between the following pins and ground (TP1, brown):		Check associated power supply.
	P1-45 P1-65 P1-114	+15 ±1.0 V dc +5 ±0.5 V dc -15 ±1.0 V dc	
	c. Note front-panel indications.	FREQUENCY·KHZ is 00 000.000 (Refer to test 9 for logic levels at 00 000.000). Note Because of keep-alive feature, previously stored FREQUENCY KHZ may be in memory.	Check U29 through U36, and variable clock circuit.
		RCV FAULT is lit. (logic 1 at P1-3).	Check U15B, U18C, U16C, and variable clock circuits.
	d. Check dc voltage at TP4 (3-state control).	NMT 0.5 V dc.	Check U19B, U19C, U17C, U2B, U2C, and associated circuits.
	e. Check dc voltage at TP5 (variable clock).	NMT 0.5 V dc.	Check U11B and associated circuits.
3. 3-State buffer control	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to any. BANDWIDTH to any. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Apply a ground to P1-113 (parallel frequency enable).		
	c. Measure dc voltage at TP 4.	NMT 0.5 V dc.	Check U19C and associated circuit.
	d. Apply a ground to P1-84 ($\overline{\text{clock inhibit}}$).		
(Cont)	e. Measure dc voltage at TP4.	NLT +3.0 V dc.	Check U2C, U2B, U19B, and associated circuit.

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	f. Remove P1-84 and P1-113 grounds.		
	g. Connect +5 V dc to P1-113.		
	h. Measure dc voltage at TP4.	NMT 0.5 V dc.	Check U19B and associated circuit.
	i. Set CONT to REM (removes +5 V dc from P1-16, local enable).		
	j. Measure dc voltage at TP4.	NLT +3.0 V dc.	Same as step 3.h.
	k. Remove +5 V dc from P1-113.		
4. Receiver fault latch	a. Connect an oscilloscope to P1-99 (tune start).		
	b. Front-panel controls set as follows: PWR to on. CONT to REM. MODE to any. BANDWIDTH to any. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	c. Apply momentary +5 V dc to P1-21 (remote frequency change).	Note that a tune start pulse is generated (displayed on oscilloscope).	Check U16C, U18C, U15, U17E, Q14, and associated circuit.
	d. Measure dc voltage at P1-3 (receiver fault indication).	NMT 0.5 V dc (RCV FAULT indicator goes out).	Check U16C, U18C, U15B, U13A, U1C, and associated circuit.
	e. Set CONT to LCL (applies +5 V dc to P1-16, local enable).		
	f. Apply a momentary +5 V dc to P1-86 (power supply fault).		
	g. Measure dc voltage at P1-3.	NLT +3.0 V dc (RCV FAULT indicator lights).	Check U40A, U1C, U1D, U20D, and associated circuit.
	h. Apply +5 V dc to P1-30 (rate (1)).		
	i. Measure dc voltage at P1-3.	NMT 0.5 V dc (RCV FAULT indicator goes out).	Check U11B, U13A, U1C, and associated circuit.
(Cont)	j. Remove +5 V dc from P1-30.		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	k. Measure dc voltage at P1-3.	NMT 0.5 V dc (RCV FAULT indicator remains out).	Same as step 4.i.
	l. Apply momentary +5 V dc to P1-86.		
	m. Measure dc voltage at P1-3.	NLT +3.0 V dc (RCV FAULT indicator lights).	Same as step 4.g.
	n. Apply momentary +5 V dc to P1-21 (several times).		
	o. Measure dc voltage at P1-3.	NLT +3.0 V dc (RCV FAULT indicator remains lit).	Check U18C and associated circuits.
	p. Apply a momentary +5 V dc to P1-30.		
5. Word 4 strobe routing	a. Front-panel controls set as follows: PWR to on. CONT to any. MODE to SSB/CW. BANDWIDTH to 16. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Apply +5 V dc to P1-70 (word 4 strobe).		
	c. Measure dc voltage at P1-69 (WDIG).	NLT +3.0 V dc.	Check U49A, U5D, and associated circuit.
	d. Measure dc voltage at P1-68 (WD3G).	NMT 0.5 V dc.	Check U49A, U5A, and associated circuit.
	e. Set BFO switch to TUNE (applies +5 V dc to P1-82, vbfo tune).		
	f. Measure dc voltage at P1-69.	NMT 0.5 V dc.	Same as step 5c.
	g. Measure dc voltage at P1-68.	NLT +3.0 V dc.	Same as step 5d.
	h. Remove +5 V dc from P1-70 and set BFO switch to FIX (removes +5 V dc from P1-82).		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
6. Tune start	a. Connect an oscilloscope to P1-99 (tune start).		
	b. Front-panel controls set as follows: PWR to on. CONT to REM. MODE to SSB/CW. BANDWIDTH to 16. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	c. Set CONT switch to LCL (applied +5 V dc to P1-16.	Note that a tune start pulse is generated (displayed on oscilloscope) when CONT switch is just switched to LCL.	Check U13C, U13D, U15A, Q14, and associated circuits.
	d. Set CONT switch to REM (removes +5 V dc from P1-16).	Note that a tune start pulse is generated when CONT switch is just switched to REM.	Same as step 6.a.
7. Counter parallel enable	a. Connect an oscilloscope to TP3 (parallel enable).		
	b. Front-panel controls set as follows: PWR to on. CONT to REM. MODE to any. BANDWIDTH to any. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw.		Check U16C, U18C, U15B and associated circuits.
	c. Apply a momentary +5 V dc to P1-21 (remote frequency change).	Note that a logic 1 parallel enable pulse is generated 0.5 to 2.5 ms long.	
	d. Repeat as often as necessary to obtain accurate pulse length.		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
8. Fault and interface circuits	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to any. BANDWIDTH to any. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Apply +5 V dc at P1-49 (synthesizer fault).		
	c. Measure dc voltage at P1-3 (receiver fault indication).	NLT +3.0 V dc (RCV FAULT indicator lights).	Check U1D, U20D, and associated circuits.
	d. Remove +5 V dc from P1-49.		
	e. Apply +5 V dc at P1-110 (vbfo synthesizer fault).		
	f. Measure dc voltage at P1-3 (receiver fault indication).	NLT +3.0 V dc (RCV FAULT indicator lights).	Check U3D, U20D, and associated circuits.
	g. Remove +5 V dc from P1-110.		
	h. Apply +5 V dc at P1-35 (preselector fault).		
	i. Measure dc voltage at P1-71 (preselector fault indication).	NLT +3.0 V dc (PRESEL FAULT indicator lights).	Check U3C, U3E, and associated circuits.
	j. Remove +5 V dc from P1-35.		
	k. Apply +5 V dc at P1-100 (preselector rf overload).		
	l. Measure dc voltage at P1-67 (rf overload indication).	NLT +3.0 V dc (RCV OVERLOAD indicator lights).	Check U37C, U3F, and associated circuits.
	m. Remove +5 V dc from P1-100.		
	n. Set MODE switch to SSB/CW (applies +5 V dc to P1-72, ssb enable).		
	o. Measure dc voltage at P1-48 (450-kHz enable).	NLT +3.0 V dc.	Check U49E, U49F, and associated circuits.
	p. Set MODE switch to AM (removes +5 V dc from P1-72).		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
9. Parallel frequency control	a. Front-panel controls set as follows: PWR to on. CONT to REM. MODE to SSB/CW. BANDWIDTH to USB. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Apply +5 V dc to P1-113 (parallel frequency enable).		
	c. Refer to chart below to apply any parallel bcd frequency input to P1.		
	d. With any noted bcd frequency input applied, momentarily apply +5 V dc to P1-Z1 (remote frequency change).		
	e. Remove +5 V dc from P1-113.		
	f. Remove applied bcd frequency input and measure dc voltages at all bcd input pins.	Should be same as noted frequency input in step c. (Front-panel FREQUENCY KHZ indicators should indicate the applied bcd frequency input of step c.)	Check U29 thru U36, U42 thru U48, and associated circuits.
	g. Repeat steps c, d, e, and f at several different frequency inputs.		
(Cont)			

BCD WT	BCD INPUT PINS (Hz)								LOGIC INPUTS FOR EACH DIGIT									
	1	10	100	1k	10k	100k	1M	10M										
	CONNECTOR PIN P1-( )								0	1	2	3	4	5	6	7	8	9
1	50	52	54	56	58	60	62	64	0	1	0	1	0	1	0	1	0	1
2	115	117	119	121	123	125	127	129	0	0	1	1	0	0	1	1	0	0
4	51	53	55	57	59	61	63	-	0	0	0	0	1	1	1	1	0	0
8	116	118	120	122	124	126	128	-	0	0	0	0	0	0	0	0	1	1

Logic 1 = +3.0 to +5.5 V dc. Logic 0 = NMT 0.5 V dc (ground).

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
9. (Cont)	h. Apply +5 V dc to P1-113 (parallel frequency enable).		
	i. Apply bcd frequency input for 00 000.000 kHz.		
	j. Momentarily apply +5 V dc to P1-21 (remote frequency change).		
	k. Remove +5 V dc from P1-113.		
	l. Remove bcd frequency input.		
	m. Set CONT switch to LCL (applied +5 V dc to P1-16, local enable).		
	n. Measure dc voltages at all bcd input pins.	Should be same as frequency applied. (Front-panel FREQUENCY KHZ indicators should indicate the applied bcd frequency input.)	Same as step 9.f.
	o. Repeat steps h thru m at each of the following frequencies: 11 111.111 22 222.222 23 333.333 24 444.444 25 555.555 26 666.666 27 777.777 28 888.888 29 999.999		
10. Band decoder, 1/2-octave (applicable only with OF strapping) (Cont)	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to SSB/CW. BANDWIDTH to USB. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Rotate TUNING knob thru the frequency range of the receiver. Note the exact frequency that each 1/2-octave band output changes (see table below).		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
10. (Cont)			

BAND	FREQUENCY RANGE (MHz)	LOGIC LEVELS P1-( )											CHECK
		18	19	20	22	87	23	88	24	89	25	90	
1	0.000-0.559	1	0	0	0	0	0	0	0	0	0	0	Q4
2	0.560-1.599	0	1	0	0	0	0	0	0	0	0	0	Q5
3	1.600-1.999	0	0	1	0	0	0	0	0	0	0	0	Q15
4	2.000-2.999	0	0	0	1	0	0	0	0	0	0	0	Q6
5	3.000-3.999	0	0	0	0	1	0	0	0	0	0	0	Q7
6	4.000-5.999	0	0	0	0	0	1	0	0	0	0	0	Q8
7	6.000-7.999	0	0	0	0	0	0	1	0	0	0	0	Q9
8	8.000-11.999	0	0	0	0	0	0	0	1	0	0	0	Q10
9	12.000-15.000	0	0	0	0	0	0	0	0	1	0	0	Q11
10	16.000-23.999	0	0	0	0	0	0	0	0	0	1	0	Q12
11	24.000-29.999	0	0	0	0	0	0	0	0	0	0	1	Q13

Logic 1 = +3.0 to 5.5-V dc (enable).
Logic 0 = NMT 0.5-V dc (disable).

11. Band decoder, standard (applicable only with SF strapping)

a. Front-panel controls set as follows:

PWR to on.
CONT to LCL.
MODE to SSB/CW.
BANDWIDTH to USB.
DIAL to FINE.
BFO to FIX.
AGC to FAST.
RF GAIN to full cw.

b. Rotate TUNING knob thru the frequency range of the receiver. Note the exact frequency that each standard band output changes. (See table that follows.)

BAND	FREQUENCY RANGE (MHz)	LOGIC LEVELS P1-( )			CHECK
		18	19	20	
1	0.000-0.539	0	1	1	U54, U23D
2	0.540-1.599	1	0	1	U54, U22A
3	1.600-29.999	1	1	0	U54, U23A

Logic 1 = open circuit (disable).
Logic 0 = ground (enable).

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
12. Clocked frequency counter, fine tune	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to SSB/CW. BANDWIDTH to USB. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Rotate the TUNING knob slowly in a clockwise direction.		
	c. Observe front-panel FREQUENCY KHZ display.	The lowest order digit is clocked up and carries over to the next higher digit as the TUNING knob is rotated.	Check variable clock at TP5. If clock available, check U29 thru U36. If clock not available, check U25 and associated circuits. If direction wrong, check input at P1-27.
	d. Rotate the TUNING knob slowly in a counterclockwise direction.		
	e. Observe front-panel FREQUENCY KHZ display.	The lowest order digit is clocked down and borrows from the next higher digit as the TUNING knob is rotated.	Same as step c.
	f. Repeat step b at increased speed and rotate clockwise thru entire frequency range plus.		
	g. Observe front-panel FREQUENCY KHZ display.	Same as step c. Note that when hundredths are clocked thru they carry over to tenths, when tenths are clocked thru they carry over to ones, etc. When 29 999.99 kHz is clocked thru it starts over at 000.00 kHz.	Same as step c.
(Cont)			

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
12. (Cont)	h. Repeat step d at increased speed and rotate counterclockwise thru entire frequency range plus.		
	i. Observe front-panel FREQUENCY KHZ display.	Same as step e. Note that when hundredths are clocked thru they borrow from tenths, when tenths are clocked thru they borrow from ones, etc. When 000.00 kHz is clocked thru it starts over at 29 999.99 kHz.	Same as step c.
13. Clocked frequency counter, coarse tune	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to SSB/CW. BANDWIDTH to USB. DIAL to CRS. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Rotate the TUNING knob slowly in a clockwise direction.		
	c. Observe front-panel FREQUENCY KHZ display.	The 10-kHz digit is clocked up and carries over to the next higher digit as the TUNING knob is rotated.	Check U34 thru U36 and associated circuits.
	d. Rotate the TUNING knob slowly in a counterclockwise direction.		
	e. Observe front-panel FREQUENCY KHZ display.	The 10-kHz digit is clocked down and borrows from the next higher digit as the TUNING knob is rotated.	Same as step c.
(Cont)	f. Repeat step b at increased speed and rotate clockwise thru entire frequency range plus.		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
13. (Cont)	g. Observe front-panel FREQUENCY KHZ display.	Same as step c. Note that when 10 kHz are clocked thru, they carry over to 100 kHz, when 100 kHz are clocked thru they carry over to 1 MHz, etc. When 29 990.00 kHz is clocked thru it starts over at 000.00 kHz.	Same as step c.
	h. Repeat step d at increased speed and rotate counterclockwise thru entire frequency range plus.		
	i. Observe front-panel FREQUENCY KHZ display.	Same as step e. Note that when 10 kHz are clocked thru they borrow from 100 kHz, when 100 kHz are clocked thru they borrow from 1 MHz, etc. When 000.00 kHz is clocked thru it starts over at 29 990.00 kHz.	Same as step c.
14. Clocked frequency counter, clock inhibit	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to SSB/CW. BANDWIDTH to USB. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. While rotating the TUNING knob and observing the FREQUENCY KHZ display, apply ground to P1-84 (clock inhibit).	Frequency display is clocked until +5 V dc is applied at P1-84, when the clocking is ceased and the front-panel FREQUENCY KHZ displays 000.00.	Check U2C, U2B, U17F, U11A, U11B, and associated circuits. If 000.00 is not displayed check U42 thru U4B and associated circuits.
(Cont)	c. Stop rotating the TUNING knob.		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
14. (Cont)	d. Remove ground from P1-84.		
	e. Observe FREQUENCY KHZ display.	Frequency last displayed, before +5 V dc was applied to P1-84, should be displayed.	Check U29 thru U36 and associated circuits.
15. Vbfo clock	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to SSB/CW. BANDWIDTH to USB. DIAL to FINE. BFO to TUNE. AGC to FAST. RF GAIN to full cw.		
	b. Rotate the TUNING knob slowly in a clockwise direction.		
	c. Observe front-panel VBFO OFFSET HZ display.	The tens-Hz digit is clocked up. (Note that carryover and up/down direction of the vbfo frequency is not a function of the control card).	Check U11D, U11C and associated circuits.
	d. Rotate the TUNING knob slowly in a counterclockwise direction.		
	e. Observe front-panel VBFO OFFSET HZ display.	The tens-Hz digit is clocked down.	Same as step c.
	f. Set DIAL switch to CRS.		
	g. Rotate the TUNING knob slowly in a clockwise direction.		
	h. Observe front-panel VBFO OFFSET HZ display.	The tens-Hz digit is clocked up at about the same speed as when the DIAL switch was set to FINE.	Check U25 and associated circuits.
	i. While rotating the TUNING knob and observing the VBFO OFFSET HZ display, apply ground to P1-84 (clock inhibit).	VBFO OFFSET HZ display is clocked until +5 V dc is applied at P1-84, when the clocking is ceased and the VBFO OFFSET HZ display is locked at the last frequency displayed.	Check U2C, U2B, U11C, and associated circuits.
(Cont)			

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
15. (Cont)	j. Stop rotating the TUNING knob.		
	k. Remove ground from P1-84.		
	l. Observe VBFO OFFSET HZ display.	VBFO OFFSET display should not change.	Same as step i.
16. Keep-alive checks	a. Front-panel controls set as follows: PWR to off. CONT to LCL. MODE to SSB/CW. BANDWIDTH to USB. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Disconnect external power from rear panel.		
	c. Discharge capacitors C14, C15, and C16 by temporarily placing a short across any one of them.		
	d. Connect +12-V dc power supply to external keep-alive; positive to TB3-4, negative to TB3-5.		
	e. Measure dc voltage at TP2.	+4.0 to +7.5 V dc.	Check CR3, Q16, and associated circuit.
	f. Remove external keep-alive supply from TB3.		
	g. Reconnect external power to rear panel.		
	h. Set PWR switch on.		
	i. Measure dc voltage at TP2.	+4.8 to +5.4 V dc.	Check VR1, Q3, and associated circuit.
	j. Set PWR switch off.		
	k. Disconnect external power from rear panel.		
	l. Discharge capacitors C14, C15, and C16.		
	m. Reconnect external power to rear panel.		
(Cont)	n. Set PWR switch on.		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
16. (Cont)	o. Note front-panel frequency reading.	000.00 kHz.	Check U29 thru U36 and associated circuit.
	p. Adjust front-panel TUNING knob for a 12 345.67 kHz frequency reading.		
	q. Set PWR switch off for several seconds.		
	r. Set PWR switch on.		
	s. Note front-panel frequency reading.	12 345.67 kHz.	Check C14, C15, C16, and associated circuit.
	t. Set PWR switch off.		
	u. Disconnect external power from rear panel for approximately 30 minutes.		
	v. Reconnect external power to rear panel.		
	w. Set PWR switch on.		
	x. Note front-panel frequency reading.	12 345.67 kHz.	Same as step 16.5.
17. Test complete	a. Set PWR switch off.		
	b. Disconnect external power from rear panel.		
	c. Remove control from extender and extender from unit.		
	d. Reinstall control in unit.		
	e. If removed in setup, reinstall parallel input, parallel output, and serial interface.		
	f. Reinstall top cover of unit.		

4. ALIGNMENT/ADJUSTMENT

4.1 Tuning Control

4.1.1 100-Hz Tuning Control

To provide 100-Hz tuning control, straps on the control must be positioned as shown in figure 7.

4.1.2 10-Hz Tuning Control

To provide 10-Hz tuning control, straps on the control must be positioned as shown in figure 7.

4.2 RF Filter Control

4.2.1 Standard Filters

To provide rf filter control when using standard rf bandpass, filtering, straps on control must be positioned as shown in figure 8.

4.2.2 1/2-Octave Filtering

To provide rf filter control when using 1/2-octave filtering, straps on control must be positioned as shown in figure 8.

5. REPAIR

Repair of the control card is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

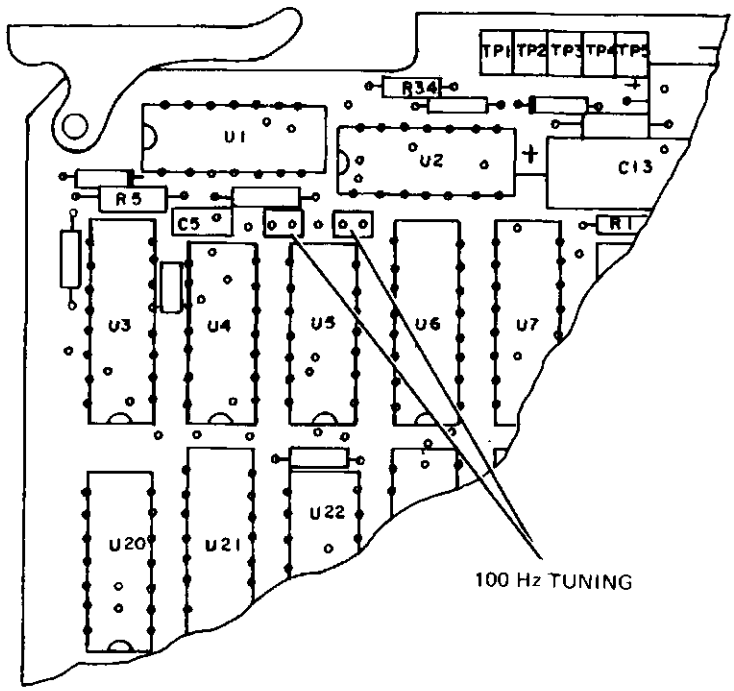
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram, figure 9. The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

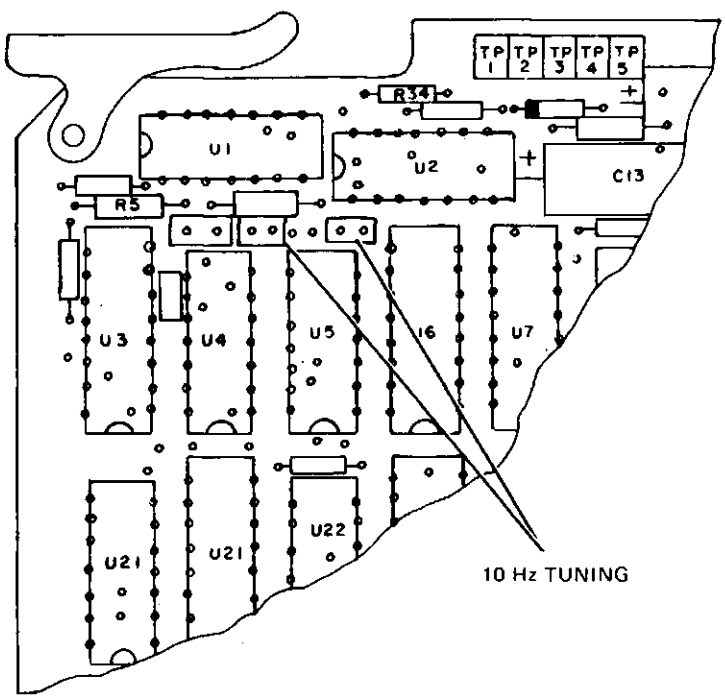
Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points to the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

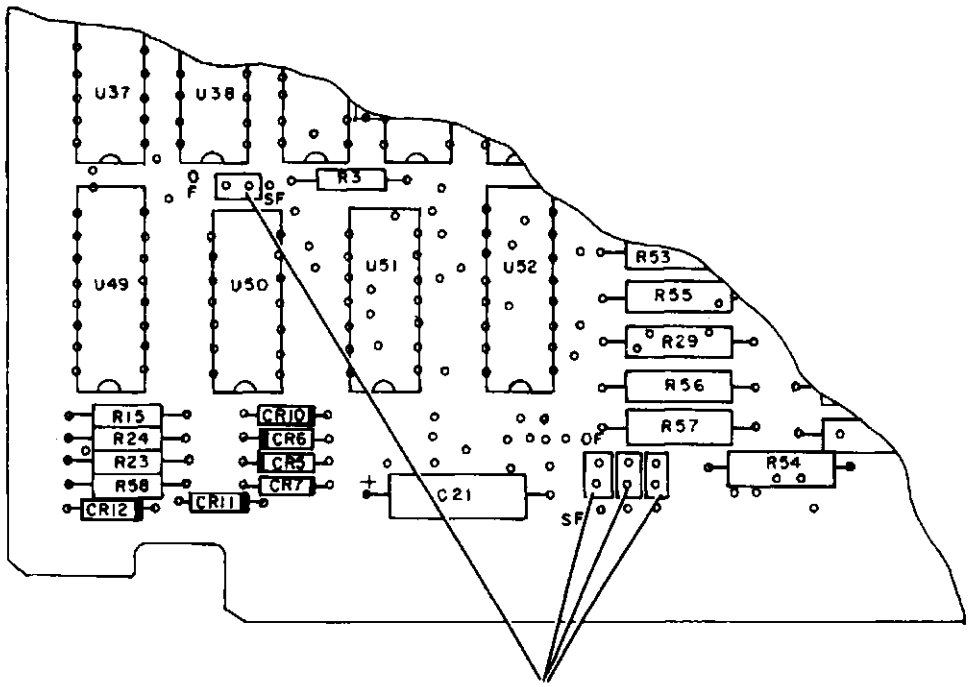
CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Control	638-6065-001	REV D



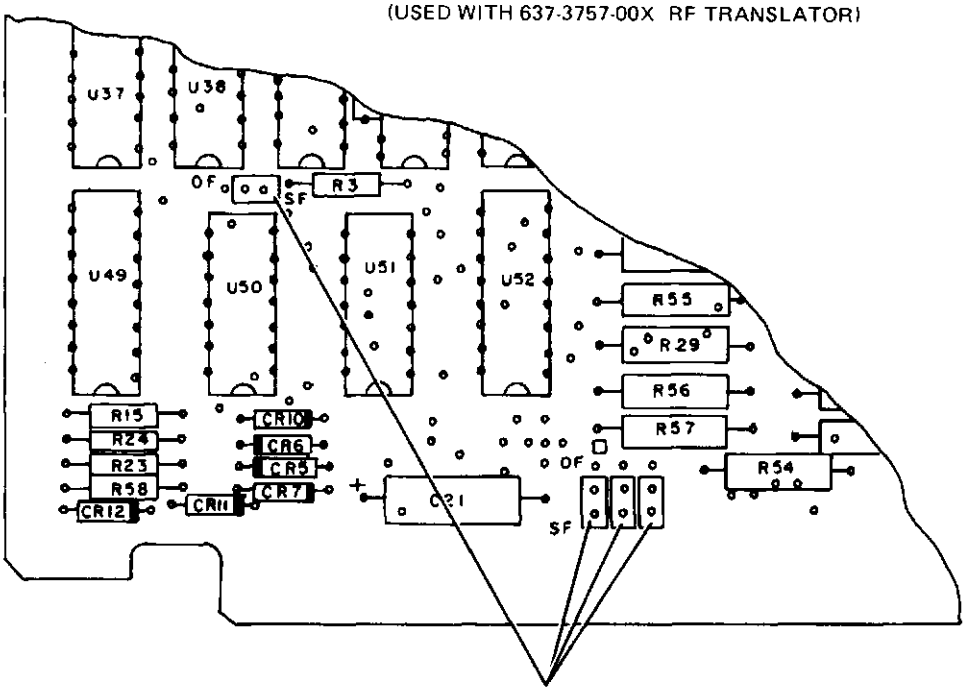


TPA-0849-019

Strapping for Tuning Control
Figure 7



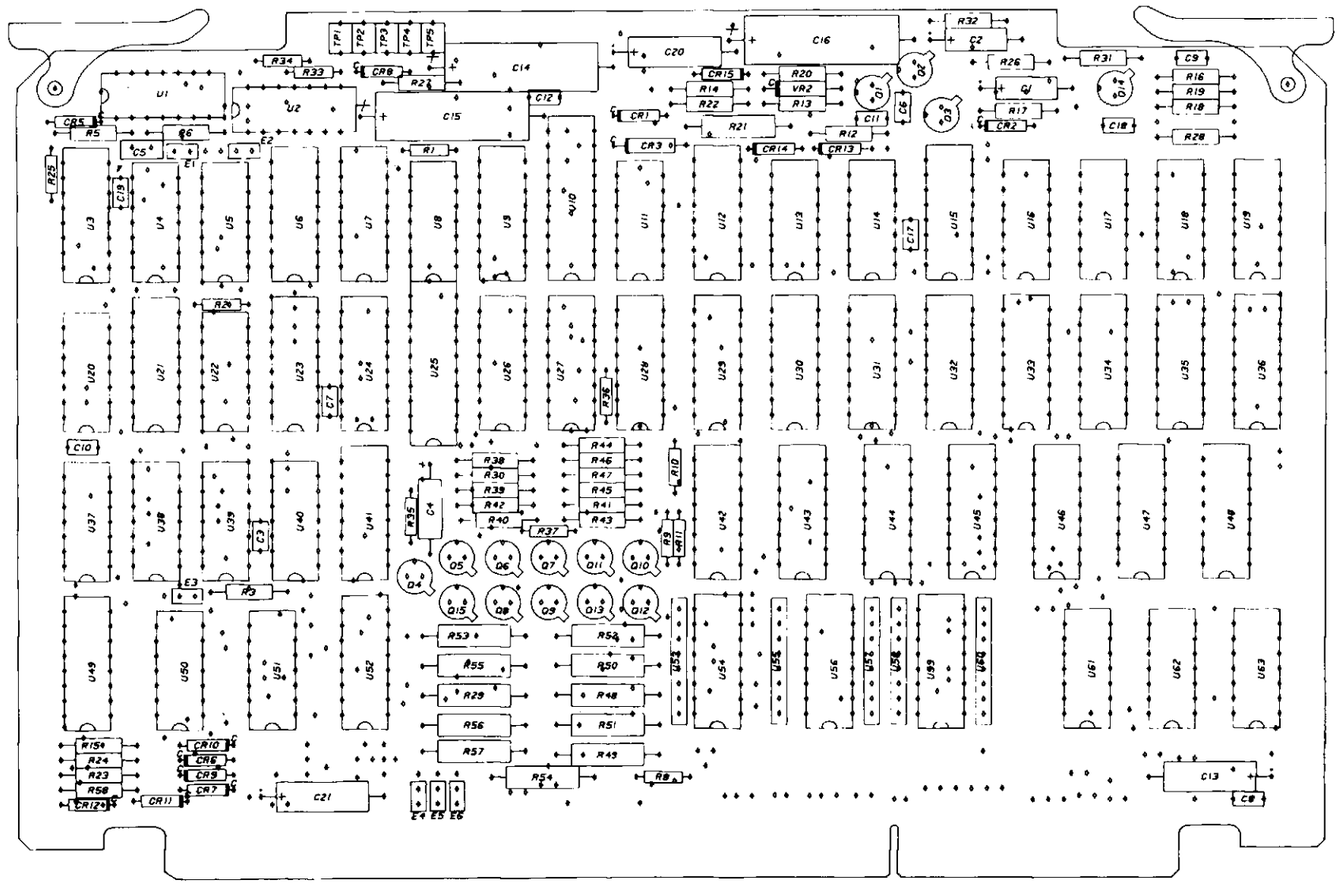
½ OCTAVE FILTERS
(USED WITH 637-3757-00X RF TRANSLATOR)



STANDARD FILTERS
(USED WITH 637-1767-00X RF TRANSLATOR)

TPA-0850-019

Strapping for Rf Filter Control
Figure 8



TPA-0903-014

Control, Schematic Diagram
Figure 9 (Sheet 1 of 6)

PARTS LIST

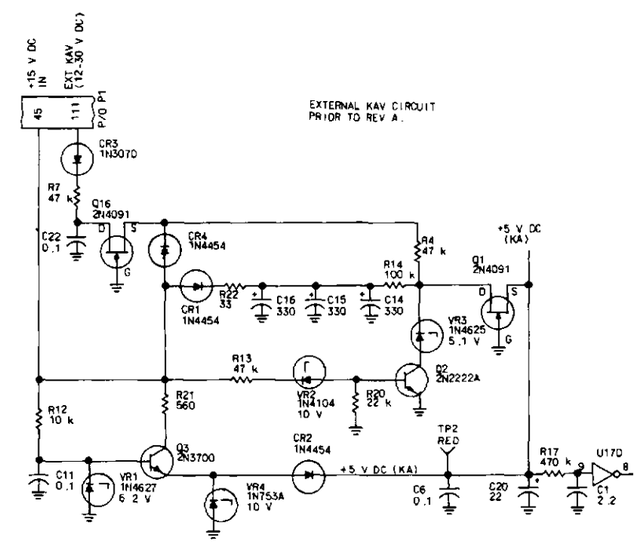
REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
	CONTROL	638-6065-001	
CR1,CR2	SEMICOND DEVICE 1N4454	353-3644-010	
CR3	SEMICOND DEVICE 1N3070	353-3083-000	
CR4	SEMICOND DEVICE 1N4454 (A1)	353-3644-010	
CR5-CR12	SEMICOND DEVICE 1N4454	353-3644-010	
CR13-CR15	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V (A1)	913-5019-200	
C1,C2	CAPACITOR,FXD ELCTLT, 2.2UF, 10%, 20V	184-9086-430	
C3	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C4	CAPACITOR,FXD ELCTLT, 2.2UF, 10%, 20V	184-9086-430	
C5	CAPACITOR,FXD MICA DIEL, 68PF, 5%, 50V	912-4141-330	
C6-C12	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C13	CAPACITOR,FXD ELCTLT, 22UF, 10%, 15V	184-9086-310	
C14-C16	CAPACITOR,FXD ELCTLT, 330UF, POR20%, 20V	184-9117-040	
C17-C19	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C20	CAPACITOR,FXD ELCTLT, 22UF, 10%, 15V	184-9086-310	
C21	CAPACITOR,FXD ELCTLT, 15UF, 10%, 20V	184-9086-490	
Q1	TRANSISTOR 2N4091	352-0759-010	
Q2	TRANSISTOR 2N2222A	352-0661-020	
Q3	TRANSISTOR 2N2222A	352-0661-020	
Q4-Q13	TRANSISTOR 2N2907A	352-0551-010	
Q14	TRANSISTOR 2N2222A	352-0661-020	
Q15	TRANSISTOR 2N2907A	352-0551-010	
Q16	TRANSISTOR 2N4091(A1)	352-0759-010	
R1	RESISTOR,FXD CMPSN, 470K, 10%, 1/8W	745-2437-000	
R2	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R3	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W	745-0809-000	
R4	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W	745-0809-000	
R5	RESISTOR,FXD FILM, 88.7K, 1%, 1/8W	705-3605-930	
R6	RESISTOR,FXD FILM, 178K, 1%, 1/8W	705-1104-000	
R7	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W	745-0809-000	
R8-R11	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R12	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W (A1)	745-0785-000	
R12	RESISTOR,FXD CMPSN, 27K, 10%, 1/4W	745-0800-000	
R13	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W (A1)	745-0809-000	
R13	RESISTOR,FXD CMPSN, 33K, 10%, 1/4W	745-0803-000	
R14	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W (A1)	745-0821-000	
R14	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W	745-0809-000	
R15	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000	
R16	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R17,R18	RESISTOR,FXD CMPSN, 0.47MEGO, 10%, 1/4W	745-0845-000	
R19	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R20	RESISTOR,FXD CMPSN, 22K, 10%, 1/4W (A1)	745-0797-000	
R20	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000	
R21	RESISTOR,FXD CMPSN, 560 OHMS, 10%, 1/2W (A1)	745-1342-000	
R21	RESISTOR,FXD CMPSN, 6.8K, 10%, 1/2W	745-1387-000	
R22	RESISTOR,FXD CMPSN, 33 OHMS, 10%, 1/4W	745-0695-000	
R23,R24	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R25,R26	RESISTOR,FXD CMPSN, 0.47MEGO, 10%, 1/4W	745-0845-000	
R27,R28	RESISTOR,FXD CMPSN, 0.22MEGO, 10%, 1/4W	745-0833-000	
R29	RESISTOR,FXD 1.5K, 1%, 1W	747-1499-591	
R30	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/4W	745-0761-000	
R31	RESISTOR,FXD CMPSN, 15K, 10%, 1/4W	745-0791-000	
R32	RESISTOR,FXD CMPSN, 0.22MEGO, 10%, 1/4W	745-0833-000	
R33,R34	RESISTOR,FXD CMPSN, 470K, 10%, 1/8W	745-2437-000	
R35-R37	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R38-R47	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/4W	745-0761-000	
R48	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/2W	745-1359-000	
R49	RESISTOR,FXD 1.5K, 1%, 1W	747-1499-591	
R50	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/2W	745-1359-000	
R51	RESISTOR,FXD 1.5K, 1%, 1W	747-1499-591	
R52-R55	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/2W	745-1359-000	
R56,R57	RESISTOR,FXD 1.5K, 1%, 1W	747-1499-591	
R58	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000	
TP1	JACK,TIP BRN	360-0464-070	
TP2	JACK,TIP RED	360-0484-020	
TP3	JACK,TIP ORN	360-0484-050	
TP4	JACK,TIP YEL	360-0484-060	
TP5	JACK,TIP GRN	360-0484-040	
U1	INTEGRATED CIRCUIT 4001BPC	351-8159-320	
U2	INTEGRATED CIRCUIT 4011BPC	351-8159-340	
U3	INTEGRATED CIRCUIT F4049BPC	351-8159-210	
U4	INTEGRATED CIRCUIT 4013BPC	351-8159-110	
U5	INTEGRATED CIRCUIT 4001BPC	351-8159-320	
U6	INTEGRATED CIRCUIT 4040BPC	351-8159-240	
U7	INTEGRATED CIRCUIT F4051PC	351-8227-010	
U8	INTEGRATED CIRCUIT MC14071BCP	351-8287-010	
U9	INTEGRATED CIRCUIT 4050BPC	351-8159-220	
U10	PROM, BAND DECODER	614-0133-013	
U11	INTEGRATED CIRCUIT MC14081BCP	351-8287-030	
U12	RESISTOR NTWK 1M, 5%, 1.25W PKG	350-4030-150	
U13	INTEGRATED CIRCUIT MC14070BCP	351-8407-010	
U14	INTEGRATED CIRCUIT 4016BPC	351-8159-070	
U15	INTEGRATED CIRCUIT MC14528BCP	351-8421-020	
U16	INTEGRATED CIRCUIT 4011BPC	351-8159-340	
U17	INTEGRATED CIRCUIT MC14069UBPC	351-8287-080	
U18	INTEGRATED CIRCUIT 4001BPC	351-8159-320	
U19,U20	INTEGRATED CIRCUIT 4011BPC	351-8159-340	
U21	INTEGRATED CIRCUIT MC14018BCP	351-8253-010	
U22	INTEGRATED CIRCUIT 4011BPC	351-8159-340	
U23	INTEGRATED CIRCUIT F4049BPC	351-8159-210	
U24	INTEGRATED CIRCUIT F4051PC	351-8227-010	
U25	PROM,RATE DECODER (A2)	614-0133-010	

PARTS LIST (Cont)

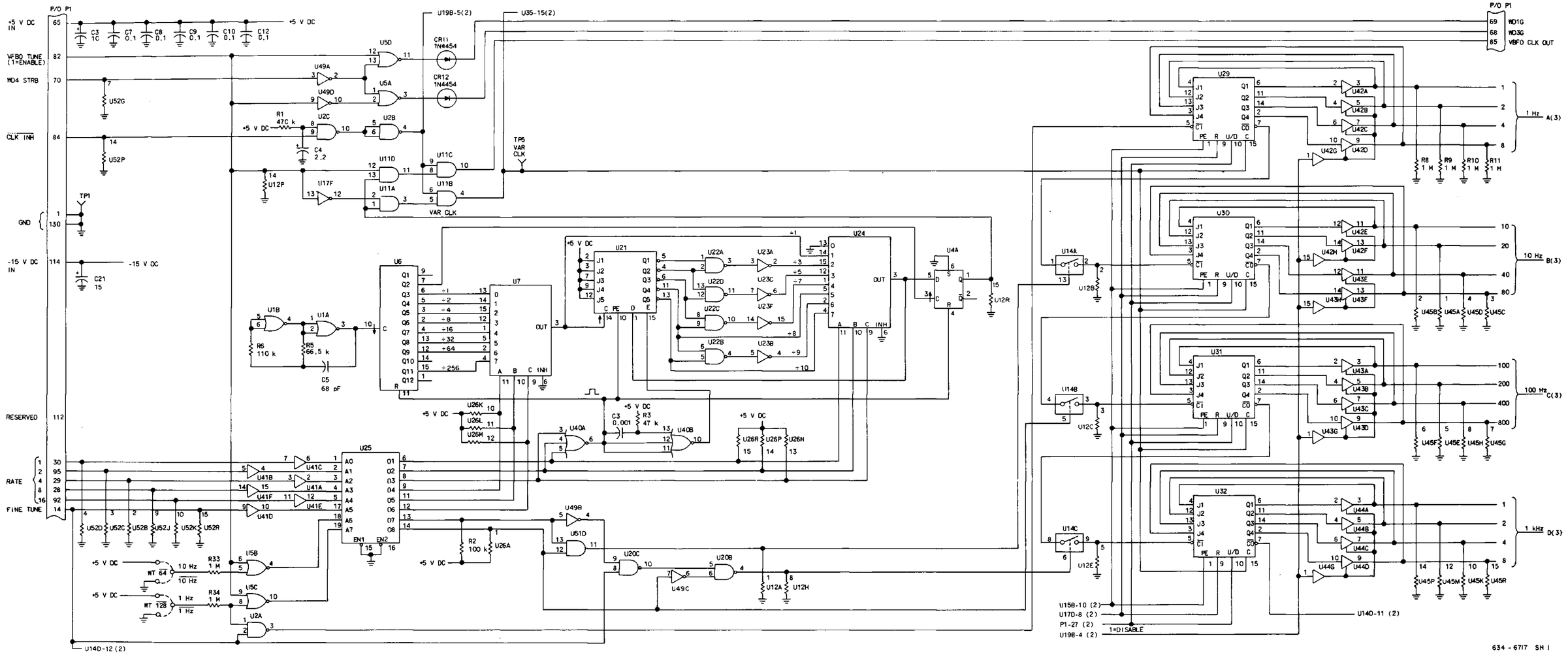
REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
U25	PROM,RATE DECODER	614-0133-012	
U26	RESISTOR NTWK 100K, 5%, 1.25W PKG	350-4030-130	
U27,U28	INTEGRATED CIRCUIT F4049BPC	351-8159-210	
U29-U36	INTEGRATED CIRCUIT CD4510BCN	351-8497-010	
U37	INTEGRATED CIRCUIT 4001BPC	351-8159-320	
U38	INTEGRATED CIRCUIT MC14071BCP	351-8287-010	
U39	INTEGRATED CIRCUIT MC14081BCP	351-8287-030	
U40	INTEGRATED CIRCUIT 4025BPC	351-8159-370	
U41	INTEGRATED CIRCUIT 4050BPC	351-8159-220	
U42-U44	INTEGRATED CIRCUIT MC14503BCP	351-8490-010	
U45	RESISTOR NTWK 1M, 5%, 1.25W PKG	350-4030-150	
U46	INTEGRATED CIRCUIT MC14503BCP	351-8490-010	
U47	RESISTOR NTWK 1M, 5%, 1.25W PKG	350-4030-150	
U48	INTEGRATED CIRCUIT MC14503BCP	351-8490-010	
U49	INTEGRATED CIRCUIT F4049BPC	351-8159-210	
U50	INTEGRATED CIRCUIT MC14071BCP	351-8287-010	
U51	INTEGRATED CIRCUIT MC14081BCP	351-8287-030	
U52	RESISTOR NTWK 1M, 5%, 1.25W PKG	350-4030-150	
U53	RESISTOR NTWK FILM, 15K, 2%, 1W	350-4046-770	
U54	INTEGRATED CIRCUIT CA3081	351-7802-020	
U55	RESISTOR NTWK FILM, 15K, 2%, 1W	350-4046-770	
U56	INTEGRATED CIRCUIT CA3081	351-7802-020	
U57,U58	RESISTOR NTWK FILM, 15K, 2%, 1W	350-4046-770	
U59	INTEGRATED CIRCUIT CA3081	351-7802-020	
U60	RESISTOR NTWK FILM, 15K, 2%, 1W	350-4046-770	
U61-U63	INTEGRATED CIRCUIT MC14069BCP	351-8287-080	
VR1	SEMICOND DEVICE 1N4627(A1)	353-3591-510	
VR2	SEMICOND DEVICE 1N4104	353-3591-060	
VR3	SEMICOND DEVICE 1N4625(A1)	353-3591-490	
VR4	SEMICOND DEVICE 1N758A(A1)	353-2724-000	

MODIFICATION HISTORY

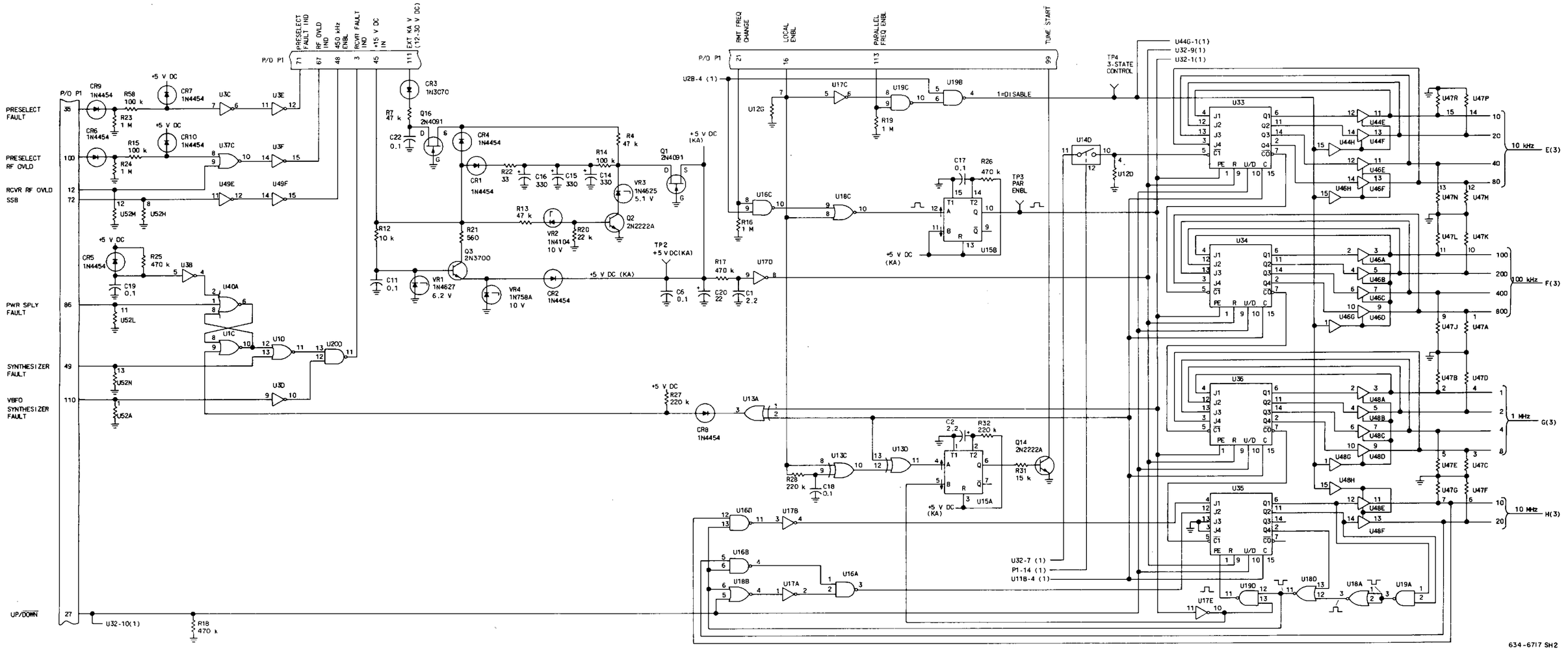
REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	External KAV (keep-alive voltage) circuit changed. Circuit was as shown in diagram below. Deleted: CR4, 1N4454. C22, 0.01 µF. Q16, 2N4091. R4, 47 kΩ. R7, 47 kΩ. VR1, 1N4627. VR3, 1N4625. VR4, 1N758A. Changed: Q3 from 2N3700 to 2N2222A. R12 from 10 kΩ to 27 kΩ. R13 from 47 kΩ to 33 kΩ. R14 from 100 kΩ to 47 kΩ. R20 from 22 kΩ to 10 kΩ. R21 from 560 Ω to 6800 Ω. Added: CR13, 1N4454. CR14, 1N4454. CR15, 1N4454.	REV A and above
A2	Changed PROM U25 (Tuning Rate Decoder) from 614-0133-010 to 614-0133-012.	REV C and above



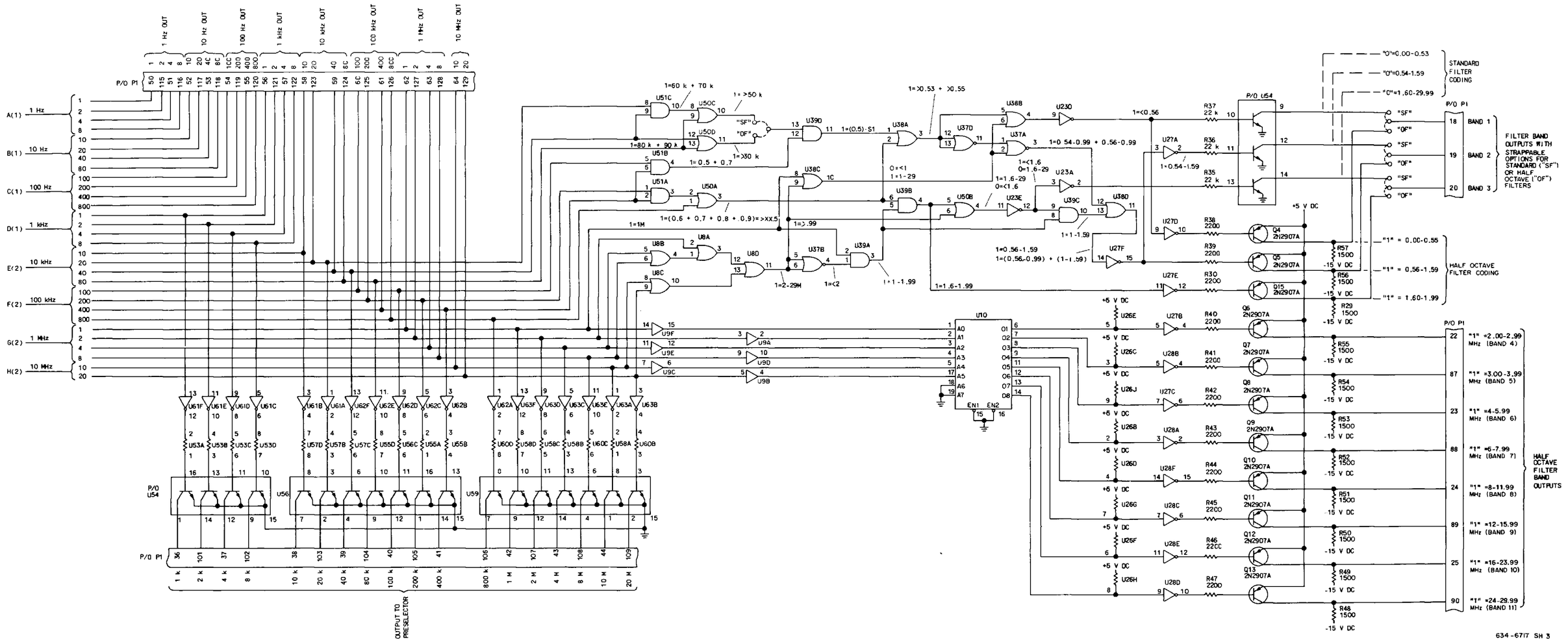
Control, Schematic Diagram
Figure 9 (Sheet 2)



Control, Schematic Diagram
Figure 9 (Sheet 3)



Control, Schematic Diagram
Figure 9 (Sheet 4)



Control, Schematic Diagram
Figure 9 (Sheet 5)

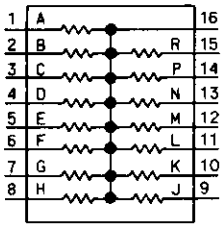
NOTES:

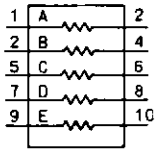
1. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS.

2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.

3. U12, U45, U47, U52 (1 M)
U26 (100 k)

U53, U55, U57
U58, U60 (15 k)





4. NONSTANDARD ABBREVIATION
KA-KEEP ALIVE

MICROCIRCUIT INFORMATION

U NO.	TYPE	PWR (V DC) +5	+5 KA	GND	SPARE SECTIONS
U1	F4001BPC	14		7	
U2	F4011BPC		14	7	D
U3	F4049BPC	1		8	
U4	F4013BPC	14		7	B
U5	R4001BPC	14		7	
U6	F4040BPC	16		8	
U7	F4051PC	16		7, 8	
U8	MC14071BCP	14		7	
U9	F4050PC	1		8	
* U10	74S471	20		10	
U11	MC14081BCP		14	7	
U12	NOTE 3			16	F, J, L, M, N
U13	MC14070BCP		14	7	B
U14	F4016BPC		14	7	
U15	MC14528BCP		16	8	
U16	F4011BPC		14	7	
U17	MC14069BCP		14	7	
U18	F4001BPC		14	7	
U19	F4011BPC		14	7	
U20	F4011BPC	14		7	A
U21	MC14018BCP	16		8	
U22	F4011BPC	14		7	
U23	F4049BPC	1		8	
U24	F4051PC	16		7, 8	
(A1) ** U25	74S471	20		10	
U26	NOTE 3	16			
U27	F4049BPC	1		8	
U28	F4049BPC	1		8	
U29	CD4510BCN		16	8	
U30	CD4510BCN		16	8	
U31	CD4510BCN		16	8	
U32	CD4510BCN		16	8	

U NO.	TYPE	PWR (V DC) +5	+5 KA	GND	SPARE SECTIONS
U33	CD4510BCN		16	8	
U34	CD4510BCN		16	8	
U35	CD4510BCN		16	8	
U36	CD4510BCN		16	8	
U37	F4001BPC	14		7	
U38	MC14071BPC	14		7	
U39	MC14081BCP	14		7	
U40	F4025BPC	14		7	
U41	F4050PC	1		8	
U42	MC14503BCP		16	8	
U43	MC14503BCP		16	8	
U44	MC14503BCP		16	8	
U45	NOTE 3			16	J, L, N
U46	MC14503BCP		16	8	
U47	NOTE 3			16	H
U48	MC14503BCP		16	8	
U49	F4049BPC	1		8	
U50	MC14071BCP	14		7	
U51	MC14081BCP	14		7	
U52	NOTE 3			16	
U53	NOTE3				
U54	CA3081			5	
U55	NOTE 3				
U56	CA3081			5	
U57	NOTE 3				A
U58	NOTE 3				
U59	CA3081			5	
U60	NOTE 3				A
U61	MC14069BCP	14		7	
U62	MC14069BCP	14		7	
U63	MC14069BCP	14		7	

* PROM, BAND DECODER, PROGRAMMED PN 614-0133-013.
(A1) ** PROM, TUNING RATE DECODER, PROGRAMMED PN 614-0133-012.

634-6717 SH 4

Control, Schematic Diagram
Figure 9 (Sheet 6)

Parallel Input (635-0751-001, -002)

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

523-0767949-002211
2nd Edition, 1 June 1978

1. DESCRIPTION

Parallel Input 635-0751-001, -002, shown in figure 1, is a 2-layer planar card with a 130-pin (2 layers, 65 pins each) edge-on connector. All test points are mounted at the top edge of the card for easy access with the card installed in the unit.

2. PRINCIPLES OF OPERATION

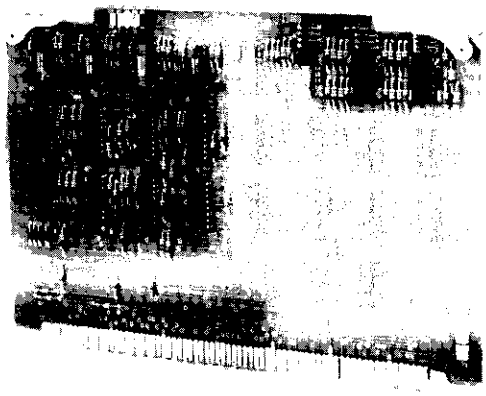
2.1 General

The parallel input card consists of two primary circuits: sixteen 8-channel multiplexers, and five gate generators. Each multiplexer receives up to eight inputs developed by the unit front panel controls. Address bits, from the serial interface card, select individual inputs for transfer to the single output from the multiplexer. These address bits are developed from word gate signals produced by the gate generator circuits.

2.2 Multiplexers

The multiplexers are integrated circuits functioning as 8-channel data selectors. (Refer to figure 2 for a block diagram and truth table of the component.) Note, from reference to the schematic diagram, figure 5, that the circuit arrangement is two sections of eight multiplexers each. The MX8 input selects the active section. When at a logic 1 level, the disable input of the multiplexer keeps the output at a high impedance. A logic 0 input allows the output to be developed from the eight input lines. Inverter U10F keeps one section disabled while the other is enabled.

The MX1, MX2, and MX4 inputs, applied simultaneously to all multiplexers, controls which of the eight input signals to each multiplexer is coupled to the output line. (Refer to the truth table of figure 2.) The resulting output signals from the eight multiplexers are eight data bits of the control word for

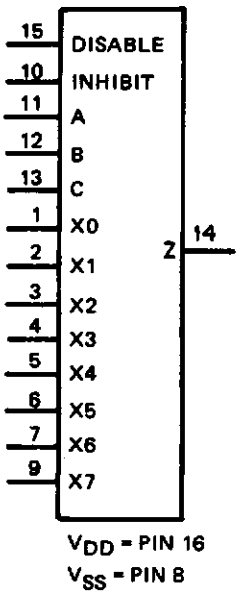


TP5-2312-017

Parallel Input
Figure 1

NOTICE: This section replaces first edition dated 1 June 1977.

BLOCK DIAGRAM



TRUTH TABLE

C	B	A	INHIBIT	DISABLE	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
X	X	X	1	0	0
X	X	X	X	1	HIGH IMPEDANCE

X = DON'T CARE

TP5-2026-011

8-Channel Data Selector MC14512
Figure 2

the unit under control. These data bits are coupled to the serial interface card for parallel-to-serial conversion, word formation, and application to the control bus.

2.3 Gate Generators

When a front panel control is switched to a different position, a gate signal is developed by one of five gate generators. Each of these generator circuits is two multivibrators that develop a single output pulse. The output is a word or address gate signal applied to the serial interface card.

The two multivibrators are connected in series. (Refer to the schematic diagram, figure 5.) An input pulse to the first multivibrator causes an output pulse from that multivibrator of about 0.1 second width.

The output pulse from the first multivibrator is the input to the second multivibrator. The second circuit does not trigger until the end (1-to-0 transition) of the first output pulse. This delay gives time for switch settling into the final position selected.

The output from the second multivibrator is a 0.1-millisecond pulse for the word gates and a 10-microsecond pulse for the address gate. Figure 3 shows a block diagram and timing waveforms for the multivibrators used in the word and address gate generator circuits.

3. TESTING/TROUBLESHOOTING PROCEDURES

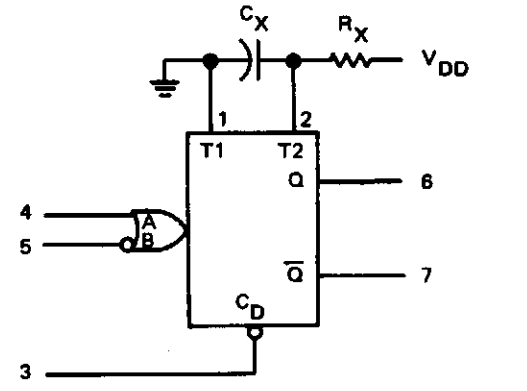
3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the parallel input are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 1 check total performance of the parallel input. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

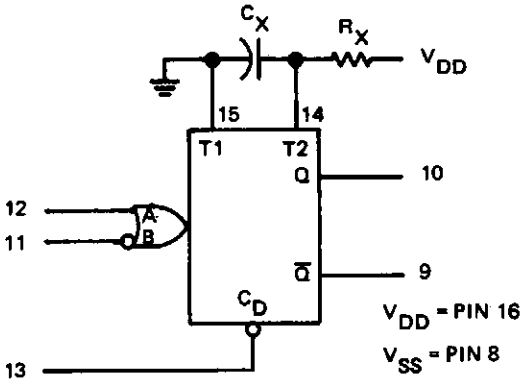
BLOCK DIAGRAM



A INPUT TERMINAL CLOCKS ON 0-TO-1 TRANSITION.

B INPUT TERMINAL CLOCKS ON 1-TO-0 TRANSITION.

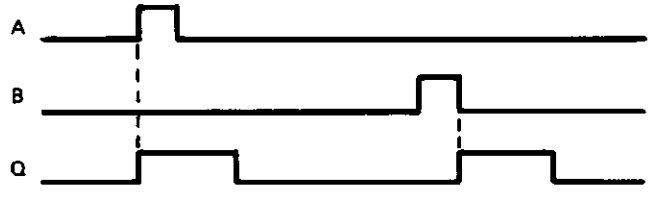
C_D (RESET) TERMINAL, WHEN SWITCHED TO LOGIC 0, IMMEDIATELY TERMINATES OUTPUT PULSE.



V_{DD} = PIN 16

V_{SS} = PIN 8

R_X AND C_X ARE EXTERNAL COMPONENTS.



TP5-2299-011

Dual Monostable Multivibrator CD4098BE
Figure 3

Table 1. Parallel Input, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	**Note** These testing and troubleshooting procedures are based on using a control unit and an associated local unit. The most effective method of testing and troubleshooting is obtained by installing the questionable parallel input in the control unit. During these tests when a control unit is referred to it is a receiver-exciter control, an exciter control, or a receiver control. When a local unit is referred to it is a receiver-exciter, an exciter, or a receiver.		
	a. Remove top cover of unit containing parallel input to be tested.		
	b. Remove parallel input. Install it on an extender card and place it in the control unit.		
	c. Set control unit and local unit LINE SELECTOR switches to 115 V.		
	d. Connect control unit and local unit to 115-V ac power source and set power on.		
	e. Measure dc voltages, on the card under test, between the following pins and ground (TP1, brown):		
	P1-45	+15 ±1.0 V dc.	
	P1-65	+5 ±0.5 V dc.	
	P1-114	-15 ±1.0 V dc.	
	f. Strap local unit for address 0.		
	g. Connect local unit to control unit.		
2. Word and address gates	a. Connect oscilloscope to TP2 (red).		
	b. Set control unit KEY switch to LOCK and note oscilloscope.	A logic level 1, 100-μs (nominal) pulse.	Check U2A, U2B, and associated circuit.
	c. Set control unit KEY switch to NORM and note oscilloscope.	Same as step b.	Same as step b.
	d. Connect oscilloscope to TP3 (orange).		
	e. Set control unit PA PWR switch to STBY and note oscilloscope.	A logic level 1, 100-μs (nominal) pulse.	Check U3A, U3B, and associated circuit.
	f. Set control unit PA PWR switch to OFF and note oscilloscope.	Same as step e.	Same as step e.
(Cont)	g. Connect oscilloscope to TP4 (yellow).		

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. Word and address gates (Cont)	h. Rotate each control unit FREQUENCY KHZ thumb wheel and note oscilloscope when changing positions.	A logic level 1, 100-μs (nominal) pulse.	Check U1A, U1B, and associated circuit.
	i. Connect oscilloscope to TP5 (green).		
	j. Set control unit MODE switch to each mode position and note oscilloscope when changing positions.	A logic level 1, 100-μs (nominal) pulse.	Check U5A, U5B, and associated circuit.
	k. Connect oscilloscope to P1-88.		
	l. Rotate control unit ADDRESS switch and note oscilloscope when changing positions.	A logic level 1, 100-μs (nominal) pulse.	Check U4A, U4B, and associated circuit.
	m. Connect +5-V dc input to P1-66.		
	n. Check voltage levels at:		
	TP2	NLT +4.0 V dc.	Check CR1.
	TP3	NLT +4.0 V dc.	Check CR2.
	TP4	NLT +4.0 V dc.	Check CR4.
	TP5	NLT +4.0 V dc.	Check CR3.
	o. Remove +5 V dc from P1-66.		

Note

Tests 3 through 18 are output tests. During all of these tests serial interface card A13 is removed from unit under test and mux inputs are strapped according to word and character being tested. To strap a logic 1 input, connect a 4700-Ω resistor in series between the mux input pin and +5 V dc. To strap a logic 0 input, connect directly from the mux input pin to ground. See following chart and figure for mux input/output strapping and setup requirements. Where front-panel controls are shown, these controls may be used to apply the appropriate inputs. If they are not used their associated front-panel connector must be disconnected.

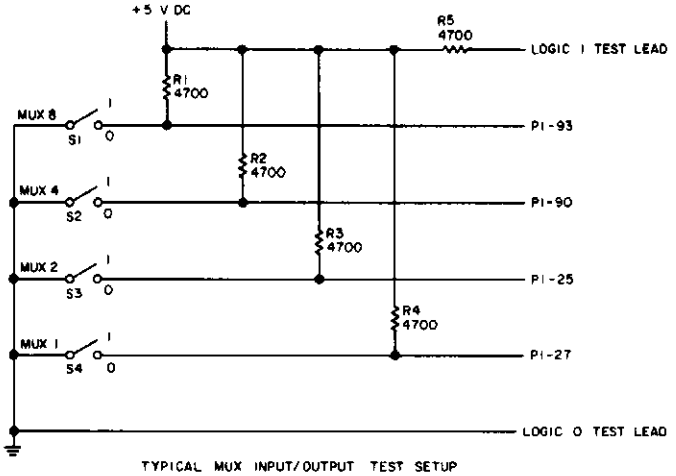
MUX CONTROL LINES INPUT STRAPPING				*OUTPUTS PRESENTED BY PARALLEL INPUT CARD									
				WORD NO	CHARACTER NO	OUTPUT BIT NO							
MX8	MX4	MX2	MX1			1	2	3	4	5	6	7	8
P1-93	P1-90	P1-25	P1-27			P1-26	P1-28	P1-29	P1-94	P1-30	P1-31	P1-96	P1-104
0	0	0	0	1	2	P1-62	P1-127	P1-63	P1-128	P1-64	P1-129	P1-38	P1-103
0	0	0	1	1	3	P1-58	P1-123	P1-59	P1-124	P1-60	P1-125	P1-61	P1-126
0	0	1	0	1	4	P1-54	P1-119	P1-55	P1-120	P1-56	P1-121	P1-57	P1-122
0	0	1	1	1	5	P1-50	P1-115	P1-51	P1-116	P1-52	P1-117	P1-53	P1-118
0	1	0	0	2	2	P1-87	P1-10	P1-75	P1-11	P1-76	NA	NA	NA
0	1	0	1	2	3	P1-20	P1-19	P1-85	P1-84	P1-37	P1-106	P1-41	NA

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL

MUX CONTROL LINES INPUT STRAPPING				*OUTPUTS PRESENTED BY PARALLEL INPUT CARD									
				WORD NO	CHARACTER NO	OUTPUT BIT NO							
MX8	MX4	MX2	MX1			1	2	3	4	5	6	7	8
P1-93	P1-90	P1-25	P1-27			P1-26	P1-28	P1-29	P1-94	P1-30	P1-31	P1-96	P1-104
0	1	1	0	2	4	P1-32	P1-97	P1-33	P1-98	P1-34	P1-35	P1-99	P1-100
0	1	1	1	2	5	P1-21	P1-91	P1-92	P1-74	P1-9	P1-72	P1-8	P1-73
1	0	0	0	3	2	P1-112	P1-47	P1-113	P1-48	P1-107	NA	NA	NA
1	0	0	1	3	3	P1-42	P1-108	P1-43	P1-109	P1-44	P1-110	P1-111	P1-46
1	0	1	0	3	4	NA	NA	NA	NA	NA	NA	NA	NA
1	0	1	1	3	5	P1-79	P1-14	P1-78	P1-82	P1-81	NA	NA	NA
1	1	0	0	4	2	NA	NA	NA	NA	P1-68	NA	NA	NA
1	1	0	1	4	3	P1-18	P1-101	P1-39	P1-83	P1-36	P1-105	P1-40	P1-2
1	1	1	0	4	4	P1-3	P1-86	P1-49	P1-67	P1-70	P1-5	P1-4	P1-69
1	1	1	1	4	5	P1-80	P1-16	P1-95	P1-71	NA	NA	NA	NA

*Outputs presented at the bit no pins are the inputs at the bit no pins associated with the word no/character no.



TYPICAL MUX INPUT/OUTPUT TEST SETUP

TP5-4247-013

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. Word 1, character 2 outputs	a. Strap mux control lines for word 1, character 2.		
	b. Apply logic 1 inputs at inputs associated with word 1, character 2 (see chart).	Verify that associated outputs are at logic 1.	
	Note FREQUENCY KHZ switches apply logic 1 inputs in the positions indicated in the chart. In the 0 position these switches apply logic 0 inputs.		
	c. Apply logic 0 inputs at inputs associated with word 1, character 2 (see chart).	Verify that associated outputs are at logic 0.	

FRONT-PANEL CONTROL		BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
1 MHz	1	1	62	26	U25, U18
	2	2	127	28	U15, U19
	4	3	63	29	U23, U20
	8	4	128	94	U21, U17
10 MHz	1	5	64	30	U24, U11
	2	6	129	31	U16, U13
NA		7	38	96	U22, U12
NA		8	103	104	U14, R42, U9

4. Word 1, character 3 outputs	a. Strap mux control lines for word 1, character 3.		
	b. Apply logic 1 inputs at inputs associated with word 1, character 3 (see chart).	Verify that associated outputs are at logic 1.	
	Note FREQUENCY KHZ switches apply logic 1 inputs in the positions indicated in the chart. In the 0 position, these switches apply logic 0 inputs.		
(Cont)	c. Apply logic 0 inputs at inputs associated with word 1, character 3 (see chart).	Verify that associated outputs are at logic 0.	

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. Word 1, character 3 outputs (Cont)			

FRONT-PANEL CONTROL		BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
10 kHz	1	1	58	26	U25, U18
	2	2	123	28	U15, U19
	4	3	59	29	U23, U20
	8	4	124	94	U21, U17
100 kHz	1	5	60	30	U24, U11
	2	6	125	31	U16, U13
	4	7	61	96	U22, U12
	8	8	126	104	U14, U9

5. Word 1, character 4 outputs	a. Strap mux control lines for word 1, character 4.		
	b. Apply logic 1 inputs at inputs associated with word 1, character 4 (see chart).	Verify that associated outputs are at logic 1.	
	Note FREQUENCY KHZ switches apply logic 1 inputs in the positions indicated in the chart. In the 0 position, these switches apply logic 0 inputs.		
	c. Apply logic 0 inputs at inputs associated with word 1, character 4 (see chart).	Verify that associated outputs are at logic 0.	

FRONT-PANEL CONTROL		BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
100 Hz	1	1	54	26	U25, U18
	2	2	119	28	U15, U19
	4	3	55	29	U23, U20
	8	4	120	94	U21, U17
1 kHz	1	5	56	30	U24, U11
	2	6	121	31	U16, U13
	4	7	57	96	U22, U12
	8	8	122	104	U14, U9

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
6. Word 1, character 5 outputs	a. Strap mux control lines for word 1, character 5.		
	b. Apply logic 1 inputs at inputs associated with word 1, character 5 (see chart). **Note** FREQUENCY KHZ switches apply logic 1 inputs in the positions indicated in the chart. In the 0 position, these switches apply logic 0 inputs.	Verify that associated outputs are at logic 1.	
	c. Apply logic 0 inputs at inputs associated with word 1, character 5 (see chart).	Verify that associated outputs are at logic 0.	

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	50	26	U25, R68, U18
NA	2	115	28	U15, R64, U19
NA	3	51	29	U23, R60, U20
NA	4	116	94	U21, R56, U17
*10 Hz 1	5	52	30	U24, R52, U11
*10 Hz 2	6	117	31	U16, R49, U13
*10 Hz 4	7	53	96	U22, R46, U12
*10 Hz 8	8	118	104	U14, R43, U9

*Applicable only with 10-Hz front-panel tuning.

7. Word 2, character 2 outputs	a. Strap mux control lines for word 2, character 2.	**Note** Grounded input as noted in chart will always be logic 0 output.	
(Cont)	b. Apply logic 1 inputs at inputs associated with word 2, character 2 (see chart).	Verify that associated outputs are at logic 1.	

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
7. Word 2, character 2 outputs (Cont)	**Note** RF GAIN switch applies logic 1 input in the position indicated in the chart (positions read as MAX minus X number of positions). In the MAX position, this switch applies logic 0 inputs.		
	c. Apply logic 0 inputs at inputs associated with word 2, character 2 (see chart).	Verify that associated outputs are at logic 0.	

FRONT-PANEL CONTROL		BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA		1	87	26	U25, R69, U18
RF GAIN	MAX-1	2	10	28	U15, R65, U19
	MAX-2	3	75	29	U23, R61, U20
	MAX-4	4	11	94	U21, R57, U17
	MAX-8	5	76	30	U24, R53, U11
NA		6	*	31	U16, U13
NA		7	38	96	U22, U12
NA		8	103	104	U14, R42, U9

*Grounded input.

8. Word 2, character 3 outputs	a. Strap mux control lines for word 2, character 3.	**Note** Grounded input as noted in chart will always be logic 0 output.	
	b. Apply logic 1 inputs at inputs associated with word 2, character 3 (see chart).	Verify that associated ouputs are at logic 1.	
	Note AGC switch applies logic 1 input in the position indicated in the chart. In the AGC-SLOW position, this switch applies logic 0 inputs.		
(Cont)	c. Apply logic 0 inputs at inputs associated with word 2, character 3 (see chart).	Verify that associated outputs are at logic 0.	

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
8. Word 2, character 3 outputs (Cont)			

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
AGC-FAST (B)	1	20	26	U25, U18
AGC-OFF (B)	2	19	28	U15, U19
AGC-FAST (A)	3	85	29	U23, U20
AGC-OFF (A)	4	84	94	U21, U17
NA	5	37	30	U24, U11
NA	6	106	31	U16, U13
NA	7	41	96	U22, U12
NA	8	*	104	U14, U9

*Grounded input.

9. Word 2, character 4 outputs	a. Strap mux control lines for word 2, character 4.		
	b. Apply logic 1 inputs at inputs associated with word 2, character 4 (see chart).	Verify that associated outputs are at logic 1.	
	Note MODE switch and/or BANDWIDTH switch applies logic 1 input in the position indicated in the chart. In the ISB position, the MODE switch applies logic 0 inputs.		
	c. Apply logic 0 inputs at inputs associated with word 2, character 4 (see chart).	Verify that associated outputs are at logic 0.	

FRONT-PANEL CONTROL (MODE)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
SSB/CW-USB or USB	1	32	26	U25, R70, U18
SSB/CW-LSB or LSB	2	97	28	U15, R66, U19
*SSB/CW-A	3	33	29	U23, R62, U20
*SSB/CW-B	4	98	94	U21, R58, U17
*SSB/CW-C	5	34	30	U24, R54, U11
*SSB/CW-D	6	35	31	U16, R50, U13
*SSB/CW-E	7	99	96	U22, R47, U12
*SSB/CW-16	8	100	104	U14, R44, U9

*SSB/CW applicable only on receiver control.

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
10. Word 2, character 5 outputs	a. Strap mux control lines for word 2, character 5.		
	b. Apply logic 1 inputs at inputs associated with word 2, character 5 (see chart).	Verify that associated outputs are at logic 1.	
	Note MODE switch applies logic 1 input in the position indicated in the chart. In any other position, the MODE switch applies logic 0 input.		
	c. Apply logic 0 inputs at inputs associated with word 2, character 5 (see chart).	Verify that associated outputs are at logic 0.	

FRONT-PANEL CONTROL (MODE)	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	21	26	U25, R71, U18
NA	2	91	28	U15, R67, U19
NA	3	92	29	U23, R63, U20
ISB	4	74	94	U21, R59, U17
*CW	5	9	30	U24, R55, U11
CW, LSB, USB, ISB, or SSB/CW	6	72	31	U16, R51, U13
AM	7	8	96	U22, R48, U12
NA	8	73	104	U14, R45, U9

*CW applicable only on exciter control and receiver-exciter control.

11. Word 3, character 2 outputs	a. Strap mux control lines for word 3, character 2.	**Note** Grounded input as noted in chart will always be logic 0 output.	
	b. Apply logic 1 inputs at inputs associated with word 3, character 2 (see chart).	Verify that associated outputs are at logic 1.	
(Cont)	c. Apply logic 0 inputs at inputs associated with word 3, character 2 (see chart).	Verify that associated outputs are at logic 0.	

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
11. Word 3, character 2 outputs (Cont)			

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	112	26	U18, R103, U25
NA	2	47	28	U19, R97, R15
NA	3	113	29	U20, R91, U23
NA	4	48	94	U17, R86, U21
NA	5	107	30	U11, R81, U24
NA	6	*	31	U13, U16
NA	7	38	96	U12, U22
NA	8	103	104	U9, R42, U14

*Grounded input.

12. Word 3, character 3 outputs	a. Strap mux control lines for word 3, character 3.		
	b. Apply logic 1 inputs at inputs associated with word 3, character 3 (see chart).	Verify that associated outputs are at logic 1.	
	c. Apply logic 0 inputs at inputs associated with word 3, character 3 (see chart).	Verify that associated outputs are at logic 0.	

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	42	26	U18, R104, U25
NA	2	108	28	U19, R98, U15
NA	3	43	29	U20, R92, U23
NA	4	109	94	U17, R87, U21
NA	5	44	30	U11, R82, U24
NA	6	110	31	U13, R78, U16
NA	7	111	96	U12, R75, U22
NA	8	46	104	U9, R72, U14

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
13. Word 3, character 4 outputs	a. Strap mux control lines for word 3, character 4.	**Note** Grounded input as noted in chart will always be logic 0 output. Verify that all associated outputs are at logic 0.	

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	*	26	U18, U25
NA	2	*	28	U19, U15
NA	3	*	29	U20, U23
NA	4	*	94	U17, U21
NA	5	*	30	U11, U24
NA	6	*	31	U13, U16
NA	7	*	96	U12, U22
NA	8	*	104	U9, U14

*Grounded input.

14. Word 3, character 5 outputs	a. Strap mux control lines for word 3, character 5.	**Note** Grounded input as noted in chart will always be logic 0 output.	
	b. Apply logic 1 inputs at inputs associated with word 3, character 5 (see chart). **Note** PA PWR and P CAR switches apply logic 1 inputs in the positions indicated in the chart. In the OFF positions these switches apply logic 0 inputs.	Verify that associated outputs are at logic 1.	
(Cont)	c. Apply logic 0 inputs at inputs associated with word 3, character 5 (see chart).	Verify that associated outputs are at logic 0.	

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
14. Word 3, character 5 outputs (Cont)			

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
PA PWR-STBY	1	79	26	U18, R105, U25
PA PWR-HIGH PWR	2	14	28	U19, R99, U15
PA PWR-LOW PWR	3	78	29	U20, R93, U23
P CAR-ON	4	82	94	U17, R8, U21
NA	5	81	30	U11, R83, U24
NA	6	*	31	U13, U16
NA	7	*	96	U12, U22
NA	8	*	104	U9, U14

*Grounded input.

15. Word 4, character 2 outputs	a. Strap mux control lines for word 4, character 2.	**Note** Grounded input as noted in chart will always be logic 0 output.	
	b. Apply logic 1 inputs at inputs associated with word 4, character 2 (see chart). **Note** KEY switch in the LOCK position applies a logic 1 input and in the NORM position applies a logic 0 input.	Verify that associated outputs are at logic 1.	
(Cont)	c. Apply logic 0 inputs at inputs associated with word 4, character 2 (see chart).	Verify that associated outputs are at logic 0.	

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
15. Word 4, character 2 outputs (Cont)			

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	*	26	U18, U25
NA	2	*	28	U19, U15
NA	3	*	29	U20, U23
NA	4	*	94	U17, U21
KEY-LOCK	5	68	30	U11, R12, U24
NA	6	*	31	U13, U16
NA	7	38	96	U12, U22
NA	8	103	104	U9, R42, U14

*Grounded input.

16. Word 4, character 3 outputs	a. Strap mux control lines for word 4, character 3.		
	b. Apply logic 1 inputs at inputs associated with word 4, character 3 (see chart).	Verify that associated outputs are at logic 1.	
	c. Apply logic 0 inputs at inputs associated with word 4, character 3 (see chart).	Verify that associated outputs are at logic 0.	

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	18	26	U18, R106, U25
NA	2	101	28	U19, R100, U15
NA	3	39	29	U20, R94, U23
NA	4	83	94	U17, R88, U21
NA	5	36	30	U11, R84, U24
NA	6	105	31	U13, R79, U16
NA	7	40	96	U12, R76, U22
NA	8	2	104	U9, R73, U14

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
17. Word 4, character 4 outputs	a. Strap mux control lines for word 4, character 4.		
	b. Apply logic 1 inputs at inputs associated with word 4, character 4 (see chart).	Verify that associated outputs are at logic 1.	
	c. Apply logic 0 inputs at inputs associated with word 4, character 4 (see chart).	Verify that associated outputs are at logic 0.	

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	3	26	U18, R107, U25
NA	2	86	28	U19, R101, U15
NA	3	49	29	U20, R95, U23
NA	4	67	94	U17, R89, U21
NA	5	70	30	U11, R85, U24
NA	6	5	31	U13, R80, U16
NA	7	4	96	U12, R77, U22
NA	8	69	104	U9, R74, U14

18. Word 4, character 5 outputs	a. Strap mux control lines for word 4, character 5.	*Note* Grounded input as noted in chart will always be logic 0 output.	
	b. Apply logic 1 inputs at inputs associated with word 4, character 5 (see chart).	Verify that associated outputs are at logic 1.	
(Cont)	c. Apply logic 0 inputs at inputs associated with word 4, character 5 (see chart).	Verify that associated outputs are at logic 0.	

Table 1. Parallel Input, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
18. Word 4, character 5 outputs (Cont)			

FRONT-PANEL CONTROL	BIT NO	INPUTS P1-( )	OUTPUTS P1-( )	IF ABNORMAL CHECK
NA	1	80	26	U18, R108, U25
NA	2	16	28	U19, R102, CR24, C28, U15
NA	3	95	29	U20, R96, U23
NA	4	71	94	U17, R90, U21
NA	5	*	30	U11, U24
NA	6	*	31	U13, U16
NA	7	*	96	U12, U22
NA	8	*	104	U9, U14

*Grounded input.

4. REPAIR

Repair of the parallel input card is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

5. PARTS LIST/DIAGRAMS

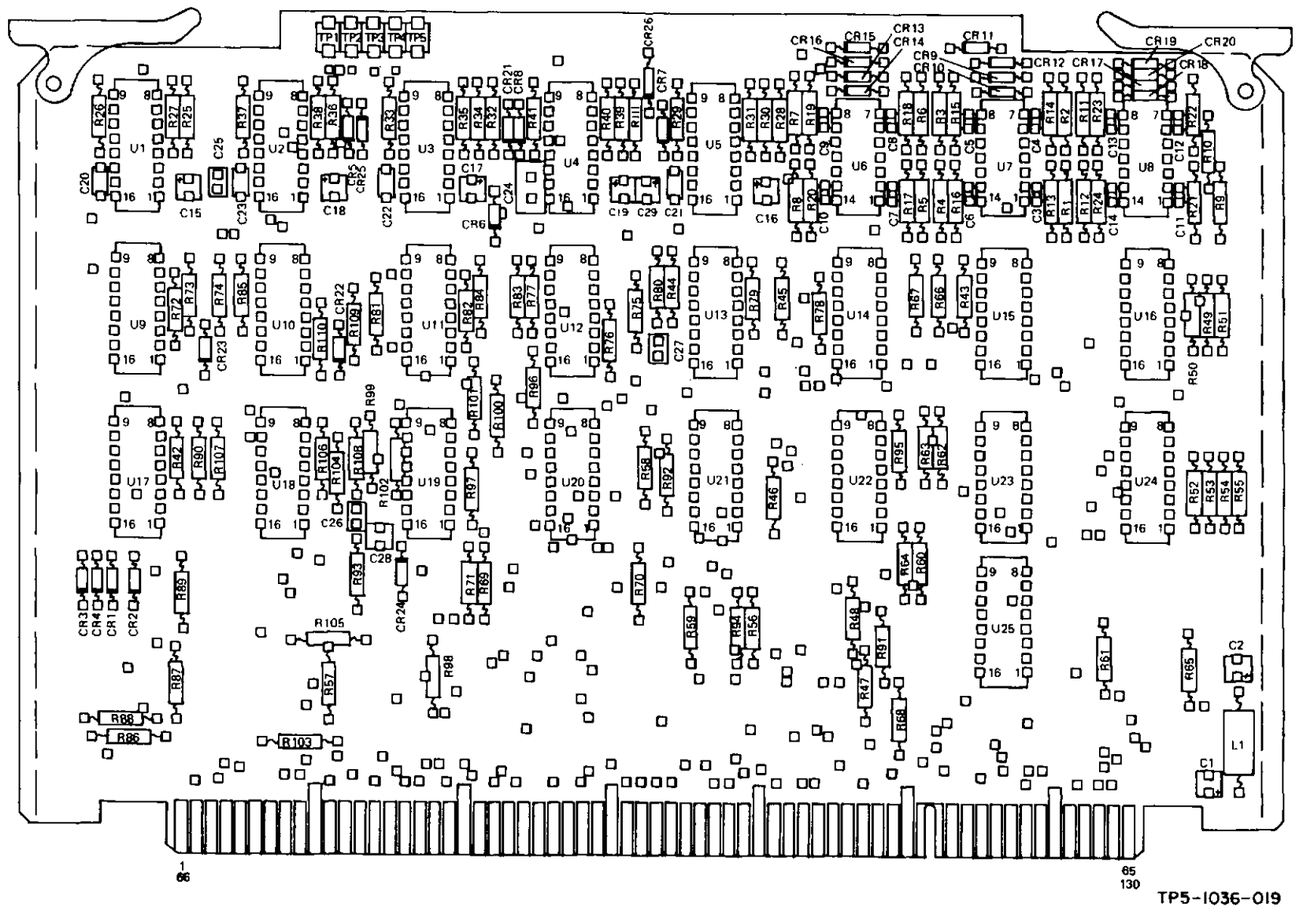
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram, figure 4. The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points to the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Parallel input	635-0751-001	REV N
Parallel input	635-0751-002	REV M



Parallel Input, Schematic Diagram
Figure 4 (Sheet 1 of 8)

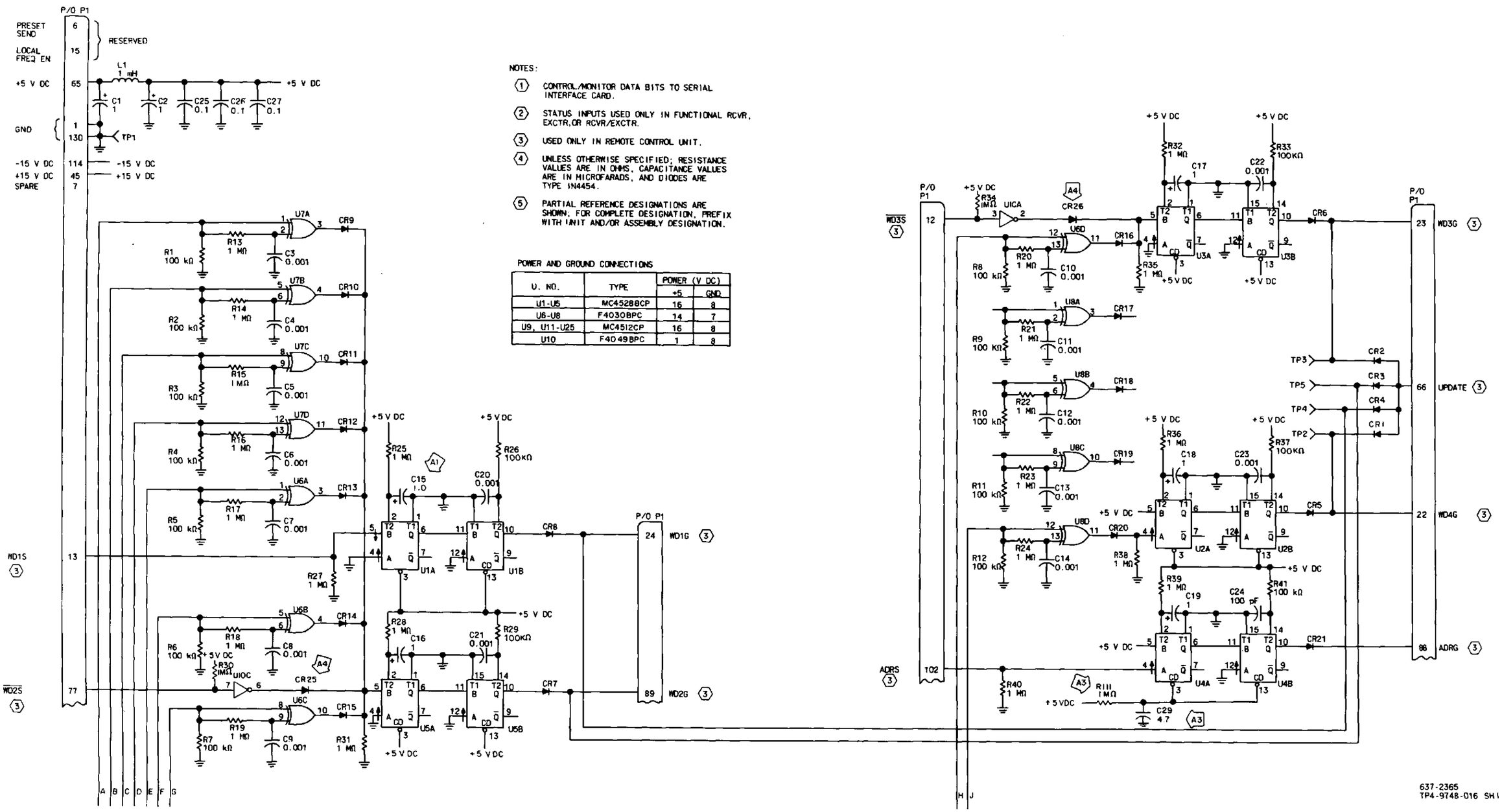
PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	PARALLEL INPUT 635-0751-001		A
	PARALLEL INPUT 635-0751-002		B
CR1-CR24	SEMICOND DEVICE, 1N4454	353-3644-010	
CR25, CR26	SEMICOND DEVICE, 1N4454 (A4)	353-3644-010	A
C1, C2	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	
C3-C14	CAPACITOR, FXD, CER DIEL, 1000pF, 20%, 50V	913-3279-030	
C15	CAPACITOR, FXD, ELCTLT, 4.7μF, 20%, 35V (A1)	184-9102-390	A
C15	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	A
C15	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	B
C16-C19	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	
C20-C23	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C24	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 500V	912-3879-000	
C25-C27	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-680	
C28	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V (A2)	184-9102-350	A
C28	CAPACITOR, FXD, ELCTLT, 4.7μF, 20%, 35V	184-9102-390	A
C28	CAPACITOR, FXD, ELCTLT, 4.7μF, 20%, 35V	184-9102-390	B
C29	CAPACITOR, FXD, ELCTLT, 4.7μF, 20%, 35V (A3)	184-9102-390	A
C29	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-390	B
L1	COIL, RF, 1000μH	240-2540-000	
R1-R12	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R13-R25	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R26	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R27, R28	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R29	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R30-R32	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R33	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R34-R36	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R37	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R38-R40	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R41	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R42-R108	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R109	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R110	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R111	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W (A3)	745-0857-000	A
R111	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	B
TP1	JACK, TIP, BRN	360-0484-070	
TP2	JACK, TIP, RED	360-0484-020	
TP3	JACK, TIP, ORN	360-0484-050	
TP4	JACK, TIP, YEL	360-0484-060	
TP5	JACK, TIP, GRN	360-0484-040	
U1-U5	INTEGRATED CKT, MC14528BCP	351-8421-020	
U6-U8	INTEGRATED CKT, F4030BPC	351-8159-190	
U9	INTEGRATED CKT, MC14512CP	351-8420-020	
U10	INTEGRATED CKT, F4049BPC	351-8159-210	
U11-U25	INTEGRATED CKT, MC14512CP	351-8420-020	

MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Changed C15 from 4.7μF to 1.0μF.	REV C and above
A2	Changed C28 from 1.0μF to 4.7μF.	REV D and above
A3	Added R111, 1MΩ and C29, 4.7μF.	REV E and above
	Note	
	The preceding modification history effectivities apply only to the 635-0751-001. Preceding modifications are included in all 635-0751-002 cards.	
A4	Added CR25, 1N4454 and CR26, 1N4454.	635-0751-001, REV K and above

Parallel Input, Schematic Diagram
Figure 4 (Sheet 2)



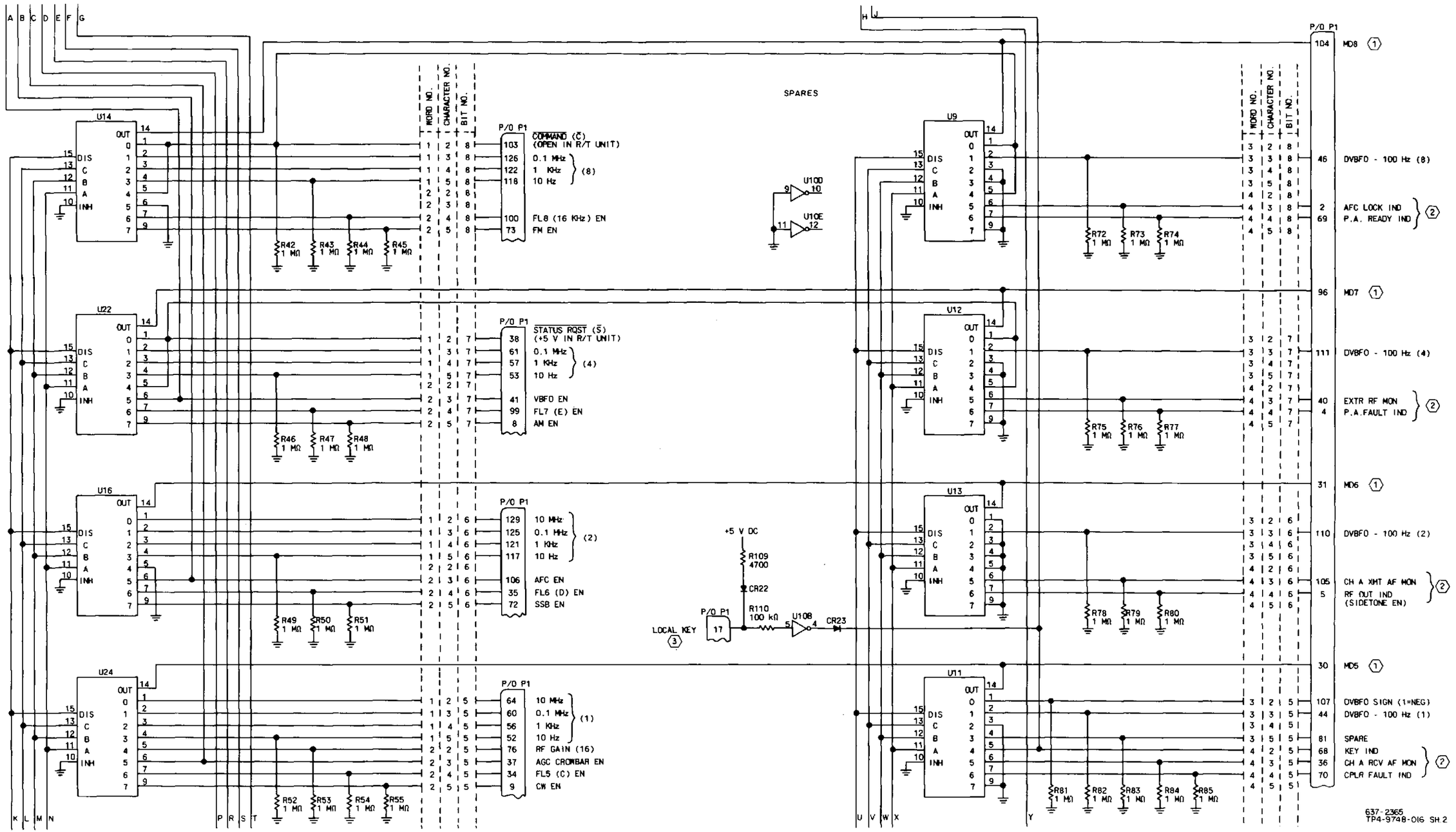
NOTES:

1. CONTROL/MONITOR DATA BITS TO SERIAL INTERFACE CARD.
2. STATUS INPUTS USED ONLY IN FUNCTIONAL RCVR, EXCTR,OR RCVR/EXCTR.
3. USED ONLY IN REMOTE CONTROL UNIT.
4. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, AND DIODES ARE TYPE 1N4454.
5. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.

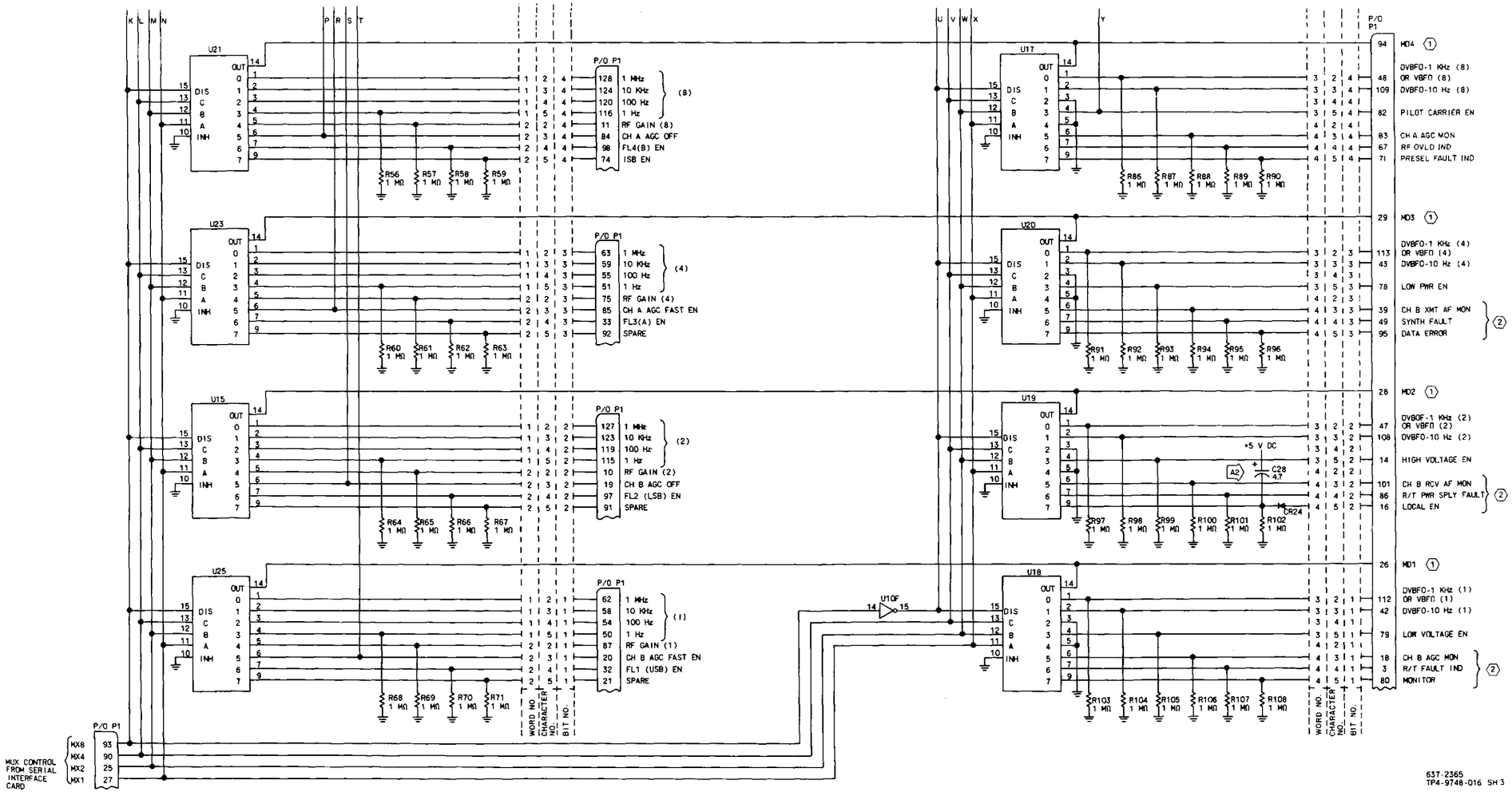
POWER AND GROUND CONNECTIONS

U. NO.	TYPE	POWER (V DC)	
		+5	GND
U1-U5	MC4528BCP	16	8
U6-U8	F4030BPC	14	7
U9, U11-U25	MC4512CP	16	8
U10	F4049BPC	1	8

Parallel Input (635-0751-001), Schematic Diagram
Figure 4 (Sheet 3)



Parallel Input (635-0751-001), Schematic Diagram
Figure 4 (Sheet 4)

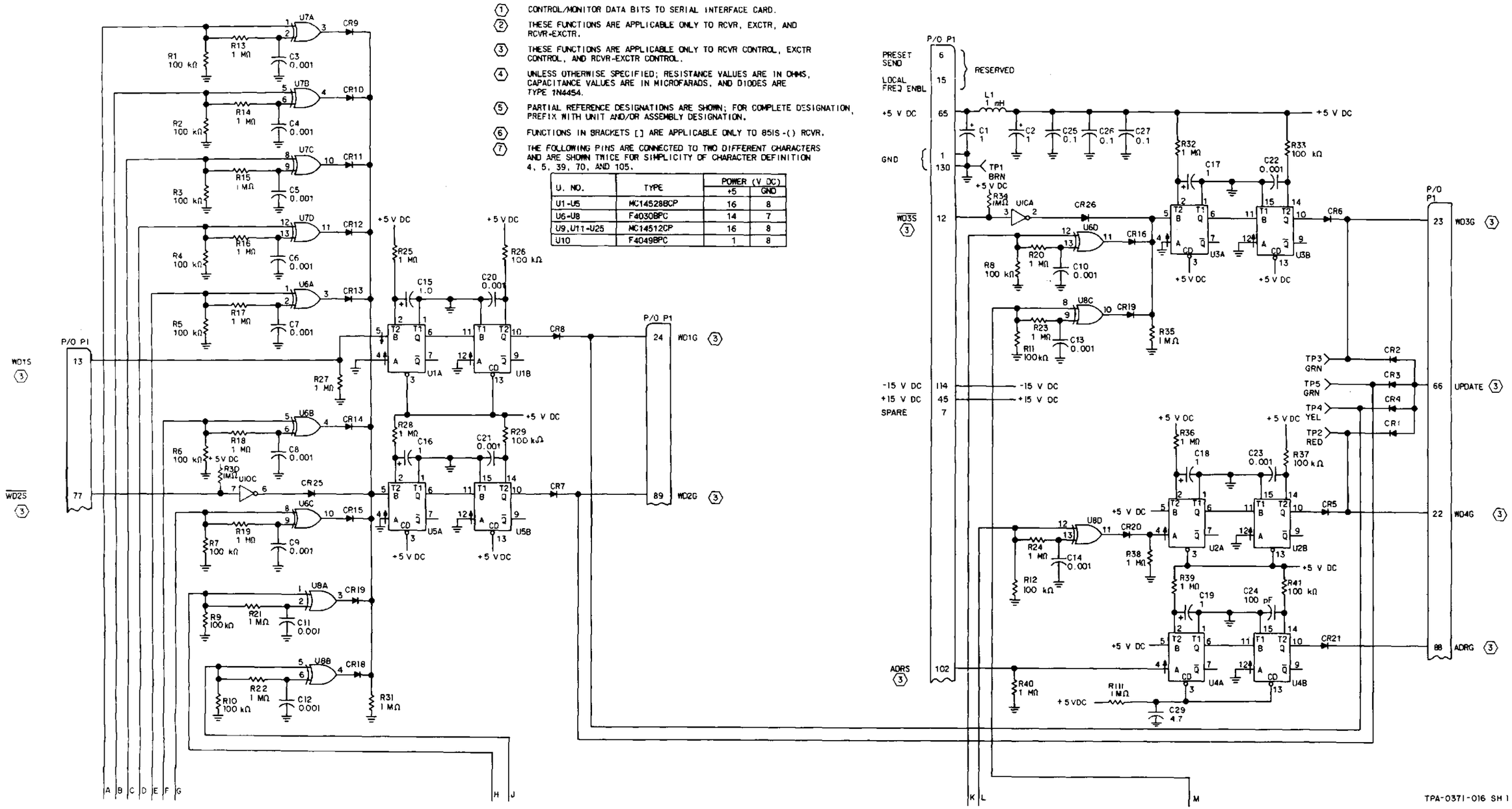


Parallel Input (635-0751-001), Schematic Diagram
Figure 4 (Sheet 5)

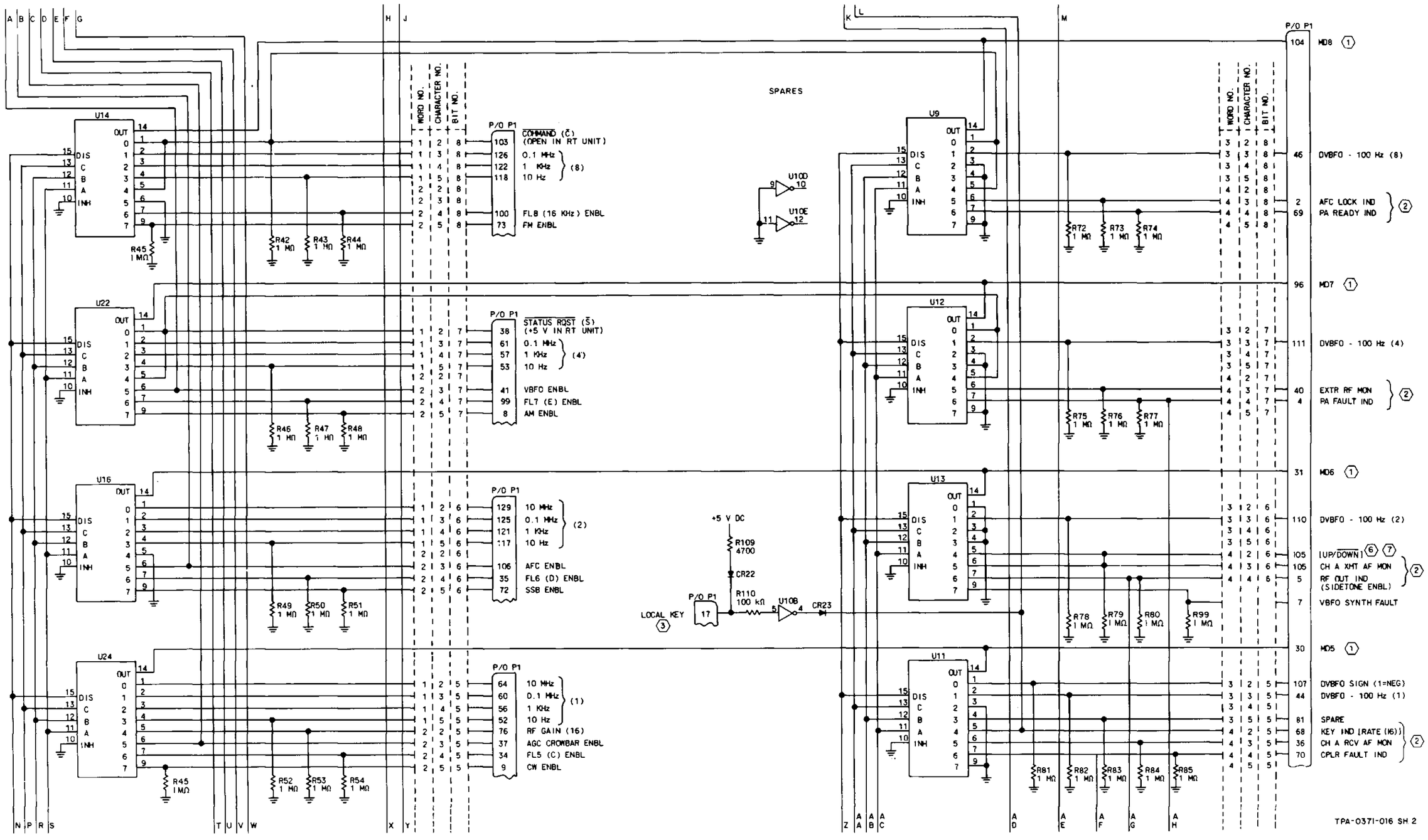
NOTES:

1. CONTROL/MONITOR DATA BITS TO SERIAL INTERFACE CARD.
2. THESE FUNCTIONS ARE APPLICABLE ONLY TO RCVR, EXCTR, AND RCVR-EXCTR.
3. THESE FUNCTIONS ARE APPLICABLE ONLY TO RCVR CONTROL, EXCTR CONTROL, AND RCVR-EXCTR CONTROL.
4. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, AND DIODES ARE TYPE 1N4454.
5. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
6. FUNCTIONS IN BRACKETS [] ARE APPLICABLE ONLY TO 851S-() RCVR.
7. THE FOLLOWING PINS ARE CONNECTED TO TWO DIFFERENT CHARACTERS AND ARE SHOWN TWICE FOR SIMPLICITY OF CHARACTER DEFINITION 4, 5, 39, 70, AND 105.

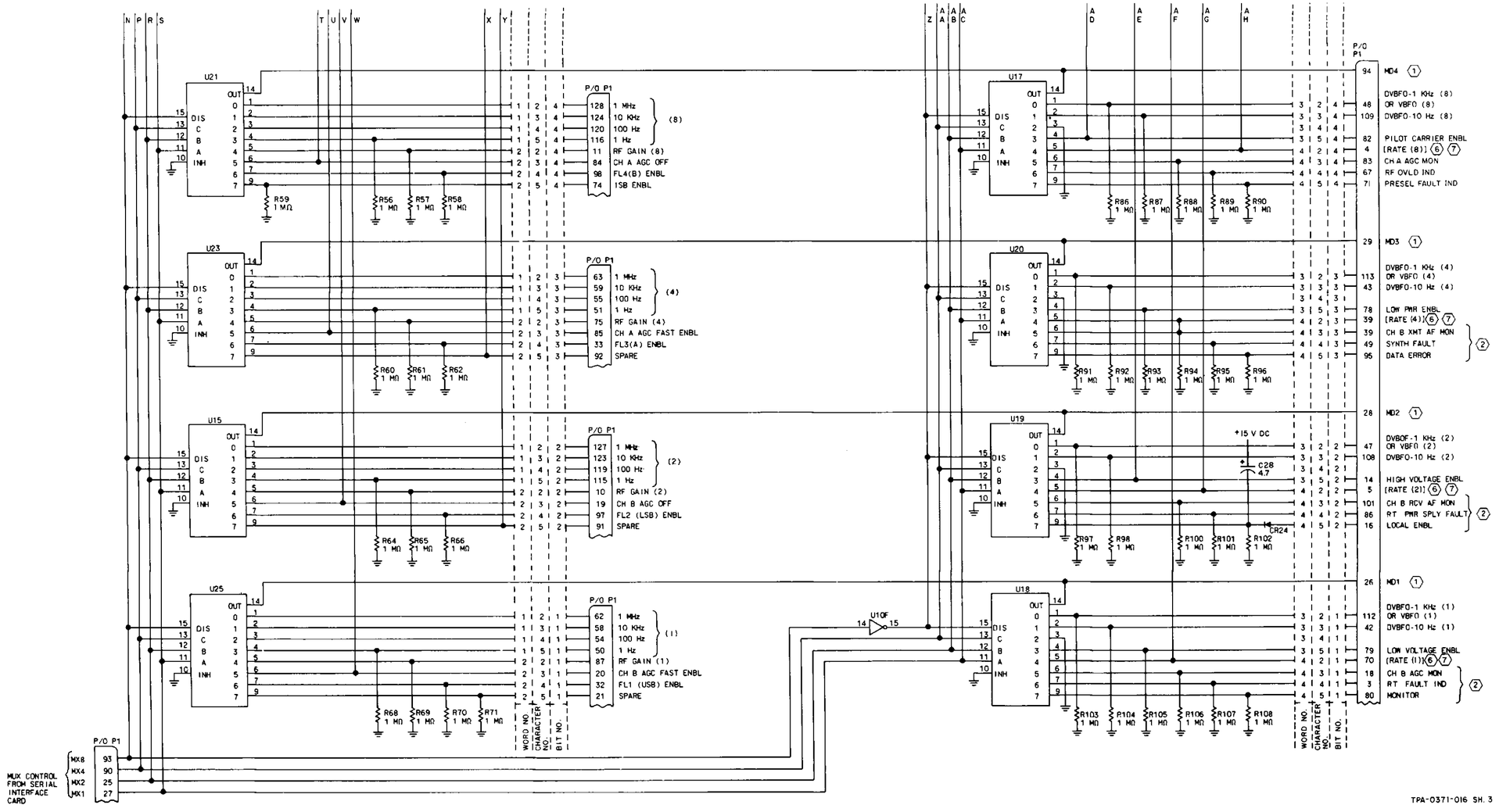
U. NO.	TYPE	POWER (V DC)	
		+5	GND
U1-U5	MC14528BCP	16	8
U6-U8	F4030BPC	14	7
U9,U11-U25	MC14512CP	16	8
U10	F4049BPC	1	8



Parallel Input (635-0751-002), Schematic Diagram
Figure 4 (Sheet 6)



Parallel Input (635-0751-002), Schematic Diagram
Figure 4 (Sheet 7)



Parallel Input (635-0751-002), Schematic Diagram
Figure 4 (Sheet 8)

Parallel Output (635-0752-001, -002)

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

523-0767950-002211
2nd Edition, 1 June 1978

1. DESCRIPTION

Parallel Output 635-0752-001, -002, shown in figure 1, is a 2-layer planar card with a 130-pin (2 layers, 65 pins each) edge-on connector. All test points are mounted at the top edge of the card for easy access with the card installed in the unit.

2. PRINCIPLES OF OPERATION

2.1 General

The parallel output card consists of 6 primary circuits: 16 shift registers used as multiplexers, 4 power-on-clear flip-flops, a strobe generator, an rf gain control, a fault indicator flasher, and an update/busy indicator/address gate (ADRG) generator. The multiplexers receive serial data and convert it to parallel outputs for application to front panel indicators. The rf gain control circuits are used only in the remote mode of the receiver circuits. A series of gates and flip-flops generates update, address gate, and busy indicator signals for use by control unit circuits. Outputs from the power-on-clear flip-flops momentarily set all the multiplexers to a no-output condition when power is initially applied to the circuits. A timing circuit develops a flashing signal for the R/E FAULT indicator under certain conditions.

2.2 Power-On-Clear

When power is applied to the parallel output card, capacitor C15 begins charging, through R28, to +5 volts. (Refer to the schematic diagram, figure 7.) Initial current through R28 develops a logic 1 voltage for approximately 1 second. When capacitor C15 is charged, no current flows through R28 and the voltage across R28 is logic 0. This momentary logic 1

TP5-2313-017

Parallel Output
Figure 1

NOTICE: This section replaces first edition dated 1 June 1977.

is applied to the set terminals of flip-flops U5A and B, and U17A and B. The flip-flop $\overline{Q}$ outputs at logic 0 with set state are applied to the enable lines of the 16 shift register multiplexers. This clears all the multiplexer outputs to an initial open-circuit condition.

2.3 Serial-to-Parallel Register

The 16 shift registers are electronically arranged in 4 groups of 4. Each group of shift registers represents one word, each shift register represents one character of the word, and each register output represents one of the eight data bits of the word. (This information is shown in detail in the columns to the right of the shift registers in the schematic diagram, figure 7.)

When the local enable (LOCAL EN) signal at P1-16 is logic 1, the enable (EN) input to all the shift registers is logic 0 which inhibits their operation. (Figure 2 shows a truth table and block diagram of the type 4094 shift register.) A logic 0, or open circuit pulled down to logic 0 by R30, at P1-16 permits the shift registers to be enabled. In this condition, the data input (P1-89) is applied to the character-5 register of each word group. The clock input (P1-88) clocks the data serially through each of the registers in a word group. When all 8 bits of characters 2 through 4 are loaded, a strobe signal at the register strobe inputs will cause the data to be stored in the registers. (Refer to the shift register block diagram in figure 2.) With the enable inputs at logic 1, the stored data is applied through buffers to the eight outputs of the shift registers. This is the parallel output signal from the circuit card.

Strobe signals to each of the word groups of registers are generated by U7. Outputs from this 8-channel multiplexer (refer to the block diagram and truth table in figure 3) are determined by the inputs to the A and B control inputs (P1-83 and -81), the strobe addresses (STA 1 and STA 2) from the serial interface card. The output signals from U7 strobe one word group of registers at a time to output the word data bits from the registers.

2.4 Fault Indicator Flasher

A type 4047 multivibrator (refer to figure 4) is connected as a retriggerable astable multivibrator to develop an on-off signal to the unit front panel R/E FAULT indicator.

During normal operation, the strobe signal to the U8 retrigger input occurs at a rate that keeps the astable multivibrator continuously triggered ($\overline{Q}$ at logic 0). This permits bit 1 of character 4, word 4 to control the output of exclusive OR gate U12B. If this character bit is logic 0, the r/t fault ind signal at P1-12 is logic 1 and the unit front panel R/E FAULT indicator is turned on. Otherwise, the output is logic 0 and the indicator is off.

In the event a malfunction interrupts monitor data transmission between the control and remote units (interconnection interruption or serial interface card malfunction, for example) the strobe signal to the U8 retrigger input goes to logic 0. This allows the multivibrator to free run at a 0.25-Hz rate (logic 1, 2s, logic 0, 2s). Regardless of the logic level at U12B-5, the r/t fault ind output will be pulsed between logic 1 and 0 to cause the R/E FAULT indicator to flash.

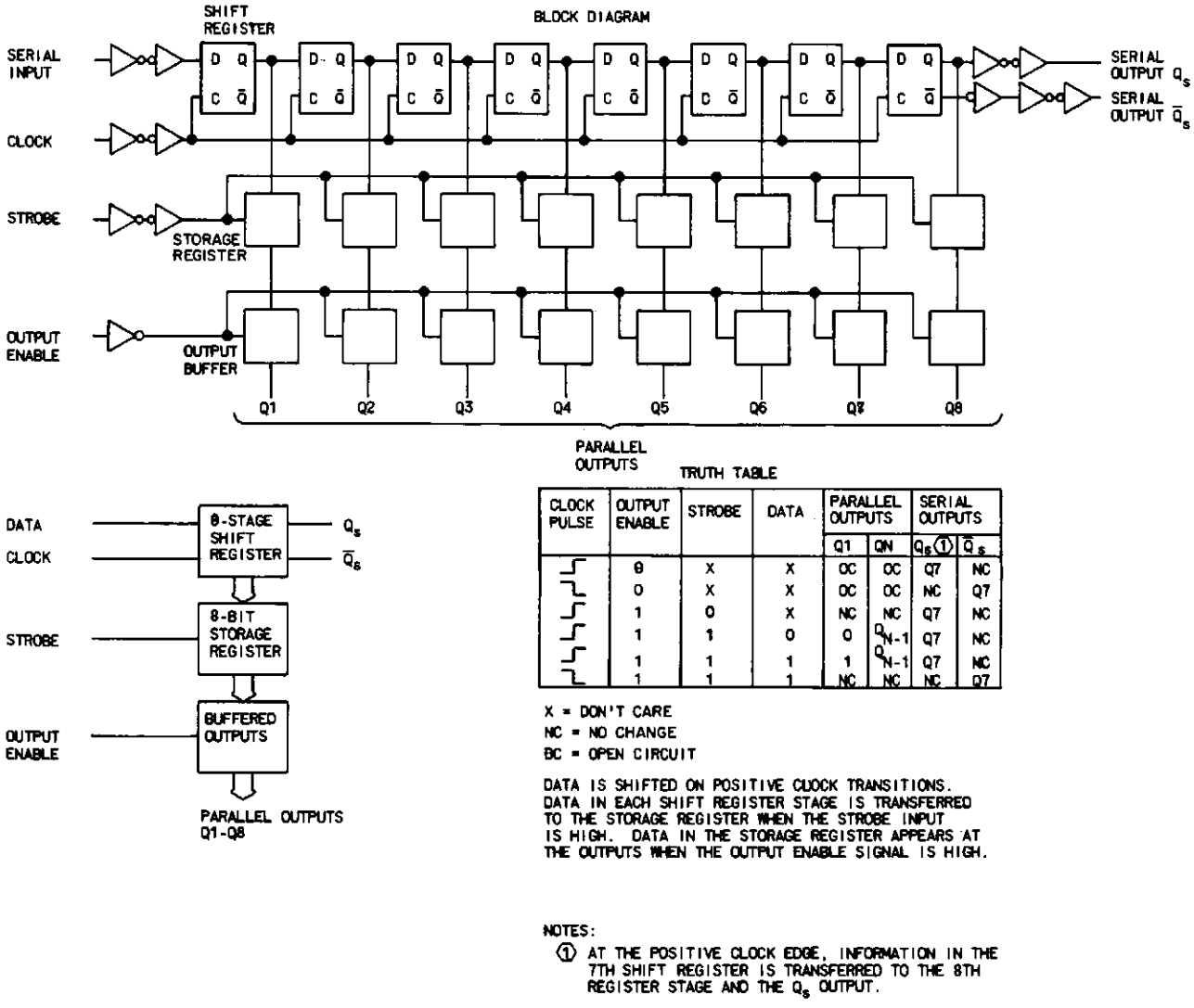
2.5 RF Gain Control

The rf gain control circuit develops a dc voltage output proportional to the binary input signals to multiplexers U2 and U10. Input signals to the multiplexers are obtained from serial-to-parallel shift register U10. The various dc output levels are developed by changing the input resistors to U1A. This is done by enabling different outputs from U10 or U2. The enabled output channel of the multiplexer is determined by the binary signals at the control inputs (pins A, B, and C). (Refer to figure 3 for a truth table and block diagram of the type 4051 multiplexer.)

When the inhibit (INH) input to the multiplexer is logic 1, the outputs are all open circuit. In local mode of operation of the remote units, the local enable input to NOR gates U9A (pin 1) and U9B (pin 5) is strapped to logic 1. This inhibits the operation of both U2 and U10 and applies approximately 0 volt to P1-86 (remote rf gain control). Otherwise, in the remote mode of operation, these inputs to U9A and B are at logic 0. The rf gain (16) signal is logic 0; this causes multiplexer U10 to be enabled and U2 to be inhibited. When the rf gain level is adjusted to the point where rf gain (16) signal goes to logic 1, U10 is inhibited and U2 is enabled (through inverter U2). Thus the various input resistor values are selected to control the dc output level from amplifiers U1A and U1B.

2.6 Update/Busy Indicator/Address Gate Generator

This circuit consists of gates U4; U12A, C, and D; U28; inverters U11A, B, and F; flip-flops U20 (truth table and diagram in figure 5); and multivibrators U3 (diagram and waveforms in figure 6). The circuit



CLOCK PULSE	OUTPUT ENABLE	STROBE	DATA	PARALLEL OUTPUTS		SERIAL OUTPUTS	
				Q1	QN	Q_s ①	$\overline{Q}_s$
↑	0	X	X	OC	OC	Q7	NC
↓	0	X	X	OC	OC	NC	Q7
↑	1	0	X	NC	NC	Q7	NC
↑	1	1	0	0	Q_{N-1}	Q7	NC
↑	1	1	1	1	Q_{N-1}	Q7	NC
↓	1	1	1	NC	NC	NC	Q7

8-Stage Shift-and-Store Bus Register CD4094BE
Figure 2

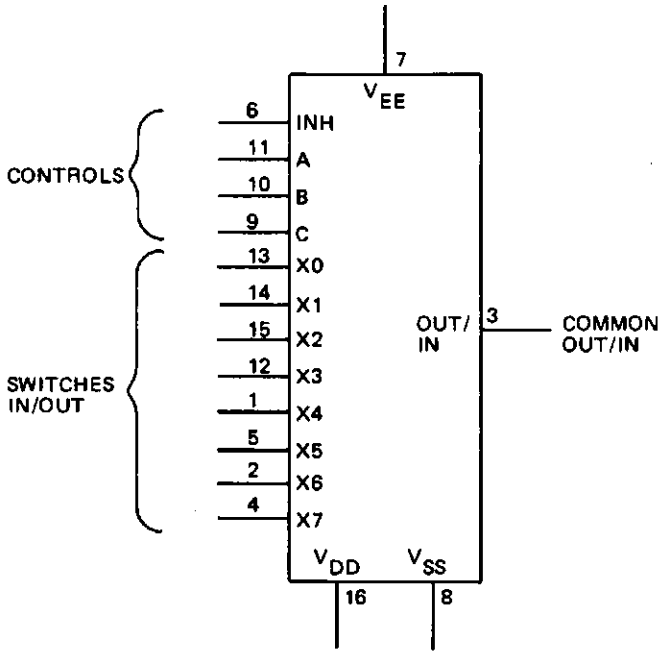
develops address gate and update pulses, and a driving voltage for the unit front panel BUSY indicator. (These signals are used in the control unit only.)

With the unit front panel CONT switch in NORM and no busy signal input from the unit being controlled, the input to U4D-13 is logic 0. The input from P1-71 through U11B to U4D-12 is logic 1. This develops a logic 0 from exclusive OR gate U12D and AND gate U28B. The logic 0 U28B output prevents the BUSY indicator on the unit front panel from lighting. This same signal is clocked through U20A to inhibit U28D from gating out WD4R pulses which are used as update requests.

When a busy signal input is received in the monitor data, the input to U4D-13 goes to logic 1. In NORM, U4D-11 is logic 0, U12D-11 is logic 1, and both inputs to U28B are logic 1. This develops a logic 1 to U28A-2 and to busy indicator output (to cause the BUSY indicator to light). The input to U28A from U4D-11 enables U28A and causes it to output continuous WD4R pulses as an address gate signal. The input to U28C-8 is logic 0, causing gate U28D to keep the update output inhibited.

When the front panel CONT switch is changed from NORM to TEST in a not-busy condition, U4D-13 is logic 0 keeping the busy indicator output at logic 0 as

SYMBOL

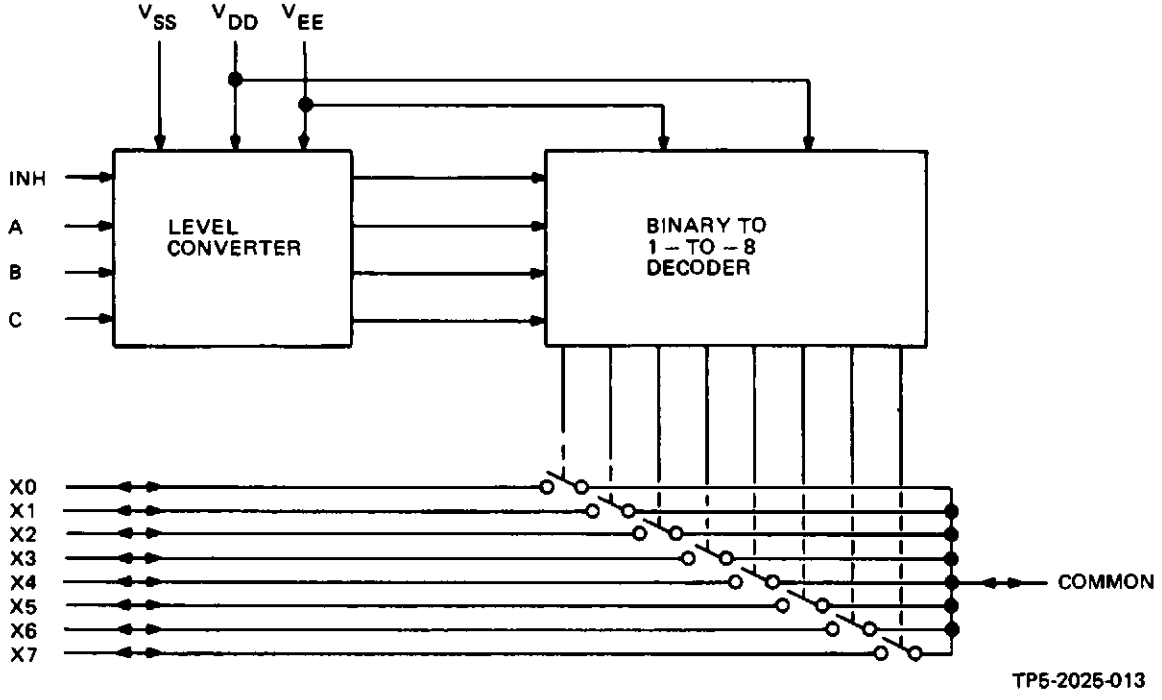


TRUTH TABLE

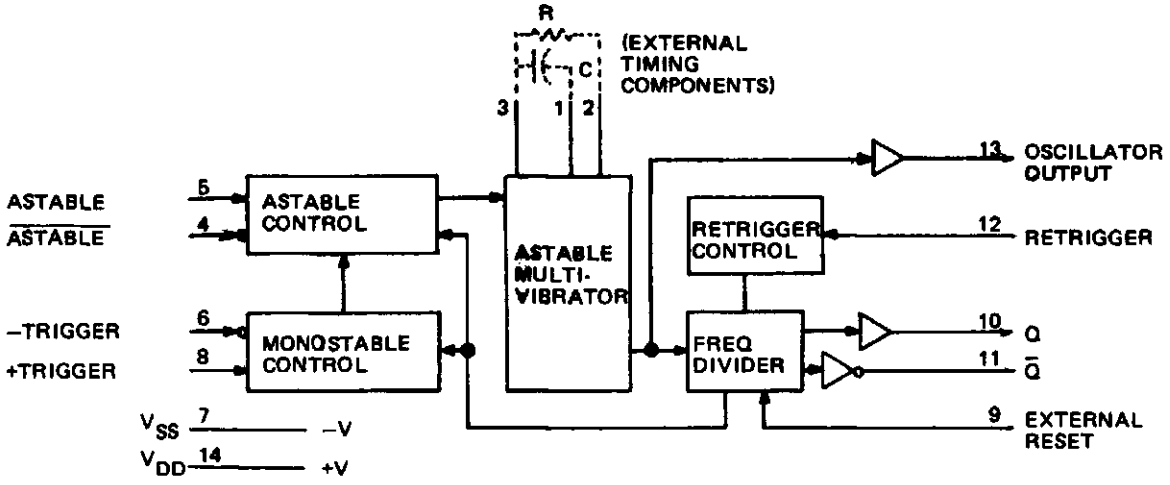
CONTROL				CLOSED SWITCH (COMMON)
INH	C	B	A	
0	0	0	0	X0
0	0	0	1	X1
0	0	1	0	X2
0	0	1	1	X3
0	1	0	0	X4
0	1	0	1	X5
0	1	1	0	X6
0	1	1	1	X7
1	X	X	X	NONE

X = DON'T CARE

FUNCTIONAL DIAGRAM



8-Channel Multiplexer/Demultiplexer MC14051B
Figure 3



FUNCTIONAL TERMINAL CONNECTIONS

NOTE: IN ALL CASES EXTERNAL RESISTOR BETWEEN TERMINALS 2 AND 3, EXTERNAL CAPACITOR BETWEEN TERMINALS 1 AND 3.

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	TO V_{DD}	TO V_{SS}	INPUT PULSE TO		
ASTABLE MULTIVIBRATOR:					
FREE RUNNING	4, 5, 6, 14	7, 8, 9, 12	–	10, 11, 13	t_A (10, 11)=4.40 RC
TRUE GATING	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	t_A (13)=2.20 RC
COMPLEMENT GATING	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
MONOSTABLE MULTIVIBRATOR					
POSITIVE-EDGE TRIGGER	4, 14	5, 6, 7, 9, 12	8	10, 11	
NEGATIVE-EDGE TRIGGER	4, 8, 14	5, 7, 9, 12	6	10, 11	
RETRIGGERABLE	4, 14	5, 6, 7, 9	8, 12	10, 11	t_M (10, 11)=2.48 RC

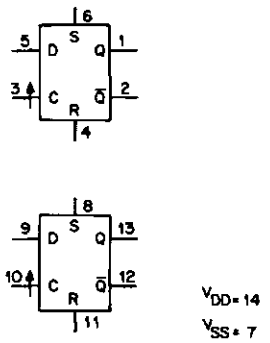
TP5-2029-012

Low-Power Monostable/Astable Multivibrator CD4047AE
Figure 4

before. (The logic 0 input to U28A also keeps the ADRG output inhibited.) Switching from NORM to TEST causes U12C to develop a momentary output pulse that is used to trigger U3A. The resulting output from U3B is a logic 1 pulse that causes a logic 0 output from U4A-3. This input to U12A allows the exclusive OR gate to momentarily go to logic 1 and set U20A-1 to logic 1. (The not-busy, logic 0 input from U28B-4 to U20A-5 and clock input to U20A-3 from the WD4R clock the Q output from U20A-1 back to logic 0.) The momentary logic 1 at U28D-13 permits one WD4R pulse to be gated out (U28D-11) as an update pulse.

With a busy signal present (U4D-13 at logic 1) when the CONT switch is placed in the TEST position, the set pulse to U20A-6 is developed as described above; however, the resulting logic 1 from U4D-11 causes U12D-11 to be logic 0. This switches the logic 1 busy indicator output to logic 0, turning off the front panel busy indicator, and causes the Q output from U20A to go to logic 0 after the set input pulse from U12A goes to logic 0. The resulting update output is one logic 1 pulse and the ADRG output is a constant logic 0.

When the front panel CONT switch is changed from TEST to NORM, the logic 1 output pulse from U3B-10



TRUTH TABLE

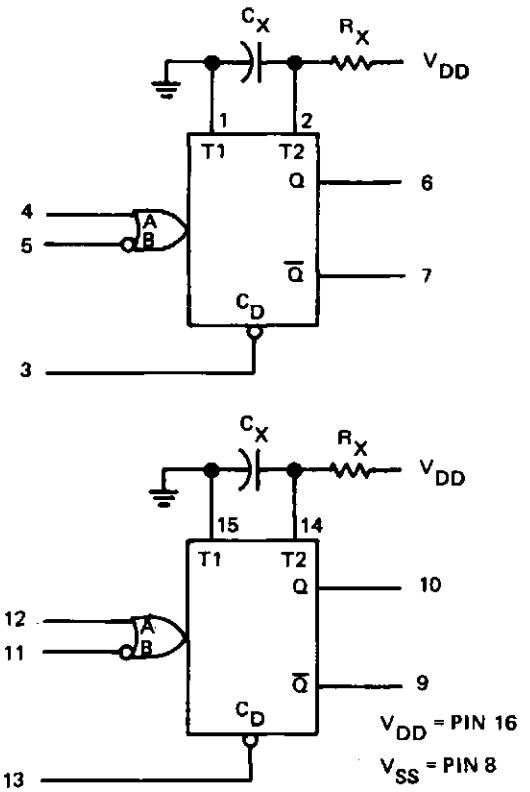
INPUTS				OUTPUTS	
CLOCK*	DATA	RESET	SET	Q	Q̄
↗	0	0	0	0	1
↗	1	0	0	1	0
↘	X	0	0	Q	Q̄ NO CHANGE
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

X = DON'T CARE
* = LEVEL CHANGE

TP5-2027-012

Dual D-Type Flip-Flop CD4013AE
Figure 5

BLOCK DIAGRAM

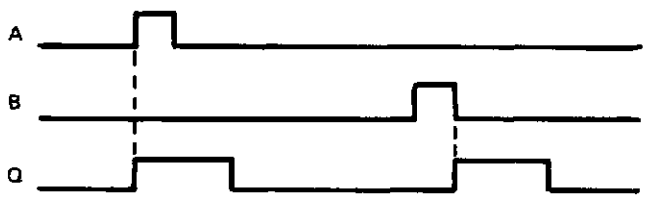


A INPUT TERMINAL CLOCKS ON 0-TO-1 TRANSITION.

B INPUT TERMINAL CLOCKS ON 1-TO-0 TRANSITION.

C_D (RESET) TERMINAL, WHEN SWITCHED TO LOGIC 0, IMMEDIATELY TERMINATES OUTPUT PULSE.

R_X AND C_X ARE EXTERNAL COMPONENTS.



TP5-2299-011

Dual Monostable Multivibrator CD4098BE
Figure 6

is developed as described above. (Exclusive OR gate U12C develops an output trigger pulse to U3A-4 when the input to pin 8 changes from one logic level to the other.) With a not-busy signal present, U4D-11 is logic 1. This enables U28C to gate the WD4R pulses to U28D. The logic 1 at U12D-13 develops a logic 0 at U12D-11 and inhibits gate U28B. The logic 0 output from U28B-4 is the busy indicator output, the D input to U20A, and an inhibiting input to U28A. The resulting Q output from U20A inhibits gate U28D, developing a logic 0 update output. With U28A inhibited, the ADRG output is also held at logic 0.

With a busy signal present when the CONT switch is set to NORM, U4D-11 is logic 0 which causes the update output to be logic 0. The logic 1 output from U12D-11 causes U28B-4 to be switched to logic 1. This outputs a logic 1 busy indicator signal and enables gate U28A. The WD4R input to U28A-1 is then gated out as continuous ADRG pulses.

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the parallel output card are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 1 check total performance of the parallel output card. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

Table 1. Parallel Output, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	**Note** These testing and troubleshooting procedures are based on using a control unit and an associated local unit. The most effective method of testing and troubleshooting is obtained by installing the questionable parallel output in the control unit. During these tests when a control unit is referred to it is a receiver-exciter control, or a receiver control. When a local unit is referred to it is a receiver-exciter, an exciter, or a receiver.		
	a. Remove top cover of unit containing the parallel output that is to be tested.		
	b. Remove parallel output. Install it on an extender card and place it in the control unit.		
	c. Set control unit and local unit LINE SELECTOR switches to 115 V.		
	d. Connect control unit and local unit to 115-V ac power source and set power on.		
	e. Measure dc voltages, on the card under test, between the following pins and ground (TP1, brown):		
	P1-45 P1-65 P1-114	+15 ±1.0 V dc. +5 ±0.5 V dc. -15 ±1.0 V dc.	Check associated power supply.
	f. Strap local unit for address 0.		
	g. Connect local unit to control unit.		
2. Data inputs, word 1	a. Set control unit CONT switch to TEST.		
	Note Word 1 tests can also be accomplished with the control unit CONT switch in NORM and local unit CONT switch in LCL. Then set local unit controls to positions indicated.		
	b. Set control unit FREQUENCY KHZ controls for 29 999.9(9).	Frequency display reads 29 999.9(9). Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
(Cont)			

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. Data inputs, word 1 (Cont)	c. Set control unit FREQUENCY KHZ controls for 16 666.6(6).	Frequency display reads 16 666.6(6). Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	d. Set control unit FREQUENCY KHZ controls for 02 000.0(0).	Frequency display reads 02 000.0(0). Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	Note Logic 1 = NLT +3.0 V dc. Logic 0 = NMT 0.5 V dc.		

BCD OUTPUT SIGNAL		PARALLEL OUTPUT PIN NO P1-( )	LOGIC LEVELS 29 999.9(9)	16 666.6(6)	02 000.0(0)	IF ABNORMAL CHECK
10 MHz	(2)	129	1	0	0	U6, U5, U7, U11, and associated circuits.
	(1)	64	0	1	0	
1 MHz	(8)	128	1	0	0	
	(4)	63	0	1	0	
	(2)	127	0	1	1	
	(1)	62	1	0	0	
100 kHz	(8)	126	1	0	0	U14, U5, U7, U11, and associated circuits.
	(4)	61	0	1	0	
	(2)	125	0	1	0	
	(1)	60	1	0	0	
10 kHz	(8)	124	1	0	0	
	(4)	59	0	1	0	
	(2)	123	0	1	0	
	(1)	58	1	0	0	

(Cont)

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. Data inputs, word 1 (Cont)			

BCD OUTPUT SIGNAL		PARALLEL OUTPUT PIN NO P1-( )	LOGIC LEVELS 29 999.9(9)	16 666.6(6)	02 000.0(0)	IF ABNORMAL CHECK
1 kHz	(8)	122	1	0	0	U22, U5, U7, U11, and associated circuits.
	(4)	57	0	1	0	
	(2)	121	0	1	0	
	(1)	56	1	0	0	
100 Hz	(8)	120	1	0	0	
	(4)	55	0	1	0	
	(2)	119	0	1	0	
	(1)	54	1	0	0	
10 Hz (with no 10-Hz tuning)	(8)	118	0	0	0	U30, U5, U7, U11, and associated circuits.
	(4)	53	0	0	0	
	(2)	117	0	0	0	
	(1)	52	0	0	0	
10 Hz (with 10-Hz tuning)	(8)	118	1	0	0	
	(4)	53	0	1	0	
	(2)	117	0	1	0	
	(1)	52	1	0	0	
1 Hz (with no 1-Hz tuning)	(8)	116	0	0	0	U30, U5, U7, U11, and associated circuits.
	(4)	51	0	0	0	
	(2)	115	0	0	0	
	(1)	50	0	0	0	
1 Hz (with 1-Hz tuning)	(8)	116	1	0	0	
	(4)	51	0	1	0	
	(2)	115	0	1	0	
	(1)	50	1	0	0	

Note

If a processor control is used, the 1-Hz outputs can be checked in the same manner that the other frequency outputs are checked.

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. Data inputs, word 2	a. Set control unit CONT switch to TEST. **Note** Word 2 tests can also be accomplished with the control unit CONT switch in NORM and local unit CONT switch in REM. Then measure voltages at local unit or control unit parallel output card (the card being tested). Rf gain test, steps b and c, is applicable to receiver and receiver-exciter controls only. b. Set control unit RF GAIN control to MAX.		
	c. Connect a dvm to TP5 (green).	Note dc levels as shown in chart for different RF GAIN positions.	Check U18, U9, U11, U1, and associated circuits. Check also circuit indicated in chart.

RF GAIN CONTROL SETTINGS		TP5 (DC VOLTS)	IF ABNORMAL CHECK
MAX	1	0.000 ±0.010	None
↓	*	-0.158 ±0.010	R20
	2	-0.316 ±0.010	R19
	*	-0.475 ±0.020	R19, R20
	3	-0.634 ±0.020	R18
	*	-0.792 ±0.030	R18, R20
rotated	4	-0.950 ±0.030	R17
from MAX	*	-1.108 ±0.040	R17, R20
ccw toward	5	-1.266 ±0.040	R16
MIN	*	-1.417 ±0.050	R16, R20
↓	6	-1.568 ±0.050	R15
	*	-1.712 ±0.060	R15, R20
	7	-1.855 ±0.060	R14
	*	-2.022 ±0.070	R14, R20
	8	-2.188 ±0.070	R13
MIN	*	-2.332 ±0.080	R13, R20

and U10.

(Cont)

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. Data inputs, word 2 (Cont)			

RF GAIN CONTROL SETTINGS		TP5 (DC VOLTS)	IF ABNORMAL CHECK
MAX	9	-2.465 ±0.080	R12
↓	*	-2.619 ±0.090	R12, R20
	10	-2.773 ±0.090	R11
	*	-3.002 ±0.100	R11, R20
	11	-3.130 ±0.100	R10
	*	-3.283 ±0.110	R10, R20
rotated	12	-3.439 ±0.110	R9
from MAX	*	-3.570 ±0.120	R9, R20
ccw toward	13	-3.700 ±0.120	R8
MIN	*	-3.886 ±0.130	R8, R20
	14	-4.072 ±0.130	R7
↓	*	-4.218 ±0.140	R7, R20
	15	-4.363 ±0.140	R6
	*	-4.532 ±0.150	R6, R20
	16	-4.700 ±0.150	R5
MIN	*	-4.858 ±0.160	R5, R20

and U2.

*Controlled by least significant bcd input for rf gain control, available only on processor controls. Bcd for least significant bcd signal at MAX setting is bit wt 0. Bcd signal for most significant bcd signal at one step beyond MIN setting is bit wt 31.

Note

AGC tests, steps d through f, are applicable to the receiver and receiver-exciter controls only.

	d. Set control unit AGC switch to FAST.	Check logic levels at the associated parallel output pin numbers as shown in chart.
	e. Set control unit AGC switch to OFF.	Check logic levels at the associated parallel output pin numbers as shown in chart.
	f. Set control unit AGC switch to SLOW.	Check logic levels at the associated parallel output pin numbers as shown in chart.
(Cont)		

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. Data inputs, word 2 (Cont)	**Note** Logic 1 = NLT +3.0 V dc. Logic 0 = NMT 0.5 V dc.		

PARALLEL OUTPUT	PIN NO P1-( )	AGC SWITCH POSITION			IF ABNORMAL CHECK
		FAST	OFF	SLOW	
CH A AGC OFF	84	0	1	0	U26, U17, U7, U11, and associated circuits.
CH A AGC FAST	85	1	0	0	
CH B AGC OFF	19	0	1	0	
CH B AGC FAST	20	1	0	0	

	Note Bandwidth tests, steps g and h, are applicable to the receiver control only.		
	g. Set control unit MODE switch to SSB/CW.		
	h. Set control unit BANDWIDTH switch to each of its positions.	The display associated with the BANDWIDTH switch positions lights. Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
(Cont)	**Note** Logic 1 = NLT +3.0 V dc. Logic 0 = NMT 0.5 V dc.		

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. Data inputs, word 2 (Cont)			

PARALLEL OUTPUT	PIN NO P1-( )	BANDWIDTH SWITCH POSITION								IF ABNORMAL CHECK
		16	A	B	USB	LSB	C	D	E	
FL8	100	1	0	0	0	0	0	0	0	U27, U17, U7, U11, and associated circuits.
FL3	33	0	1	0	0	0	0	0	0	
FL4	98	0	0	1	0	0	0	0	0	
FL1	32	0	0	0	1	0	0	0	0	
FL2	97	0	0	0	0	1	0	0	0	
FL5	34	0	0	0	0	0	1	0	0	
FL6	35	0	0	0	0	0	0	1	0	
FL7	99	0	0	0	0	0	0	0	1	

	Note Mode tests, step i, are applicable to the receiver control only.	
	i. Set MODE switch (receiver control only) to each of its positions.	The display associated with the MODE switch position lights. Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
(Cont)	**Note** Logic 1 = NLT +3.0 V dc. Logic 0 = NMT 0.5 V dc.		

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. Data inputs, word 2 (Cont)			

PARALLEL OUTPUT	PIN NO P1-( )	MODE SWITCH POSITION			IF ABNORMAL CHECK
		*SSB/CW	*AM	ISB	
SSB EN	72	1	0	1	U25, U17, U7, U11, and associated circuits.
AM EN	8	0	1	0	
FM EN	73	0	0	0	
CW EN	9	0	0	0	
ISB EN	74	0	0	1	

*In these positions the display and logic levels associated with the BANDWIDTH switch position are also activated.

Note

Mode tests, step j, are applicable to the exciter and receiver-exciter controls only.

j. Set MODE switch (exciter and receiver-exciter controls only) to each of its positions.

The display associated with the MODE switch position lights. Refer to chart for logic levels and associated parallel output pin numbers.

Note

Logic 1 = NLT +3.0 V dc.
Logic 0 = NMT 0.5 V dc.

(Cont)

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. Data inputs, word 2 (Cont)			

PARALLEL OUTPUT	PIN NO P1-( )	MODE SWITCH POSITION					IF ABNORMAL CHECK
		CW	LSB	USB	AM	ISB	
SSB EN	72	1	1	1	0	1	U25, U17, U7, U11, and associated circuits.
AM EN	8	0	0	0	1	0	
FM EN	73	0	0	0	0	0	
CW EN	9	1	0	0	0	0	
ISB EN	74	0	0	0	0	1	
FL1 (USB) EN	32	0	0	1	0	0	U27, U17, U7, U11, and associated circuits.
FL2 (LSB) EN	97	0	1	0	0	0	

4. Data inputs, word 3	a. Set control unit CONT switch to TEST. **Note** Word 3 tests can also be accomplished with control unit CONT switch in NORM and local unit CONT switch in REM. Then measure voltages at local unit parallel output card (the card being tested). Pa tests, steps b through e, are applicable to the exciter and receiver-exciter controls only.		
	b. Set control unit PA PWR switch to OFF.	Check logic levels at the associated parallel output pin numbers as shown in chart.	
	c. Set control unit PA PWR switch to STBY.	Check logic levels at the associated parallel output pin numbers as shown in chart.	
(Cont)	d. Set control unit PA PWR switch to HIGH PWR.	Check logic levels at the associated parallel output pin numbers as shown in chart.	

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. Data inputs, word 3 (Cont)	e. Set control unit PA PWR switch to LOW PWR. **Note** Logic 1 = NLT +3.0 V dc. Logic 0 = NMT 0.5 V dc.	Check logic levels at the associated parallel output pin numbers as shown in chart.	

PARALLEL OUTPUT	PIN NO P1-( )	PA PWR SWITCH POSITION				IF ABNORMAL CHECK
		OFF	STBY	HIGH PWR	LOW PWR	
PA LV EN	79	0	1	1	1	U19, U5, U7, U11, and associated circuits.
PA HV EN	14	0	0	1	1	
LO PWR EN	78	0	0	0	1	

	Note Pilot carrier tests, steps f and g, are applicable to the exciter and receiver-exciter controls only.		
	f. Set control unit P CAR switch to OFF.	Logic level 0 at P1-82 (NMT 0.5 V dc).	Check U19, U5, U7, U11, and associated circuits.
	g. Set control unit P CAR switch to ON.	Logic level 1 at P1-82 (NLT +3.0 V dc).	
	Note Dvbfo tests, steps h through k, are applicable only to the receiver and receiver-exciter controls with a dvbfo option installed.		
(Cont)	h. Set the control unit MODE switch to SSB/CW or CW and BFO switch to VAR.		

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. Data inputs, word 3 (Cont)	i. Set digital VBFO controls for +9990 Hz.	VBFO frequency display reads +9990. Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	j. Set digital VBFO controls for -6660 Hz.	VBFO frequency display reads -6660. Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	k. Set digital VBFO controls for +1000 Hz.	VBFO frequency display reads +1000. Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	Note Logic 1 = NLT +3.0 V dc. Logic 0 = NMT 0.5 V dc.		

BCD OUTPUT SIGNAL		PARALLEL OUTPUT PIN NO P1-( )	LOGIC LEVELS +9990	LOGIC LEVELS -6660	LOGIC LEVELS +1000	IF ABNORMAL CHECK
DVBFO 1 kHz	(8)	48	1	0	0	U29, U5, U7, U11, and associated circuits.
	(4)	113	0	1	0	
	(2)	47	0	1	0	
	(1)	112	1	0	1	
DVBFO 100 Hz	(8)	46	1	0	0	U21, U5, U7, U11, and associated circuits.
	(4)	111	0	1	0	
	(2)	110	0	1	0	
	(1)	44	1	0	0	
DVBFO 10 Hz	(8)	109	1	0	0	
	(4)	43	0	1	0	
	(2)	108	0	1	0	
	(1)	42	1	0	0	
DVBFO SIGN		107	1	0	1	U29, U5, U7, U11, and associated circuits.

(Cont)

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. Data inputs, word 3 (Cont)	**Note** Analog vbfo tests, steps l and m, are applicable only to the receiver and receiver-exciter controls with an analog vbfo option installed. l. Set the control unit MODE switch to SSB/CW or CW and BFO switch to VAR. m. Rotate the BFO control through its complete range.	Check logic levels at the associated parallel output pin numbers as shown in chart.	

BCD OUTPUT SIGNAL		LOGIC LEVELS PARALLEL OUTPUT PIN NO P1-( ) 48	113	47	112	LOGIC DISPLAY	IF ABNORMAL CHECK
- (Full ccw)	1	1	1	1	1		U29, U5, U7, U11, and associated circuits.
	2	1	1	1	0		
	3	1	1	0	1		
	4	1	1	0	0		
	5	1	0	1	1		
	6	1	0	1	0		
	7	1	0	0	1		
Rotated from - cw toward +	8	1	0	0	0		
	9	0	1	1	1		
	10	0	1	1	0		
	11	0	1	0	1		
	12	0	1	0	0		
	13	0	0	1	1		
	14	0	0	1	0		
	15	0	0	0	1		
+ (Full cw)	16	0	0	0	0		

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. Data inputs, word 4	a. Set control unit CONT switch to NORM.		
	b. Set local unit CONT switch to LCL.		
	Note System key test, steps c and d, is applicable only to exciter and receiver-exciter controls.		
	c. Set local unit KEY switch to LOCK.	Control unit KEY display lights. Logic level 1 at P1-68 (NLT +3.0 V dc).	Check U15, U17, U7, U11, and associated circuits.
	d. Set local unit KEY switch to NORM.	Control unit KEY display goes out. Logic level 0 at P1-68 (NMT 0.5 V dc).	
	e. Set local unit PWR switch off and back on.	Control unit EXCTR FAULT, RCV FAULT, or R/E FAULT lights. Logic level 1 at P1-12 (NLT +3.0 V dc).	Check U16, U12, U8, U17, U7, U11, and associated circuits.
	f. Change any frequency control on local unit front panel.	Control unit EXCTR FAULT, RCV FAULT, or R/E FAULT goes out. Logic level 0 at P1-12 (NMT 0.5 V dc).	
	Note Receive overload test, steps g and h, is applicable only to receiver and receiver-exciter controls.		
	g. Connect +5 V dc to local unit J16-27.	Control unit RCV OVERLOAD lights. Logic level 1 at P1-67 (NLT +3.0 V dc)	Check U16, U17, U7, U11, and associated circuits.
	h. Remove +5 V dc from local unit J16-27.	Control unit RCV OVERLOAD goes out. Logic level 0 at P1-67 (NMT 0.5 V dc).	Same as step g.
	Note Coupler fault test, steps i and j, is applicable only to exciter and receiver-exciter controls.		
(Cont)			

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. Data inputs, word 4 (Cont)	i. Connect +5 V dc to local unit J15-1.	Control unit COUPLER FAULT lights. Logic level 1 at P1-13 (NLT +3.0 V dc).	Same as step g.
	j. Remove +5 V dc from local unit J15-1.	Control unit COUPLER FAULT lights. Logic level 0 at P1-13 (NMT 0.5 V dc).	
	Note Rf out test, steps k and l, is applicable only to exciter and receiver-exciter controls.		
	k. Connect ground signal to local unit J15-5.	Control unit RF OUT lights. Logic level 1 at P1-5 (NLT +3.0 V dc).	
	l. Remove ground signal from local unit J15-5.	Control unit RF OUT goes out. Logic level 0 at P1-5 (NMT 0.5 V dc).	
	Note Pa fault test, steps m and n, is applicable only to exciter and receiver-exciter controls.		
	m. Connect +5 V dc to local unit J15-3.	Control unit PA FAULT lights. Logic level 1 at P1-77 (NLT +3.0 V dc).	
	n. Remove +5 V dc from local unit J15-3.	Control unit PA FAULT goes out. Logic level 0 at P1-77 (NMT 0.5 V dc).	
	Note Pa ready test, steps o and p, is applicable only to exciter and receiver-exciter controls.		
(Cont)	o. Connect ground signal to local unit J15-21.	Control unit PA READY lights. Logic level 0 at P1-69 (NMT 0.5 V dc).	

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. Data Inputs, word 4 (Cont)	p. Remove ground signal from local unit J15-21.	Control unit PA READY goes out. Logic level 0 at P1-69 (NMT 0.5 V dc).	Same as step g.
	q. Press and hold local unit CONT switch to MON.	Logic level 1 at P1-30 (NLT +3.0 V dc).	Check U24, U17, U7, U11, and associated circuits.
	r. Set local unit CONT switch to REM.	Logic level 0 at P1-30 (NMT 0.5 V dc).	
	s. Set local unit CONT switch to LCL.	Logic level 1 at P1-95 (NLT +3.0 V dc).	
		Control unit BUSY indicator lights. Logic level 1 at P1-7 (NLT +3.0 V dc).	Check U28, U20, U12, U4, U24, U17, U7, U11, and associated circuits.
	t. Set local unit CONT switch to REM.	After short delay logic level 0 at P1-95 (NMT 0.5 V dc).	Same as step s.
		After short delay control unit BUSY indicator goes out. Logic level 0 at P1-7 (NMT 0.5 V dc).	
	u. Set local unit CONT switch to LCL.		
	v. Apply a ground to local unit A13U51A-6.		
	w. Apply a ground to local unit A13U51A-3.		
	x. Remove ground from local unit A13U51A-3.		
	y. Apply ground to local unit A13U16A-1, 2, 8.		
	z. Remove ground from local unit A13U16A-1, 2, 8.	Logic level 1 at P1-29 (NLT +3.0 V dc).	Same as step q.
	aa. Remove ground from local unit A13U51A-6.		
(Cont)	ab. Apply ground to local unit A13U42A-3.	Logic level 0 at P1-29 (NMT 0.5 V dc).	

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. Data inputs, word 4 (Cont)	ac. Remove ground from local unit A13U42A-3.		Same as step q.
	Note Preselector fault tests, steps ad and ae, are applicable to receiver and receiver-exciter controls only.		
	ad. Apply +5 V dc to local unit J16-8.	Control unit PRESEL FAULT lights. Logic level 1 at P1-28 (NLT +3.0 V dc).	
	ae. Remove +5 V dc from local unit J16-8.	Control unit PRESEL FAULT goes out. Logic level 0 at P1-28 (NMT 0.5 V dc).	

4. REPAIR

Repair of the parallel output card is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

5. PARTS LIST/DIAGRAMS

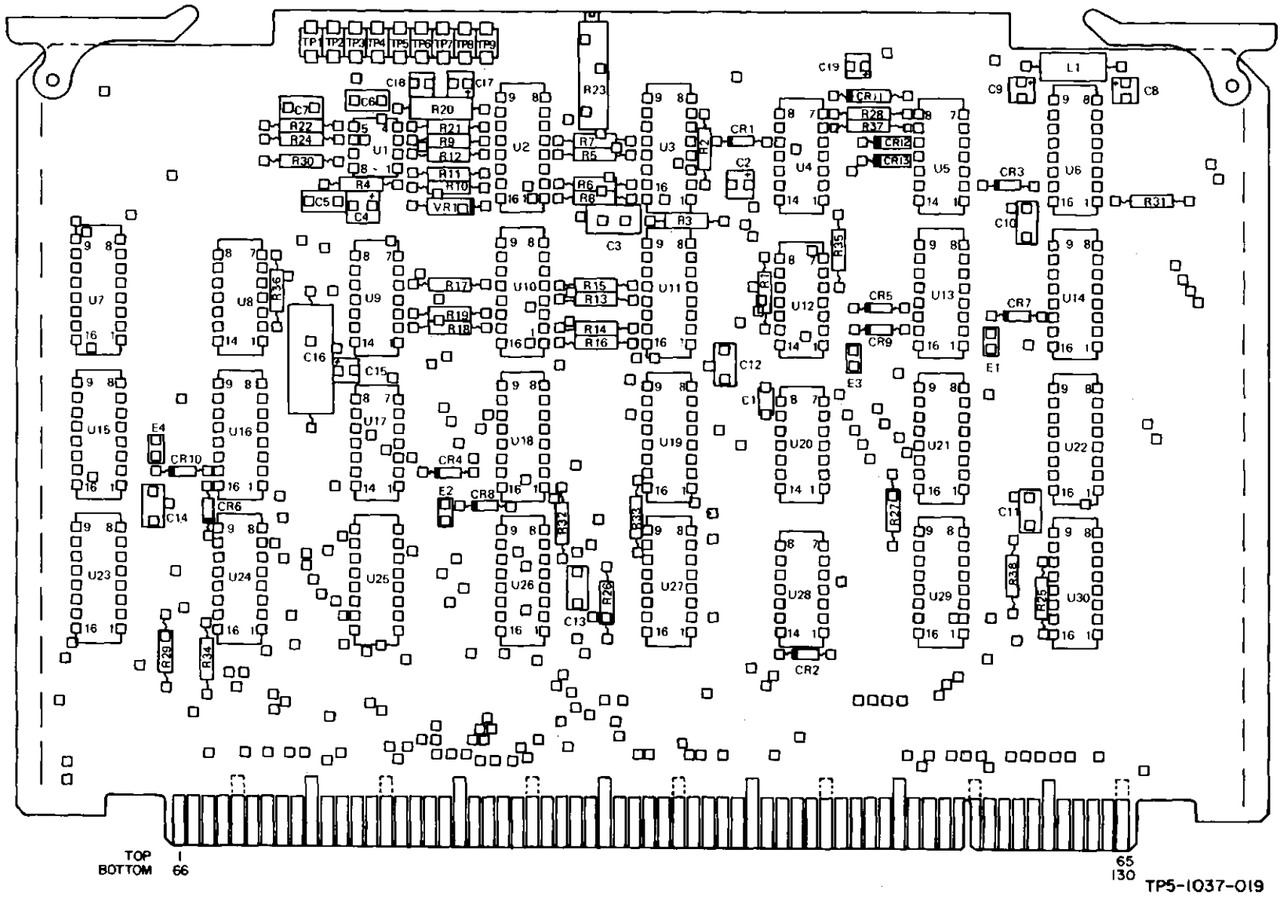
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram, figure 7. The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points to the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Parallel output	635-0752-001	REV J
Parallel output	635-0752-002	REV K



Parallel Output, Schematic Diagram
Figure 7 (Sheet 1 of 8)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	PARALLEL OUTPUT 635-0752-001		A
	635-0752-002		B
CR1-CR10	SEMICOND DEVICE, 1N4454	353-3644-010	
CR11-CR13	SEMICOND DEVICE, 1N4454	353-3644-010	B
C1	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C2	CAPACITOR, FXD, ELCTLT, 0.47μF, 20%, 35V	184-9102-330	
C3	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 500V	912-3879-000	
C4	CAPACITOR, FXD, ELCTLT, 15μF, 20%, 15V	184-9102-130	
C5-C7	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C8, C9	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	
C10-C14	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C15	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	
C16	CAPACITOR, FXD, PLSTC DIEL, 1μF, 10%, 50V	933-1081-200	
C17	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V (A4)	184-9102-350	A
C18	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V (A1)	913-3279-200	A
C18	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	B
C19	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	B
L1	COIL, RF, 1000μH	240-2540-000	
R1-R3	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R4	RESISTOR, FXD, CMPSN, 1.5kΩ, 10%, 1/4W	745-0755-000	
R5	RESISTOR, FXD, FILM, 10.2kΩ, 1%, 1/8W	705-3605-480	
R6	RESISTOR, FXD, FILM, 11kΩ, 1%, 1/8W	705-1046-000	
R7	RESISTOR, FXD, FILM, 11.8kΩ, 1%, 1/8W	705-3605-510	
R8	RESISTOR, FXD, FILM, 13kΩ, 1%, 1/8W	705-3605-530	
R9	RESISTOR, FXD, FILM, 14kΩ, 1%, 1/8W	705-1051-000	
R10	RESISTOR, FXD, FILM, 15.4kΩ, 1%, 1/8W	705-1053-000	
R11	RESISTOR, FXD, FILM, 17.4kΩ, 1%, 1/8W	705-3605-590	
R12	RESISTOR, FXD, FILM, 19.6kΩ, 1%, 1/8W	705-1058-000	
R13	RESISTOR, FXD, FILM, 22.1kΩ, 1%, 1/8W	705-3605-640	
R14	RESISTOR, FXD, FILM, 26.1kΩ, 1%, 1/8W	705-1064-000	
R15	RESISTOR, FXD, FILM, 30.9kΩ, 1%, 1/8W	705-3605-710	
R16	RESISTOR, FXD, FILM, 38.3kΩ, 1%, 1/8W	705-1072-000	
R17	RESISTOR, FXD, FILM, 51.1kΩ, 1%, 1/8W	705-1078-000	
R18	RESISTOR, FXD, FILM, 76.8kΩ, 1%, 1/8W	705-3605-900	
R19	RESISTOR, FXD, FILM, 154kΩ, 1%, 1/8W	705-1101-000	
R20	RESISTOR, FXD, FILM, 309kΩ, 1%, 1/8W	705-3601-230	
R21, R22	RESISTOR, FXD, FILM, 10kΩ, 1%, 1/8W	705-1044-000	
R23	RESISTOR, VAR, 10kΩ, 10%, 3/4W	382-0012-290	
R24	RESISTOR, FXD, FILM, 1kΩ, 1%, 1/8W	705-0996-000	
R25, R26	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R27	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	A
R27	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	B
R28-R35	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R36	RESISTOR, FXD, CMPSN, 0.33MΩ, 10%, 1/4W	745-0839-000	
R36	RESISTOR, FXD, CMPSN, 68kΩ, 10%, 1/4W, (A2)	745-0815-000	A
R36	RESISTOR, FXD, CMPSN, 0.68MΩ, 10%, 1/4W (A3)	745-0851-000	A
R36	RESISTOR, FXD, CMPSN, 0.68MΩ, 10%, 1/4W	745-0851-000	B
R37	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	B
R38	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0851-000	B
TP1	JACK, TIP, BRN	360-0484-070	
TP2	JACK, TIP,RED	360-0484-020	
TP3	JACK, TIP, ORN	360-0484-050	
TP4	JACK, TIP, YEL	360-0484-060	
TP5	JACK, TIP, GRN	360-0484-040	
TP6	JACK, TIP, BLU	360-0484-080	
TP7	JACK, TIP, VIO	360-0484-090	
TP8	JACK, TIP, GRA	360-0484-100	
TP9	JACK, TIP, WHT	360-0484-010	
U1	INTEGRATED CKT, MC1458P1	351-1071-070	
U2	MOS, ANLG MXR, F4051PC	351-8227-010	
u3	INTEGRATED CKT, MC14528BCP	351-8421-020	
U4	INTEGRATED CKT, MC14011CP	351-8159-040	
U5	INTEGRATED CKT, F4013BPC	351-8159-110	
U6	INTEGRATED CKT, CD4094BE	351-8346-010	
U7	MOS, ANLG MXR, F4051PC	351-8227-010	
U8	MICROCIRCUIT, CD4047AE	351-8200-020	
U9	INTEGRATED CKT, MC14071BCP	351-8287-010	
U10	MOS, ANLG MXR, F4051PC	351-8227-010	
U11	INTEGRATED CKT, F4049BPC	351-8159-210	

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
U12	INTEGRATED CKT, MC14070BCP	351-8407-010	
U13-U16	INTEGRATED CKT, CD4094BE	351-8346-010	
U17	INTEGRATED CKT, F4013BPC	351-8159-110	
U18, U19	INTEGRATED CKT, CD4094BE	351-8346-010	
U20	INTEGRATED CKT, F4013BPC	351-8159-110	
U21-U27	INTEGRATED CKT, CD4094BE	351-8346-010	
U28	INTEGRATED CKT, MC14081BCP	351-8287-030	
U29, U30	INTEGRATED CKT, CD4094BE	351-8346-010	
VR1	SEMICOND DEVICE, 1N752A (A4)	353-2712-000	
VR1	SEMICOND DEVICE, 1N751A	353-2710-000	A
VR1	SEMICOND DEVICE, 1N751A	353-2710-000	B

MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Added C18, 0.1μF	REV C and above.
A2	Changed R36 from 330 kΩ to 68 kΩ.	REV D and above.
A3	Changed R36 from 68 kΩ to 680 kΩ.	REV F and above.
A4	Removed C17, 1μF, electrolytic from junction of R20 and U18-11 (+) to ground (-). Changed VR1 from 1N752A (5.6 V) to 1N751A (5.1 V).	REV J and above.

The preceding modification history effectivities apply only to the 635-0752-001. Preceding modifications are included in all 635-0752-002 cards.

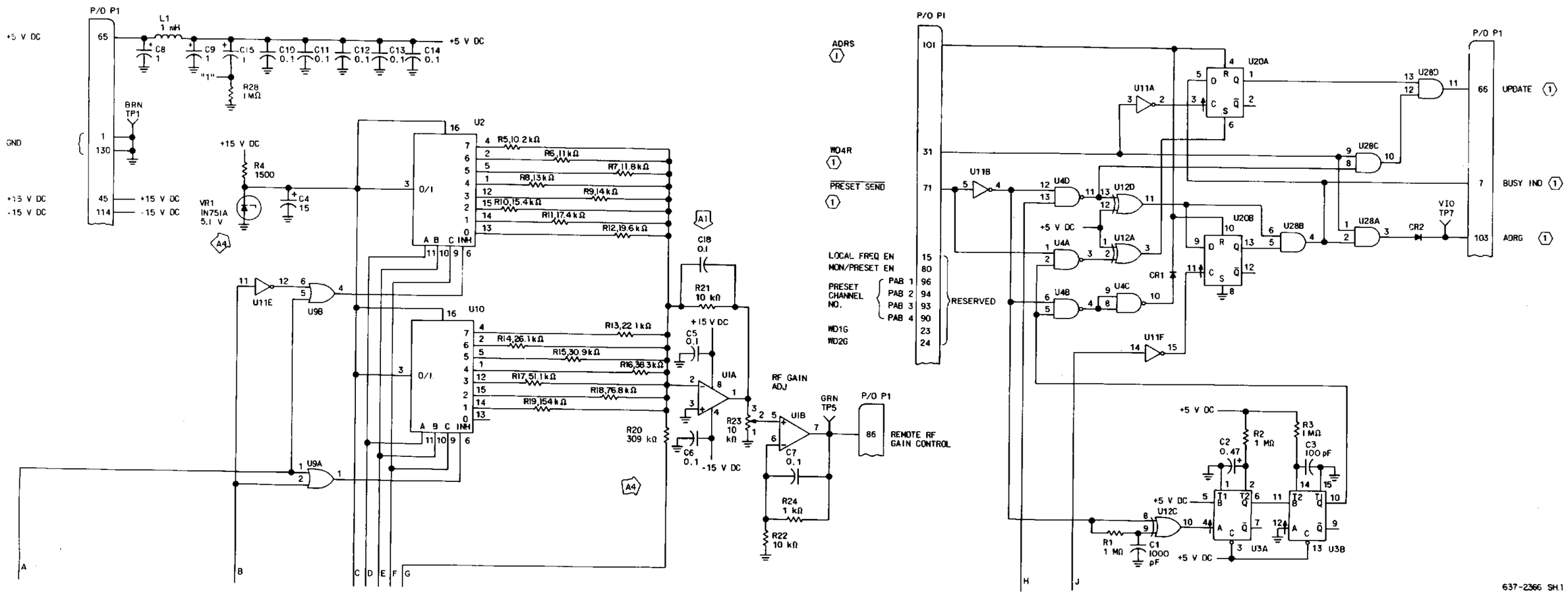
Parallel Output, Schematic Diagram
Figure 7 (Sheet 2)

POWER AND GROUND CONNECTIONS

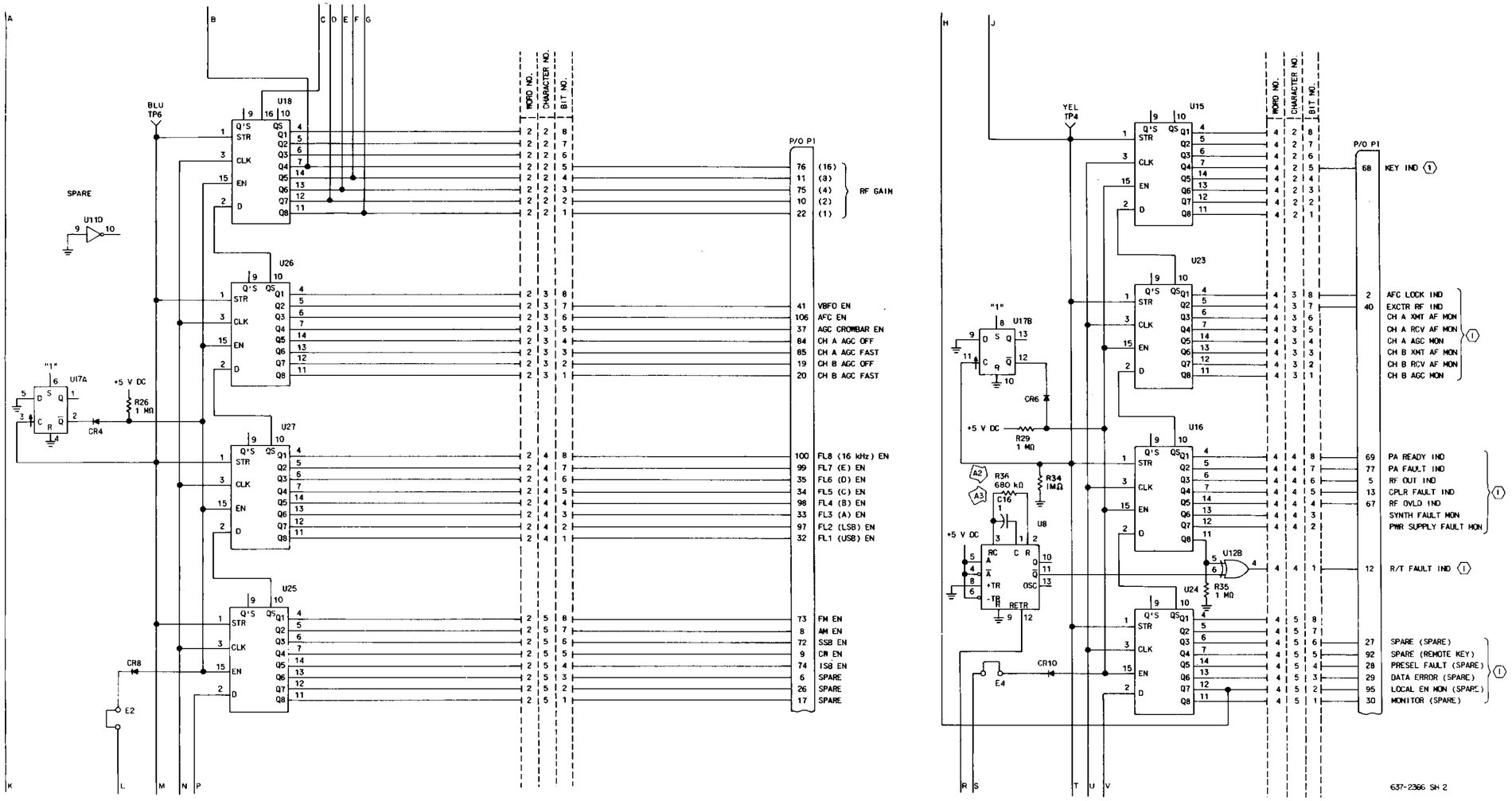
U NO.	TYPE	POWER (V DC)	
		+5	GND
U1	MC1458PI		
U2, U7, U10	F4051PC	16	8,7
U3	MC4528BCP	16	8
U4	MC4011CP	14	7
U5, U17, U20	F4013BPC	14	7
U6, U13-U16, U18, U19, U21-U27, U29, U30	CD4094BE	16	8
U8	CD4047AE	14	7
U9	MC4071BCP	14	7
U11	F4049BPC	1	8
U12	MC4070BCP	14	7
U18	MC4081BCP	14	7

NOTES:

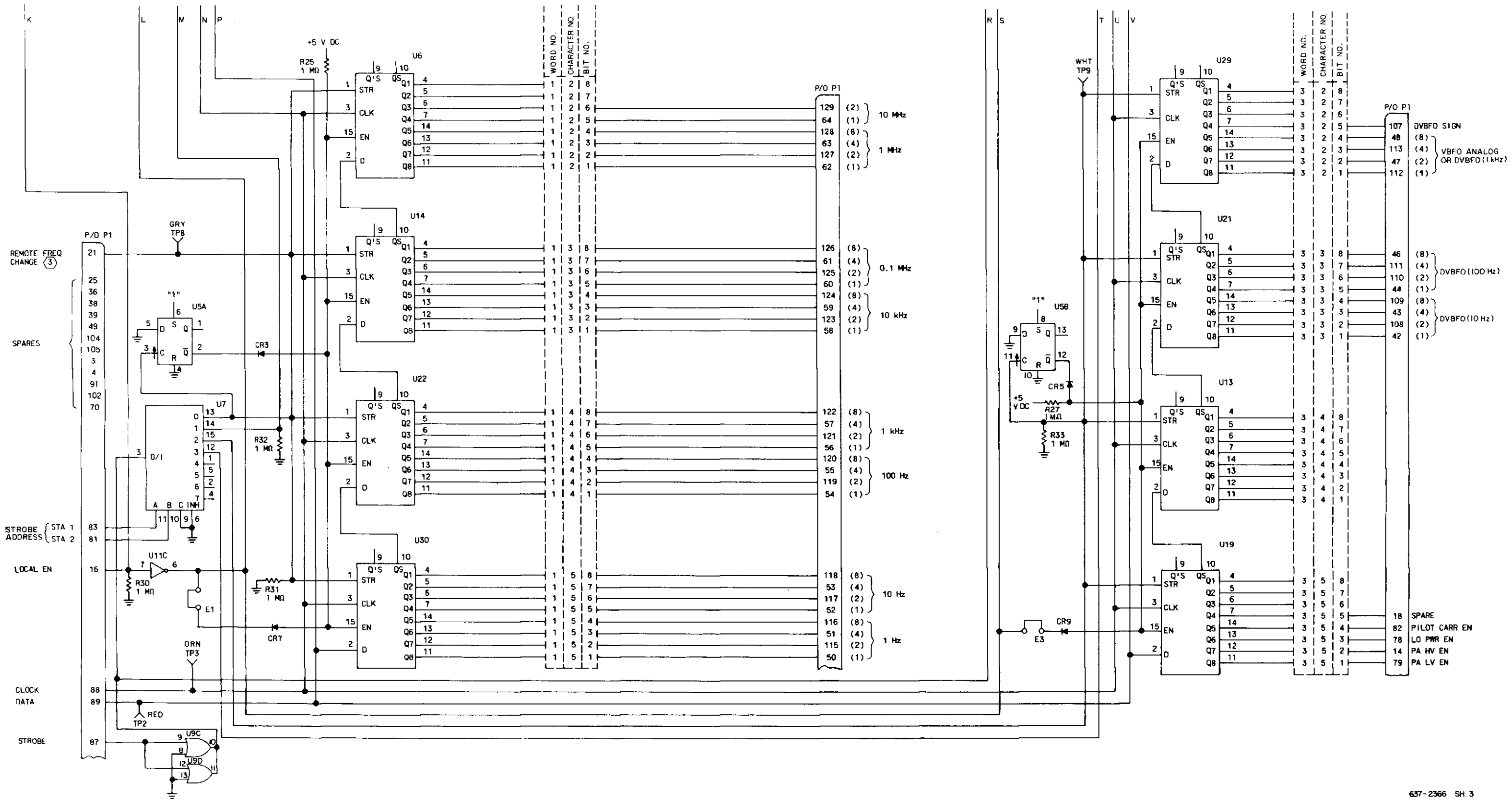
1. THESE FUNCTIONS ARE ONLY APPLICABLE TO REMOTE CONTROL UNITS.
2. FUNCTIONS IN PARENTHESES ARE APPLICABLE TO REMOTE CONTROL UNITS, (RCVR, EXCTR, RCVR-EXCTR). FOR A REMOTE UNIT, CHARACTER NO. LABELS SHOULD BE CHANGED FROM 5 TO 2.
3. THESE FUNCTIONS ARE NOT APPLICABLE TO REMOTE UNITS.
4. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS AND DIODES ARE TYPE 1N4454.
5. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.



Parallel Output (635-0752-001), Schematic Diagram
Figure 7 (Sheet 3)



Parallel Output (635-0752-001), Schematic Diagram
Figure 7 (Sheet 4)



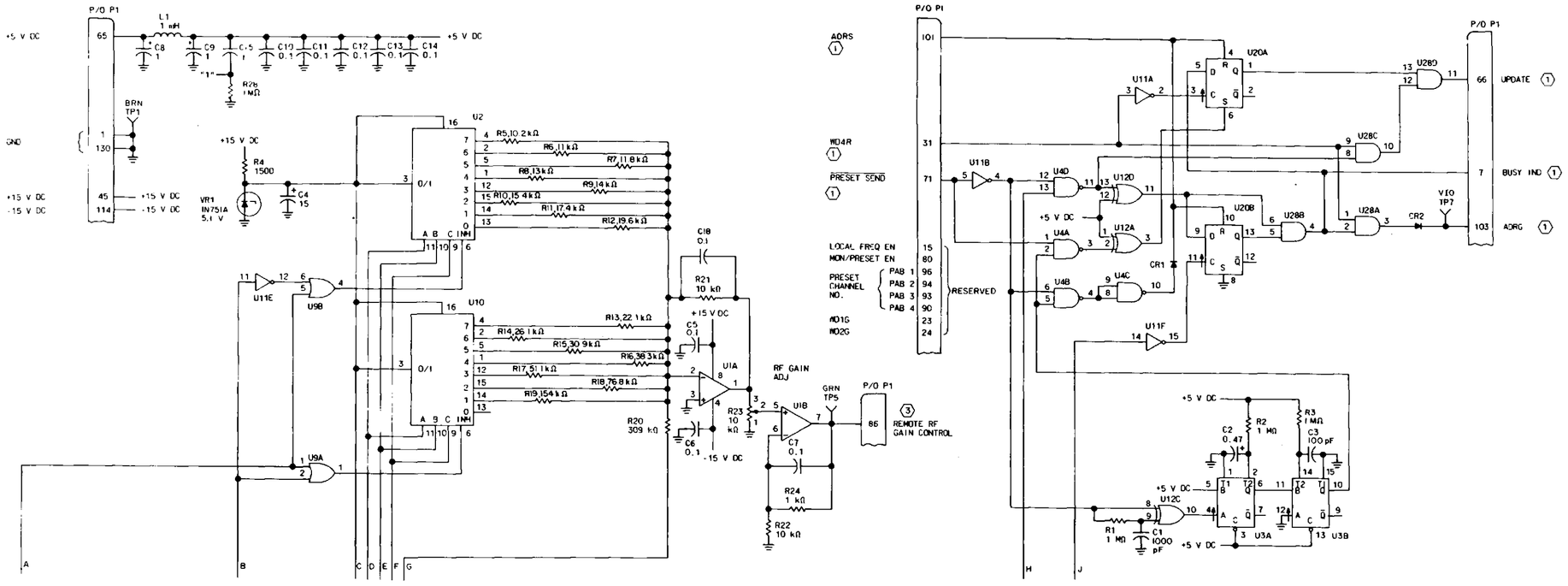
Parallel Output (635-0752-001), Schematic Diagram
Figure 7 (Sheet 5)

POWER AND GROUND CONNECTIONS

U NO	TYPE	POWER (V DC)	
		+5	GND
U1	MC1458P1		
U2, U7, U10	F4051PC	16	8,7
U3	MC14528BCP	16	8
U4	MC14011CP	14	7
U5, U17, U20	F4013BPC	14	7
U6, U13-U16, U18, U19, U21-U27, U29, U30	CD4094BE	16	8
U8	CD4047AE	14	7
U9	MC14071BCP	14	7
U11	F4049BPC	1	8
U12	MC14070BCP	14	7
U18	MC14081BCP	14	7

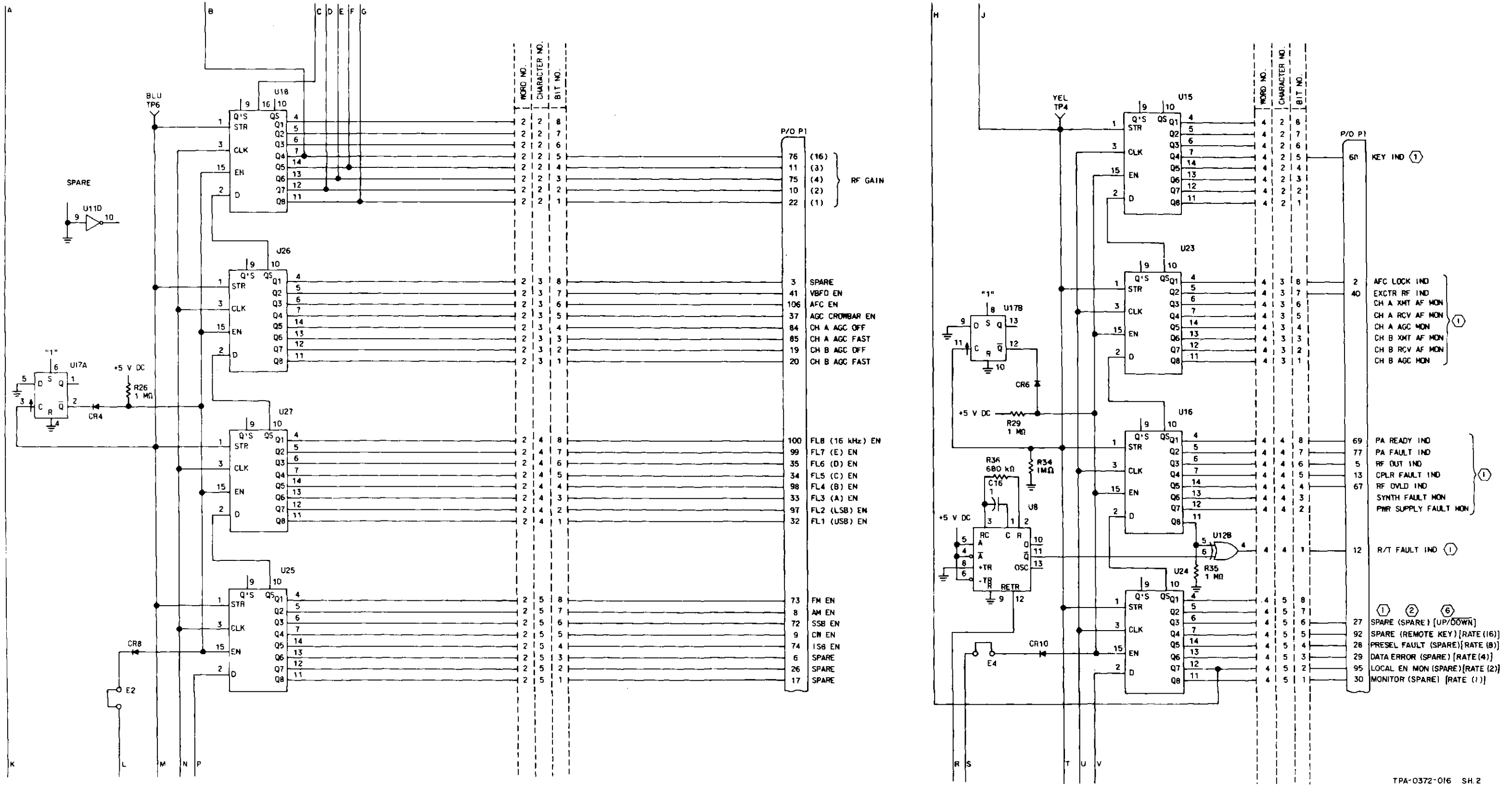
NOTES:

1. THESE FUNCTIONS ARE APPLICABLE ONLY TO RCVR CONTROL, EXCTR CONTROL, AND RCVR-EXCTR CONTROL.
2. FUNCTIONS IN PARENTHESES ARE APPLICABLE TO RCVR, EXCTR, AND RCVR-EXCTR. FOR A EXCTR, CHARACTER NO. LABELS SHOULD BE CHANGED FROM 5 TO 2.
3. THESE FUNCTIONS ARE APPLICABLE ONLY TO RCVR, EXCTR, AND RCVR-EXCTR
4. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS AND DIODES ARE TYPE 1N4454.
5. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
6. FUNCTIONS IN BRACKETS [ ] ARE APPLICABLE ONLY TO 8515-( ) RCVR
7. NONSTANDARD ABBREVIATIONS
   CH = CHANNEL
   EN = ENABLE

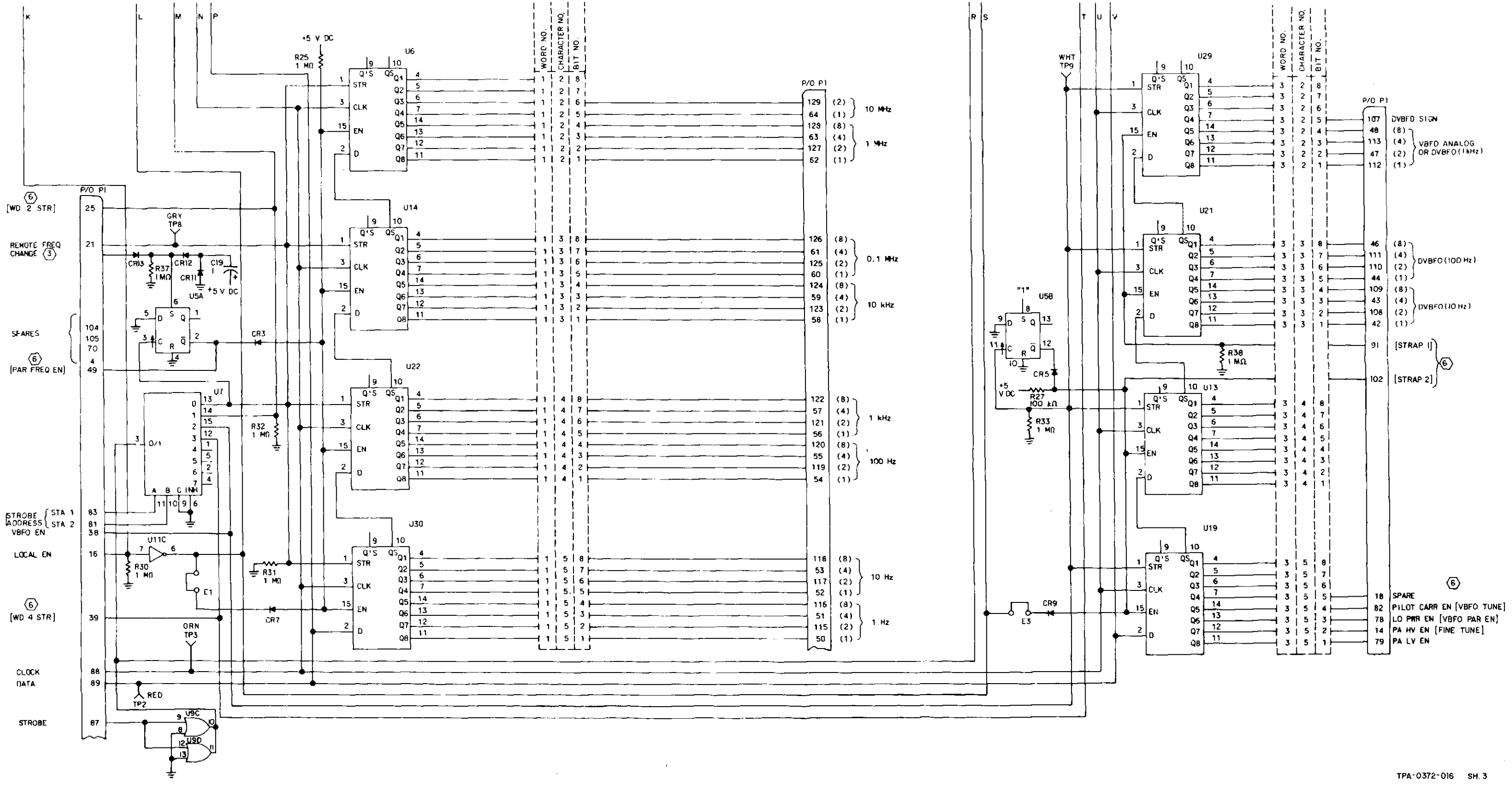


TPA-0372-016 SH.1

Parallel Output (635-0752-002), Schematic Diagram
Figure 7 (Sheet 6)



Parallel Output (635-0752-002), Schematic Diagram
Figure 7 (Sheet 7)



TPA-0372-016 SH. 3

Parallel Output (635-0752-002), Schematic Diagram
Figure 7 (Sheet 8)

Serial Interface (635-0742-001)

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

523-0767951-201211
1 June 1977
2nd Revision, 1 January 1979

1. DESCRIPTION

Serial Interface 635-0742-001, shown in figure 1, is a 2-layer planar card with a 56-pin edge-on connector (2 layers, 28 pins each).

The serial interface card consists of two primary circuits, a serial data receive circuit and a serial data transmit circuit.

In the serial data receive circuit are a receiver, an FSK decoder, a data UAR/T (universal asynchronous receiver/transmitter), an error detector, a word subaddress latch, an output parallel-to-serial shift register, a strobe decoder, and a bit/baud rate and clock generator.

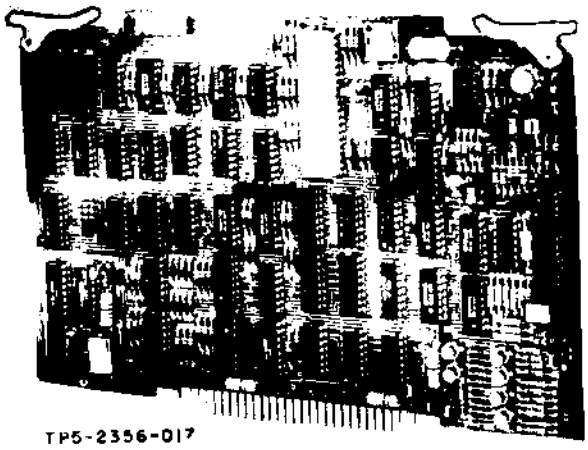
In the serial data transmit circuit are a data multiplexer, a data strobe generator, a bit/baud rate and clock generator, a data UAR/T, an FSK keyer, and an RS-232C driver.

2. PRINCIPLES OF OPERATION

2.1 General (Refer to figure 2.)

As a serial data receiver, the serial interface card receives FSK, RS-232C or MIL-STD-188C serial data control signals and checks for address, command status, and data errors. It then provides error, clock, word subaddress, strobe, and serial data outputs for decoding by a parallel output card.

As a serial data transmitter, the serial interface card receives parallel data inputs and a transmit word initiate and provides FSK, RS-232C, or MIL-STD-188C serial data monitor signals. The serial data monitor signals are supplied to the associated unit/control.

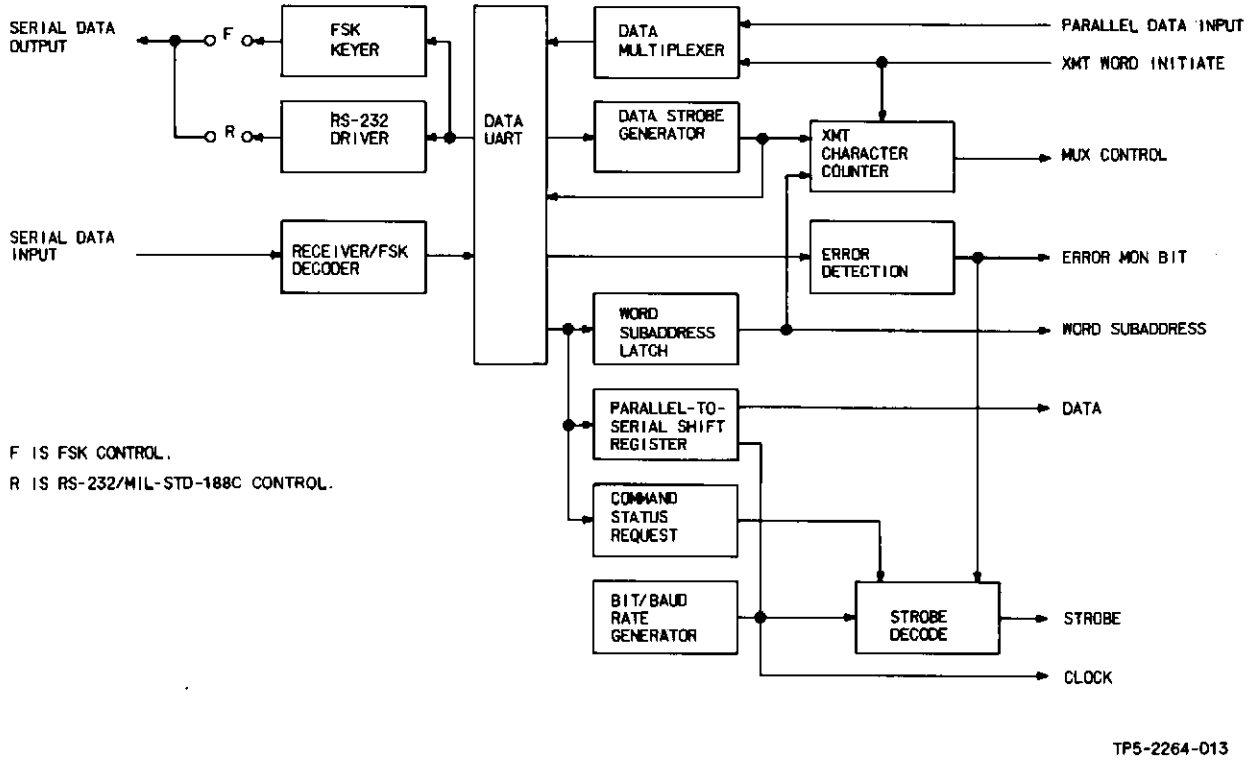


Serial Interface
Figure 1

2.2 Serial Data Inputs and Outputs

When strapped accordingly, the serial interface card receives and transmits any of the following types of control techniques.

a. FSK (mark = 1280 Hz, space = 2133 Hz) with mark equivalent to logic 1 data and space equivalent to logic 0 data. Data supplied at 75, 150, 300, or 600 bauds.
b. EIA RS-232C (mark = -6 ±1 V dc, space = +6 ±1 V dc) with mark equivalent to logic 1 data and space equivalent to logic 0 data. Using an EIA RS-232C processor, data supplied at 1200, 2400, 4800, 9600, or 19,200 bauds.
c. MIL-STD-188C (mark = +6 ±1 V dc, space = -6 ±1 V dc) with mark equivalent to logic 1 data and space equivalent to logic 0 data. Using a MIL-STD-188C control, data supplied at 75, 150, 300, 600, or



Simplified Block Diagram
Figure 2

1200 bauds. Using a MIL-STD-188C processor, data supplied at 1200, 2400, 4800, 9600, or 19,200 bauds.

Each control word is composed of five 11-bit characters. The last two bits of each character group are stop and parity bits. The first bit is a start bit. The first character of each control word is reserved for equipment address, word identification (subaddress), and word sync information. Bits seven and eight of the second character in each word are reserved for command and status request. The remaining characters of each word carry frequency, control, and monitor information.

Refer to figure 3. Control (and monitor) word timing is accomplished by a crystal-controlled oscillator on the serial interface card. A divider reduces the frequency to the desired values. Strapping permits selection of the baud rate for clock inputs to the various circuits. Selection is from 75, 150, 300, 600, 1200, 2400, 4800, 9600, and 19,200 bauds.

Refer to figure 4. Monitor data (serial data input) is applied to a serial data processor on the serial interface card. Word and status information is decoded from the monitor data and is used to determine strobe address information. The monitor data is then

applied to the data input of four word serial-to-parallel converters on the associated parallel output card. Each serial-to-parallel converter is enabled before it accepts and processes the monitor data. This occurs when the strobe address input is decoded and an enable signal is generated by the word enable circuit.

Refer to figure 4. Control information (serial data output) is stored in the multiplexers on the associated parallel input card. Word gate outputs are applied to the mux (multiplexer) address generator, located on the serial interface card. This generator uses the word gate information that is applied back to the multiplexers on the associated parallel input card. The mux address information enables the applicable multiplexer, which shifts the stored parallel information to the serial interface card that shifts the serial data through the FSK keyer or RS-232C driver circuit to the control bus.

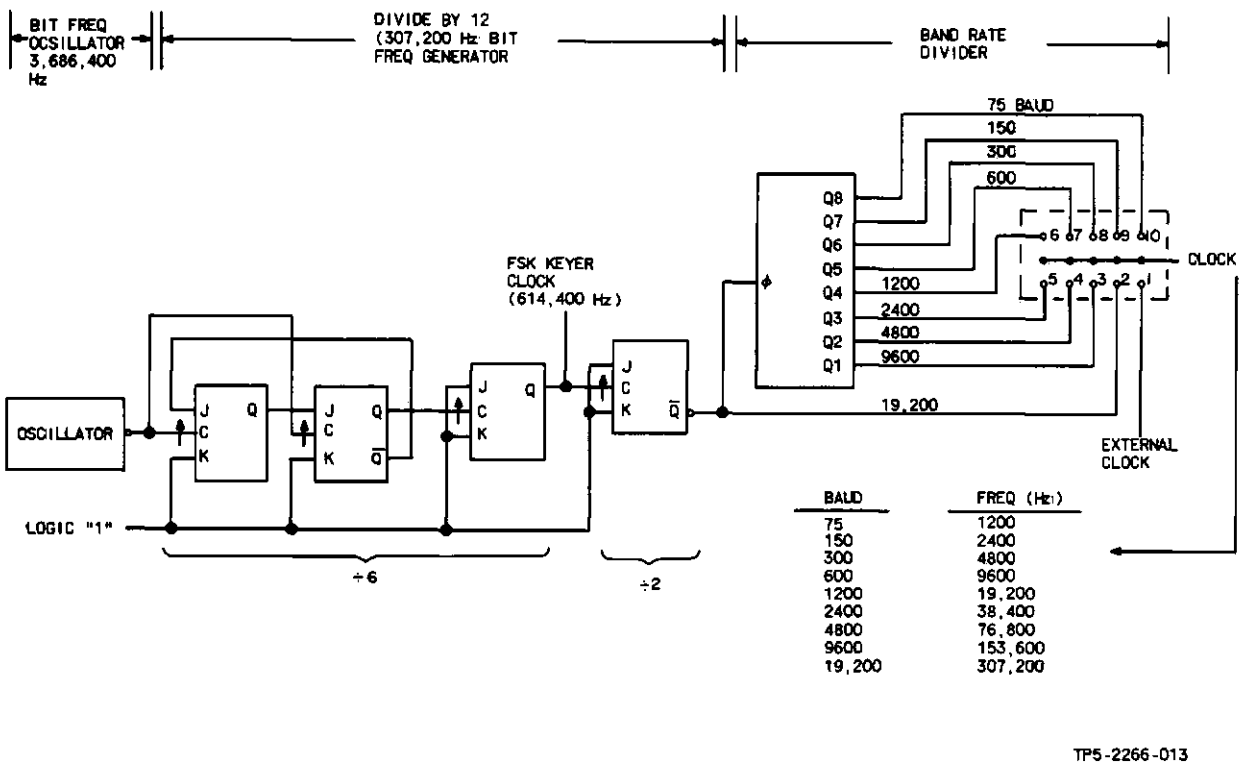
2.3 *Monitor Data (Refer to figure 4.)*

Monitor data (serial data input) is received by a line receiver and applied, through the FSK demodulator (if FSK strapped), to the UAR/T).

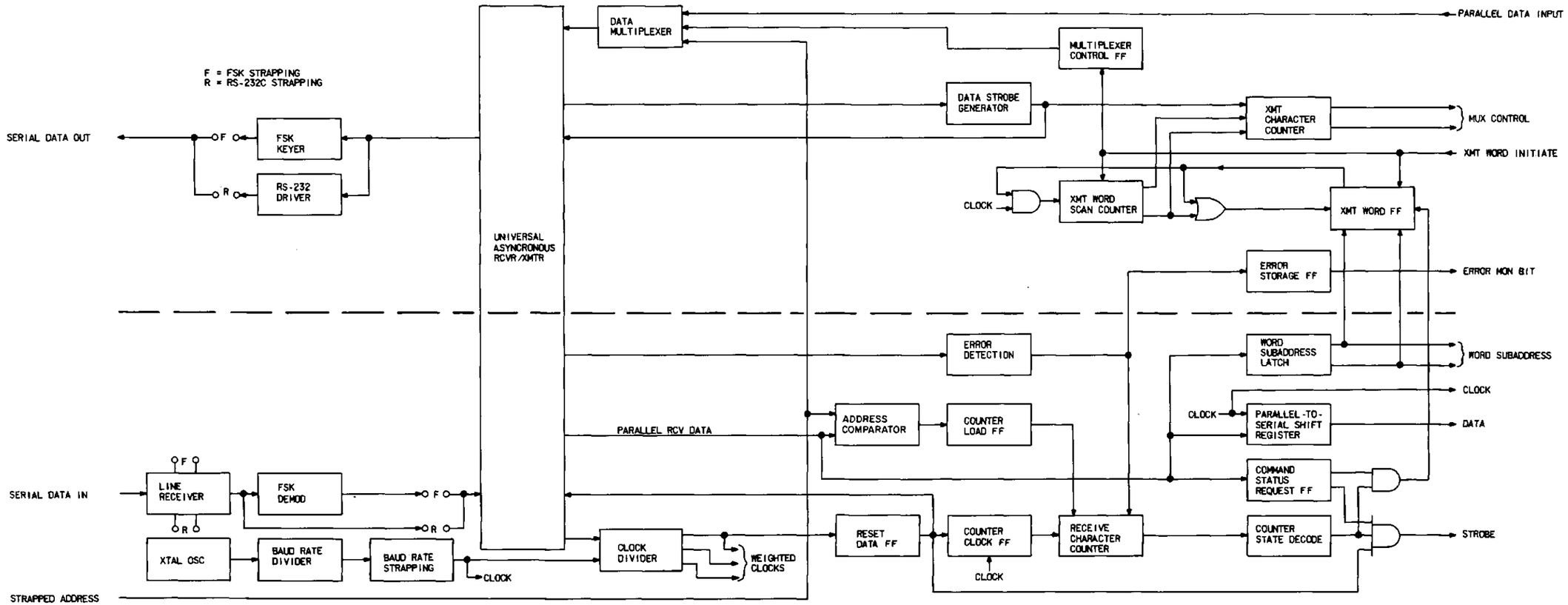
In FSK, the line receiver applies the received FSK signal to the FSK demodulator where a 1280-Hz signal is converted to a logic 1 output and a 2133-Hz signal is converted to a logic 0 output.

In RS-232C or MIL-STD-188C operation, the line receiver converts a +6-V dc input to a logic 0 (ground) output and converts a -6-V dc input to a logic 1 (+4.7-V dc) output.

The UAR/T receives the monitor data input, converts the data word to receive data outputs (RD1 through RD8), and clocks the serial data into the appropriate storage registers on the parallel output card. From the UAR/T, parallel receive data is supplied to the address comparator for comparison to the strapped address. The output of the address comparator enables/disables the receive character counter. The command status is controlled also by the received parallel data. If the command status is enabled, it provides an enable signal to the strobe. With the command status, receive character, and reset data signals applied, a strobe is supplied and data is accepted into the appropriate storage register in the associated parallel output card as determined by the word sub-address.



Bit and Baud Rate Generator
Figure 3



TP5-2265-014

Block Diagram
Figure 4

2.4 Control Data (Refer to figure 4.)

Control data (serial data output) is transmitted by an FSK keyer (for FSK operation) or by a line driver (for RS-232C or MIL-STD-188C operation).

In FSK, the FSK keyer is strapped and converts logic 0 outputs from the UAR/T to 1280-Hz FSK signal and logic 1 outputs from the UAR/T to 2133 Hz.

In RS-232C or MIL-STD-188C operation, the line driver converts logic 0 inputs to the line driver to +6 V dc and logic 1 inputs to the line driver to -6 V dc.

Parallel input data are address selected and applied to the UAR/T, and supplied as serial output (so) data to the line driver or FSK keyer. The serial data is converted to the appropriate signal data and supplied to the associated remote unit/control.

2.5 Purpose of Strapping

2.5.1 FSK Control (F Straps)

All straps marked "F" are in place. All straps marked "R" or "MIL" are removed. Baud rate is strapped for 75, 150, 300, or 600 bauds (same as associated unit control).

a. Strap between J1-54 and resistor R7 provides a 600-ohm load between J1-54 and J1-55.
b. Strap between C2 and R3 completes circuit to noninverting input of U34A to allow balanced ac (FSK) operation.
c. Strap between R1 and R2 paralleling these resistors makes inverting input load approximately equal to the noninverting input load.
d. Strap between U34A-2 to R6 provides degenerative feedback to U34A opamp.
e. Strap between CR1-anode to R78 provides a positive clipper for the FSK signal.
f. Strap between U12-7 and U20B-5 connects the FSK demodulator output to the UAR/T input.
g. Strap between J1-26 and C48 connects the FSK keyer output to the control data line.

2.5.2 RS-232C Control (R Straps)

All straps marked "R" are in place. All straps marked "F" or "MIL" are removed. Baud rate is strapped at any rate (same as associated unit/control).

a. Strap between J1-54 and R2 provides direct dc connection to opamp U34A.
b. Strap between J1-55 and ground provides reference for monitor data return.
c. Strap between U34A-3 and R4 provides reference for U34A noninverting input.
d. Strap between U34A-3 and R6 provides degenerative feedback to U34A opamp.
e. Strap between U20B-5 and R78 connects line receiver output to UAR/T input for RS-232C or MIL-STD-188C operation.
f. Strap between J1-26 and CR14-anode connects RS-232C driver output to control data line.
g. Strap between J1-27 and ground provides reference for control data return.

2.5.3 MIL-STD-188C Control (MIL Strap and R Straps)

All straps marked "R" are in place (see paragraph 2.5.5) and one strap marked "MIL" is in place. All straps marked "F" are removed. Baud rate is strapped at any rate (same as associated unit/control).

a. Strap between U9D-13 and ground inverts serial inputs to and serial outputs from UAR/T allowing application of MIL-STD-188C signals.

2.5.4 Parity

2.5.4.1 Odd Parity (O Strap)

Strapped between CR3-cathode and ground to recognize odd parity inputs.

2.5.4.2 Even Parity (E Strap)

Strapped between CR3-anode and ground to recognize even parity inputs.

2.5.4.3 No Parity

O and E straps are removed when input parity is insignificant.

2.5.5 Test Strap (Y Strap)

Strap between U20C-9 and U52B-6 removed for test purposes. Strap in place for normal operation.

2.5.6 Address Recognition (A Strap)

Strap between U5B-4 and U1A-8 provides address recognition. Serial interface card recognizes data inputs only if address input matches the address strapping provided by the unit/control in which the serial interface card is installed.

2.5.7 Baud Rate

Strap for applicable baud rate as follows:

a. 75 bauds — strap between baud pin 10 and center pin.
b. 150 bauds — strap between baud pin 9 and center pin.
c. 300 bauds — strap between baud pin 8 and center pin.
d. 600 bauds — strap between baud pin 7 and center pin.
e. 1200 bauds — strap between baud pin 6 and center pin.
f. 2400 bauds — strap between baud pin 5 and center pin.
g. 4800 bauds — strap between baud pin 4 and center pin.
h. 9600 bauds — strap between baud pin 3 and center pin.
i. 19,200 bauds — strap between baud pin 2 and center pin.
j. External bauds — strap between baud pin 1 and center pin. External baud may be any between 75 and 19,200 bauds (baud is 1/16 of applied frequency).

2.5.8 Spares (S Straps)

S straps have no associated electrical circuits. They are used only for storing unused straps.

2.6 Presettable Up/Down Counter CD4029A (Refer to figure 5.)

The CD4029A consists of a 4-stage binary or bcd decade presettable up/down counter with provisions for look-ahead carry in both counting modes.

A high preset enable signal allows information on the jam inputs to preset the counter to any state asynchronously with the clock. A low on each jam line, when the preset enable is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the carry-in and preset enable signals are low. Advancement is inhibited when the carry-in or preset enable signals are high. The carry-out signal is normally high and goes low when the counter reaches its maximum count in the up mode or the minimum count in the down mode, provided the carry-in signal is low. The carry-in signal in the low state can thus be considered a clock-enable. The carry-in terminal must be connected to V_{SS} when not in use.

Binary counting is accomplished when the binary/decade input is high; the counter counts in the decade mode when the binary/decade input is low. The counter counts up when the up/down input is high, and down when the up/down input is low.

2.7 Exclusive OR Gate CD4030A (Refer to figure 6.)

Exclusive OR gate CD4030A consists of four 2-input exclusive OR gates in a package. The exclusive OR gate is commonly used as a pulse generator similar to that shown in figure 6.

2.8 8-Stage Shift Register CD4021A (Refer to figure 7.)

The CD4021A is an 8-stage parallel or serial-input/serial-output shift register having common clock and parallel/serial control inputs, a single serial data input, and individual parallel jam inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. Q outputs are available from the sixth, seventh, and eighth stages.

When the parallel/serial control input is low, data is serially shifted into the 8-stage register synchronously with the positive-going transition of the clock pulse.

When the parallel/serial control input is high, data is jammed into the 8-stage register via the parallel input lines asynchronously with the clock line.

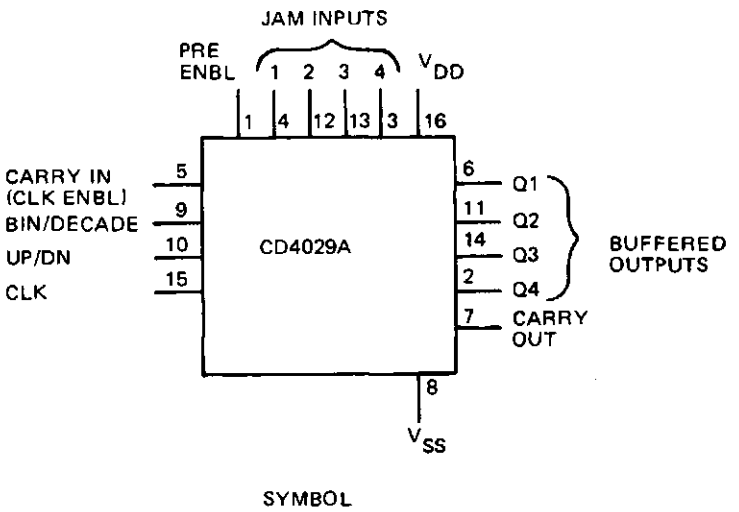
2.9 Dual D-Type Flip-Flop CD4013A (Refer to figure 8.)

The CD4013A consists of two identical, independent, data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset input, respectively.

2.10 UAR/T AY-5-1013

2.10.1 General (Refer to figure 9 and to table 1.)

The UAR/T is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, five to eight data bits,



CHARACTERISTICS

V_{DD}: +3 TO +15 V DC
V_{SS}: 0 V

OUTPUT VOLTAGE:
LOW LEVEL: V_{SS} +0.05 V DC MAX.
HIGH LEVEL: V_{DD} −0.05 V DC MIN.

CLK FREQ: 2.5 MHz TYP (WITH V_{DD} AT +5 V DC)
5.0 MHz TYP (WITH V_{DD} AT +10 V DC)

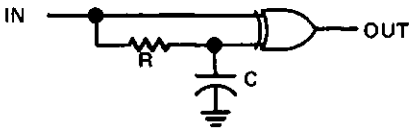
TP5-2267-011

Presettable Up/Down Counter CD4029A
Figure 5

2–INPUT
EXCLUSIVE OR GATE

INPUTS		OUTPUT
A	B	0
0	0	0
1	0	1
0	1	1
1	1	0

PULSE GENERATOR

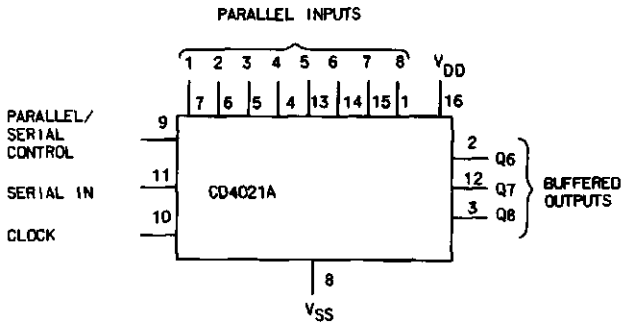


INPUT	OUTPUT	
0	0	
1	0	
0 → 1	⎍	NOTE 1
1 → 0	⎍	NOTE 1

NOTE:
1. PULSE WIDTH DEPENDANT ON VALUE OF R AND C.

TP5-2268-011

Exclusive OR Gate CD4030A
Figure 6



CHARACTERISTICS

V_{DD}: +3 TO +15 V DC

V_{SS}: 0 V

OUTPUT VOLTAGE:

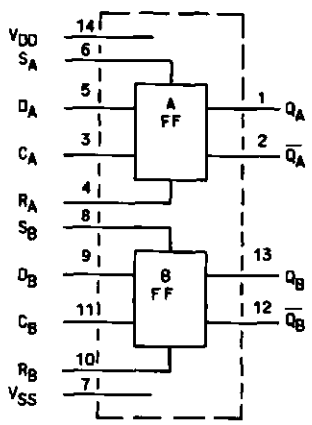
LOW LEVEL: V_{SS} +0.05 V DC MAX.

HIGH LEVEL: V_{DD} -0.05 V DC MIN.

CLOCK FREQ: 2.5 MHz TYP (WITH V_{DD} AT +5 V DC)
5.0 MHz TYP (WITH V_{DD} AT +10 V DC)

TP5-2269-014

8-Stage Static Shift Register CD4021A
Figure 7



TRUTH TABLE

C	D	R	S	Q	$\overline{Q}$	
0 ↗ 1	0	0	0	0	1	
0 ↗ 1	1	0	0	1	0	
1 ↘ 0	X	0	0	Q	$\overline{Q}$	NO CHANGE
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

X = EITHER 1 OR 0

CHARACTERISTICS

V_{DD} : +3 TO +15 V DC

V_{SS} : 0 V

OUTPUT VOLTAGE:
LOW LEVEL: V_{SS} +0.05 V DC MAX.

HIGH LEVEL: V_{DD} -0.05 V DC MIN.

CLOCK FREQ: 4 MHz TYP (WITH V_{DD} AT +5 V DC)
10 MHz TYP (WITH V_{DD} AT +10 V DC)

TP5-2270-014

Dual D-Type Flip-Flop CD4013A
Figure 8

one or two stop bits, and either odd/even parity or no parity. In order to make the UAR/T universal, the baud, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip. All inputs and outputs are directly compatible with MTOS/MTNS logic, and also with TTL/DTL/CMOS logic without the need for interfacing components. All strobed outputs are 3-state logic.

2.10.2 Receiver Operation (Refer to figure 10.)

Power is applied, external reset is enabled, and clock pulse having a frequency of 16 times the desired baud is applied. The previous conditions will set data available (DAV) to a logic 0.

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter, making individual control bit setting unnecessary. Data reception starts when serial input signal changes from marking (logic 1) to spacing (logic 0), which initiates the start bit. The start bit is valid if, after transition from logic 1 to logic 0, the S1 line continues to be at logic 0 when center sampled, 8 clock pulses later. If, however, line is at a logic 1 when center sampling occurs, the start bit verification process will be reset. If the serial input line transitions from a logic 1 to a logic 0 (marking to spacing) when the 16X clock is in a logic 1 state, the bit time for center sampling will begin when the clock line transitions from a logic 1 to a logic 0 state. After verification of a genuine start bit, data bit reception, parity bit reception, and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s), the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip-flop and/or the framing error flip-flop to a logic 1. It should be noted that, if the no parity mode is selected, the PE (parity error) will be set unconditionally to a logic 0.

Once a full character is received, internal logic looks at the data available (DAV) signal to determine if data has been read out. If the DAV signal is at a logic 1, the receiver will assume data has not been read out and the overrun flip-flop of the status word holding register will be set to a logic 1. If the DAV signal is at a logic 0, the receiver will assume that data has been read out. After DAV goes to a logic 1, the receiver shift register is ready to accept the next character and has one full character time to remove the received character.

2.10.3 Transmitter Operation (Refer to figure 11.)

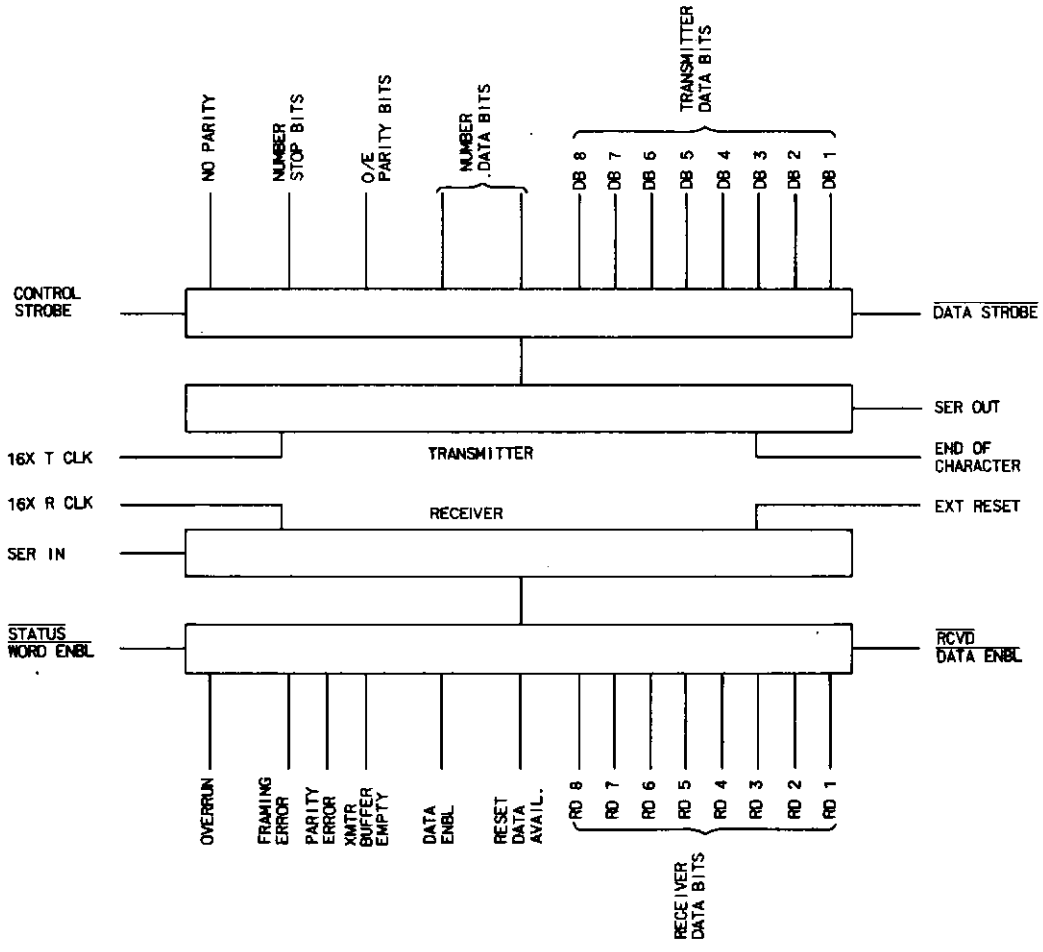
Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud. The above conditions will set TBMT, EOC, and SO to logic 1 (line is marking).

After initializing is completed, user may set control bits and data bits, with control bits selection normally occurring before data bits selection. However, one may set both DS and CS simultaneously if minimum pulse width specifications are followed. Once data strobe (DS) is pulsed, the TBMT signal will change from a logic 1 to a logic 0 indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and that the transmitter shift register is transmitting previously loaded data. TBMT will return to a logic 1. When the transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic 0, and EOC going to a logic 0, indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed, due to double buffering (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired), and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic 1, indicating that a new character is ready for transmission. This new character will be transmitted only if TBMT is a logic 0 as was previously discussed.

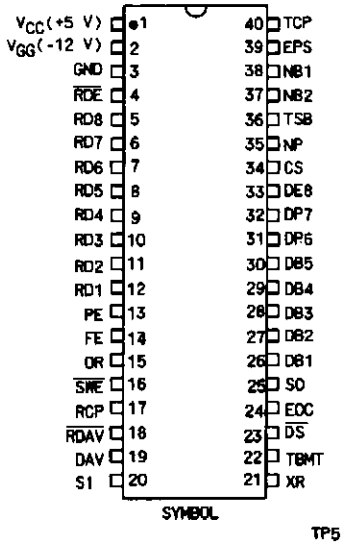
2.11 Phase-Locked Loop NE565A (Refer to figure 12.)

The NE565A phase-locked loop is a self-contained, adaptable filter and demodulator for the frequency range from 0.001 Hz to 500 kHz. The circuit is comprised of a vco, a phase detector, an amplifier, and a low-pass filter. The center frequency of the phase-locked loop is determined by the free-running frequency of the vco. The vco frequency is adjusted externally with a resistor or a capacitor. The low-pass filter that determines the capture characteristics of the loop is formed by an internal resistor and an external capacitor.



CHARACTERISTICS

V_{GG}: -12 V DC ±5%
V_{CC}: +5 V DC ±5%
INPUT LOGIC LEVELS: LOGIC 0, 0 TO +0.8 V DC;
LOGIC 1, V_{CC} -1.5 V DC TO V_{CC} +0.3 V DC
OUTPUT LOGIC LEVELS: LOGIC 0, NMT +0.4 V DC;
LOGIC 1, NLT V_{CC} -1.0 V DC
CLOCK FREQUENCY: DC TO 480 kHz
BAUD: 0 TO 30 k BAUD
CLOCK PULSE: 1.0 uS MIN.
CONTROL STROBE: 300 nS MIN.
EXTERNAL RESET: 500 nS MIN.
STATUS WORD ENABLE: 500 nS MIN.
RESET DATA ENABLE: 250 nS MIN.
RECEIVED DATA ENABLE: 500 nS MIN.
DATA STROBE: 190 nS MIN.



TP5-2271-D14

UAR/T AY-5-1013
Figure 9

Table 1. UAR/TAY-5-1013, Pin Functions.

PIN NO.	NAME (SYMBOL)	FUNCTION
1	V_{cc} power supply (V_{cc})	+5-V supply.
2	V_{GG} power supply (V_{GG})	-12-V supply.
3	Ground (V_{GD})	Ground.
4	Received data enable (RDE)	A logic 0 on the receiver enable line places the revised data onto the output lines.
5-12	Received data bits (RD8-RD1)	These are the eight data output lines. Received characters are right justified; the LSB always appears on RD1. These lines have tristate outputs; ie, they have the normal TTL output characteristics when ROE is 0 and a high impedance state when RDE is 1. Thus, the data output lines can be bus structure oriented.
13	Parity error (PE)	This line goes to a logic 1 if the received character parity does not agree with the selected parity. Tristate.
14	Framing error (FE)	This line goes to a logic 1 if the received character has no valid stop bit. Tristate.
15	Overrun (OR)	This line goes to a logic 1 if the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register. Tristate.
16	Status word enable (SWE)	A logic 0 on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. Tristate.
17	Receiver clock (RCP)	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud.
18	Reset data available (RDAV)	A logic 0 will reset the DAV line. The DAV F/F is only thing that is reset.
19	Data available (DAV)	This line goes to a logic 1 when an entire character has been received and transferred to the receiver holding register. Tristate.
20	Serial input (SI)	This line accepts the serial bit input stream. A marking (logic 1) to spacing (logic 0) transition is required for initiation of data reception.
21	External reset (XR)	Resets all registers except the received data register. Sets SO, EOC, and TBMT to a logic 1. Resets DAV, and error flags to 0. Clears input data buffer. Must be tied to logic 0 when not in use.

Table 1. UAR/T AY-5-1013, Pin Functions (Cont).

PIN NO.	NAME (SYMBOL)	FUNCTION
22	Transmitter buffer empty (TBMT)	The transmitter buffer empty flag goes to a logic 1 when the data bits holding register may be loaded with another character. Tristate.
23	Data strobe (DS)	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of DS. Data must be stable during entire strobe.
24	End of character (EOC)	This line goes to a logic 1 each time a full character is transmitted. It remains at this level until the start of transmission of the next character.
25	Serial output (SO)	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic 1 when no data is being transmitted.
26-33	Data bit inputs (DB1-DB8)	There are up to eight data bit input lines available.
34	Control strobe (CS)	A logic 1 on this lead will enter the control bits (EPS, BM1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic 1 level.
35	No parity (NP)	A logic 1 on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic 0.
36	Number of stop bits (TSB)	This lead will select the number of stop bits, one or two, to be appended immediately after the parity bit. A logic 0 will insert one stop bit and a logic 1 will insert two stop bits.
37-38	Number of bits/character (NB2, NB1)	These two leads will be internally decoded to select five, six, seven, or eight data bits/character. NB2 NB1 BITS/CHARACTER 0 0 5 0 1 6 1 0 7 1 1 8

Table 1. UAR/T AY-5-1013, Pin Functions (Cont).

PIN NO.	NAME (SYMBOL)	FUNCTION
39	Odd/even parity select (EPS)	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic 0 will insert odd parity and a logic 1 will insert even parity.
40	Transmitter clock (TCP)	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud.

2.12 Voltage Comparator LM311H (Refer to figure 13.)

The LM311H is a voltage comparator with extremely low input currents from a wide range of supply voltages. Its output is compatible with RTL, DTL, and TTL as well as MOS circuits. It can drive lamps or relays, switching voltages up to 40 volts at currents as high as 50 mA.

2.13 12-Stage Ripple-Carry Binary Counter/Divider CD4040A (Refer to figure 14.)

The CD4040A consists of an input-pulse-shaping circuit and 12 ripple-carry binary counter stages. Resetting the counter to the all-0's state is accomplished by a high level on the reset line. A master-slave flip-flop configuration is used for each counter stage. The state of the counter is advanced one step in binary order on the negative-going transition of the input pulse. All inputs and outputs are fully buffered.

2.14 7-Stage Binary Counter CD4024A (Refer to figure 15.)

The CD4024A consists of an input-pulse-shaping circuit, reset line driver circuit, and seven binary counter stages. The counter is reset to zero by a high level on the reset input. Each counter stage is a static master-slave flip-flop. The counter stage is advanced one count on the negative going transition of each input pulse.

2.15 Quad AND-OR Select Gate CD4019A (Refer to figure 16.)

The CD4019A consists of four AND-OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is made by control bits Ka and Kb. If Ka and Kb are applied simultaneously, a logical A + B function is accomplished.

2.16 Dual Binary Up Counters CD4520B (Refer to figure 17.)

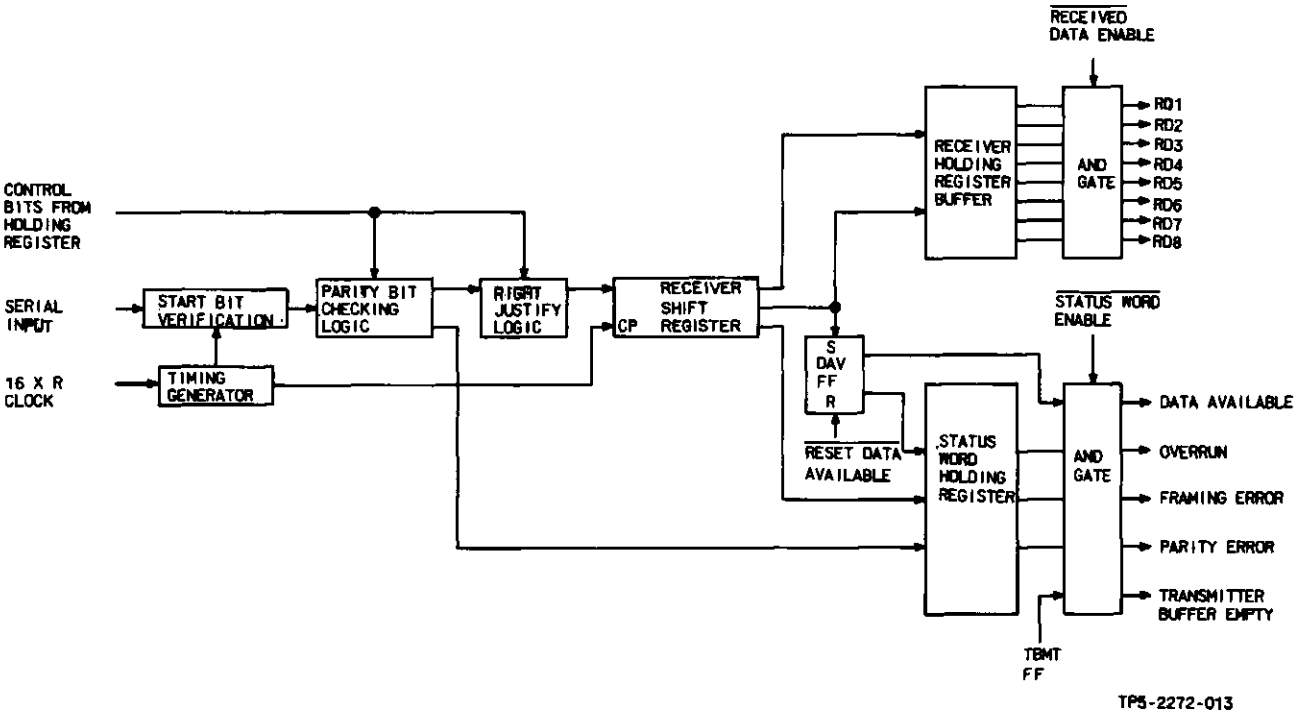
The CD4520B consists of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable clock and enable lines for incrementing on either the positive-going or negative-going transition. For single-unit operation, the enable input is maintained high and the counter advances on each positive-going transition of the clock. The counters are cleared by high levels on their reset lines.

2.17 Dual Operational Amplifier MC1458P1 (Refer to figure 18.)

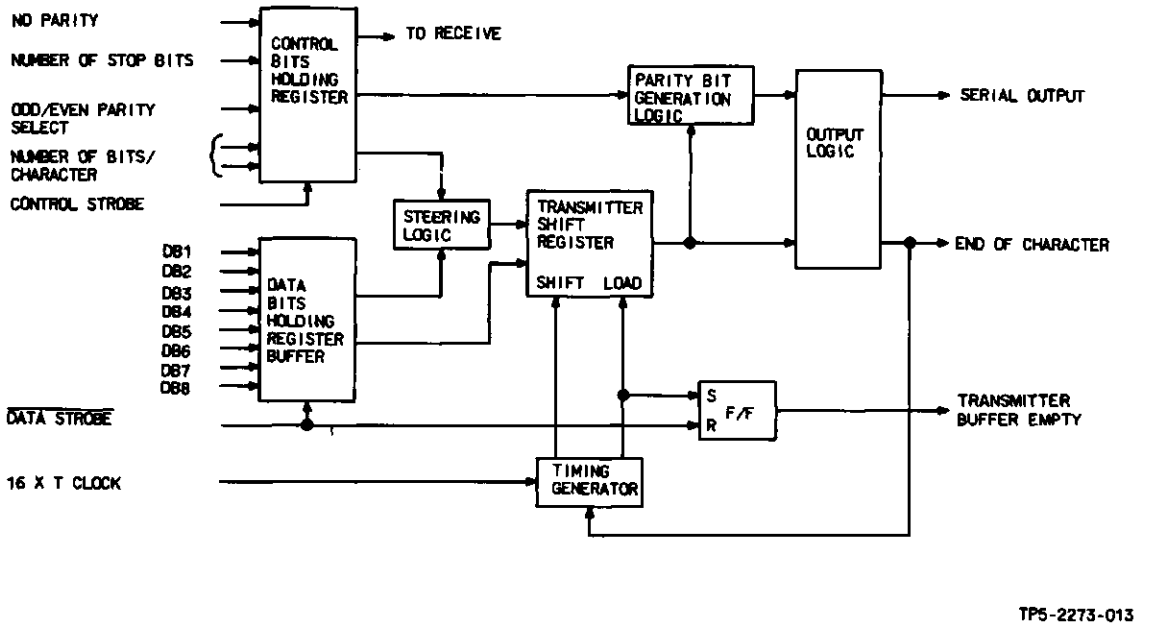
The MC1458P1 consists of two operational amplifiers in one package designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components.

2.18 Dual J-K Master-Slave Flip-Flop CD4027A (Refer to figure 19.)

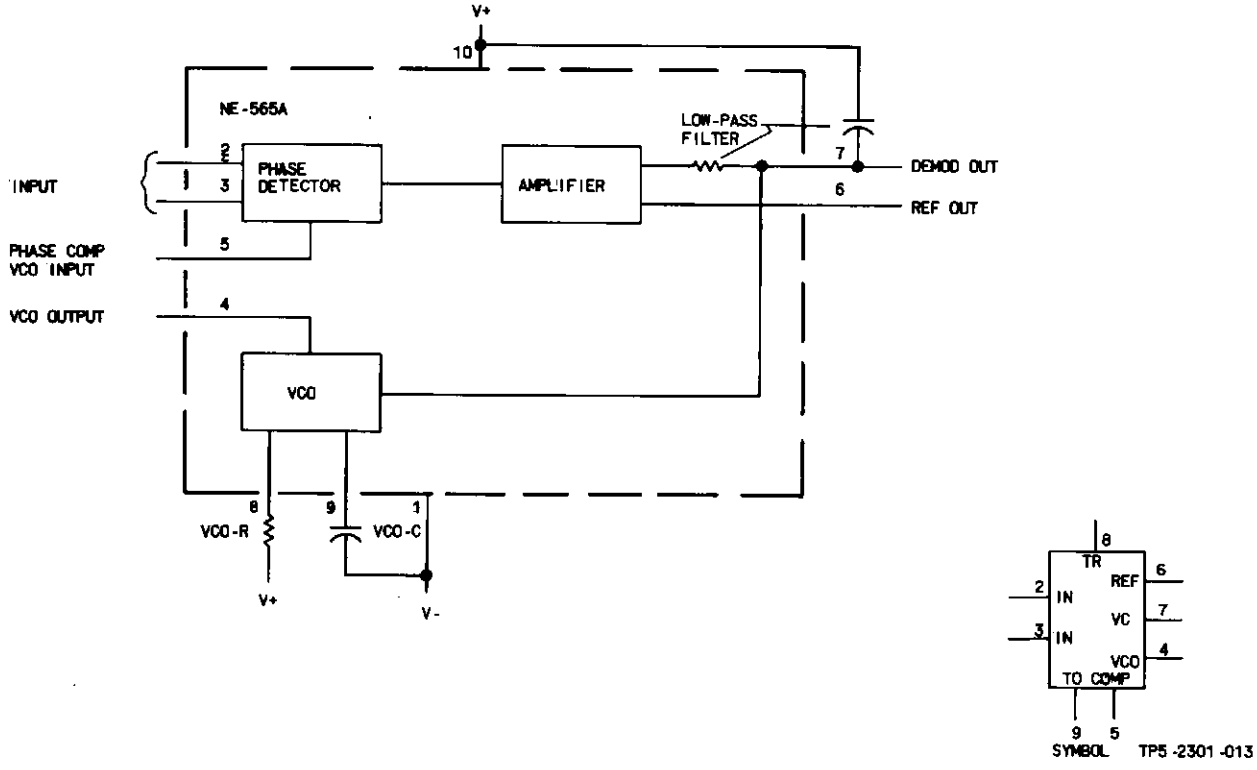
The CD4027A consists of two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has independent J, K, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for control, register, and toggle functions. Logic levels at the J and K inputs, along with internal



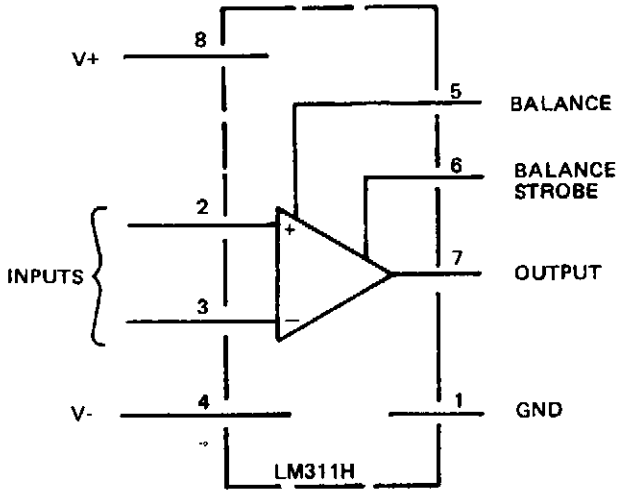
UAR/T Receiver, Block Diagram
Figure 10



UAR/T Transmitter, Block Diagram
Figure 11



Phase-Locked Loop NE565A
Figure 12



CHARACTERISTICS

SUPPLY VOLTAGE: V+ +30 V DC MAX, V− -30 V DC MAX, 40 V MAX BETWEEN V+ AND V−.

INPUT DIFF VOLTAGE: ±30 V MAX

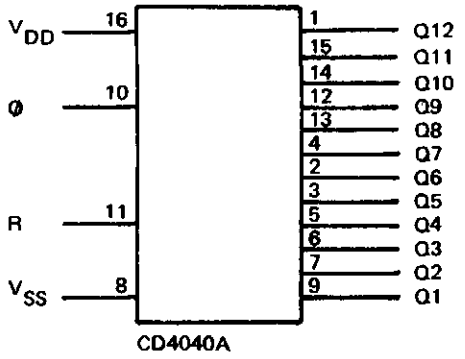
INPUT VOLTAGE: ± 15 V MAX

OUTPUT SHORT CIRCUIT DURATION: 10 s MAX

VOLTAGE GAIN: 200 TYPICAL

TP5-2302-011

Voltage Comparator LM311H
Figure 13



CHARACTERISTICS

V_{DD}: +3 TO +15 V DC

V_{SS}: 0 V

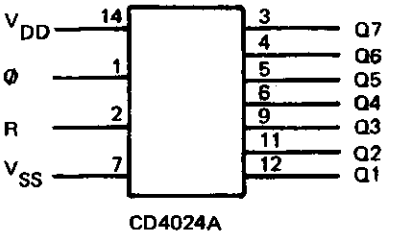
OUTPUT VOLTAGE:
LOW LEVEL: V_{SS} +0.05 V DC MAX.

HIGH LEVEL: V_{DD} −0.05 V DC MIN.

INPUT FREQ (Ø): 1.75 MHz TYPICAL (V_{DD} AT 5 V DC);
5.00 MHz TYPICAL (V_{DD} AT 10 V DC)

TP5-2303-011

12-Stage Ripple-Carry Binary Counter/Divider CD4040A
Figure 14



CHARACTERISTICS

V_{DD}: +3 TO +15 V DC

V_{SS}: 0 V

OUTPUT VOLTAGE:
LOW LEVEL: V_{SS} +0.05 V DC MAX.

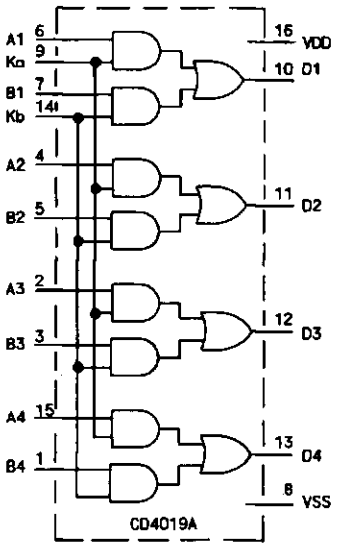
HIGH LEVEL: V_{DD} −0.05 V DC MIN.

INPUT FREQ (Ø): 2.5 MHz TYPICAL (V_{DD} AT 5 V DC);

7.00 MHz TYPICAL (V_{DD} AT 10 V DC)

TP5-2304-011

7-Stage Binary Counter CD4024A
Figure 15



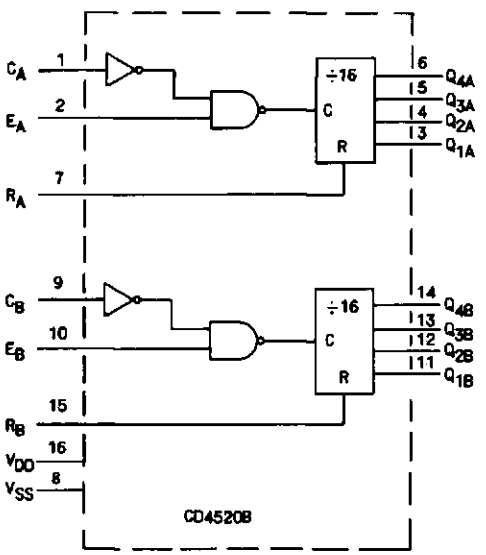
TRUTH TABLE

INPUTS				OUTPUT
A	Ka	B	Kb	D
0	0	0	0	0
1	0	0	0	0
0	1	0	0	0
1	1	0	0	1
0	0	1	0	0
1	0	1	0	0
0	1	1	0	0
1	1	1	0	1
0	0	0	1	0
1	0	0	1	0
0	1	0	1	0
1	1	0	1	1
0	0	1	1	1
1	0	1	1	1
0	1	1	1	1
1	1	1	1	1

CHARACTERISTICS
VDD: +3 TO +15 V DC
VSS: 0V
OUTPUT VOLTAGE:
LOW LEVEL: VSS +0.05 V DC MAX.
HIGH LEVEL: VDD - 0.05 V DC MIN.

TP5-2305-013

Quad AND-OR Select Gate CD4019A
Figure 16



CHARACTERISTICS

V_{DD}: +3 TO +18 V DC

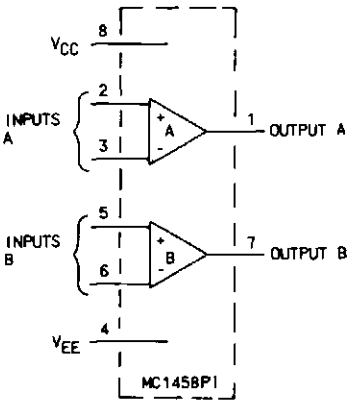
V_{SS}: 0 V

OUTPUT VOLTAGES:
LOW LEVEL: V_{SS} +0.05 V DC MAX.
HIGH LEVEL: V_{DD} -0.05 V DC MIN.

CLOCK FREQ:
1.5 MHz MAX (V_{DD} AT 5 V DC)
3 MHz MAX (V_{DD} AT 10 V DC)
4 MHz MAX (V_{DD} AT 15 V DC)

TP3-2306-013

Dual Binary Up Counters CD4520B
Figure 17

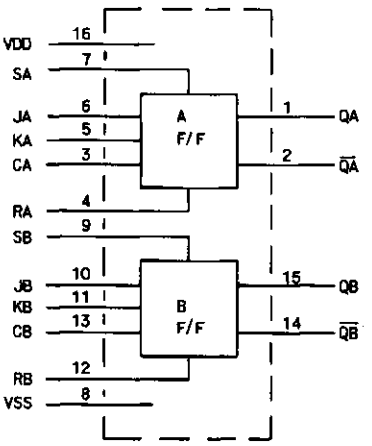


CHARACTERISTICS
SUPPLY VOLTAGE: V_{CC} +18 V DC MAX
V_{EE} -18 V DC MAX
INPUT DIFF VOLTAGE: ±30 V MAX
INPUT COMMON MODE VOLTAGE:
±15 V MAX (1)
OUTPUT SHORT CIRCUIT DURATION:
CONTINUOUS (2)
INPUT RESISTANCE: 300 kΩ MIN, 2.0 MΩ MAX
OUTPUT RESISTANCE: 75Ω TYPICAL
VOLTAGE GAIN: 15 MIN

NOTES:
(1) FOR SUPPLY VOLTAGE LESS THAN ±15.0 V, MAX INPUT VOLTAGE EQUAL TO SUPPLY VOLTAGE.
(2) SUPPLY VOLTAGE EQUAL TO OR LESS THAN 15 V.

TP5-2285-013

Dual Operational Amplifier MC1458P1
Figure 18



TRUTH TABLE

PRESENT STATE INPUTS J	K	S	R	OUTPUTS Q	C	NEXT STATE OUTPUTS Q	$\overline{Q}$	
1	X	0	0	0	↗	1	0	
X	0	0	0	1	↗	1	0	
0	X	0	0	0	↗	0	1	
X	1	0	0	1	↗	0	1	
X	X	0	0	X	↘			← NO CHANGE
X	X	1	0	X		1	0	
X	X	0	1	X	X	0	1	
X	X	1	1	X	X	1	1	

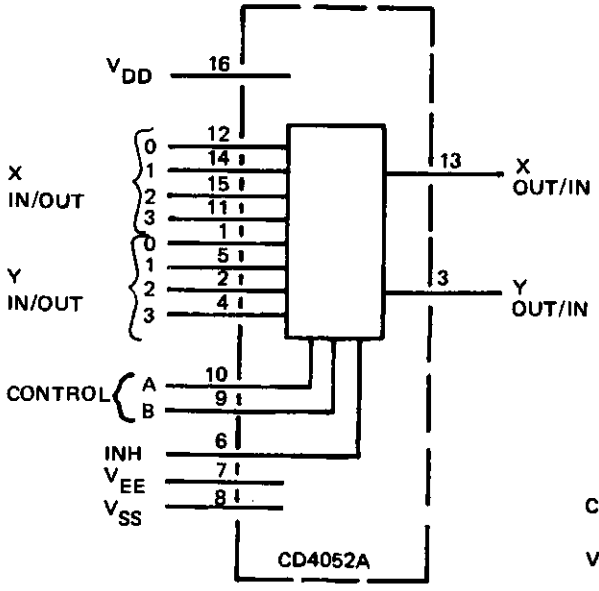
X = EITHER 1 OR 0

CHARACTERISTICS

VDD: +3 TO +15 V DC
VSS: 0V
OUTPUT VOLTAGE
LOW LEVEL: VSS +0.05 V DC MAX
HIGH LEVEL: VDD -0.05 V DC MIN
CLOCK FREQ:
3 MHz TYP (VDD AT +5 V DC)
8 MHz TYP (VDD AT +10 V DC)

TP5-2307-013

Dual J-K Master-Slave Flip-Flop CD4027A
Figure 19



TRUTH TABLE

INPUTS			OUTPUT
INHIBIT	A	B	X–Y
0	0	0	0X, 0Y
0	1	0	1X, 1Y
0	0	1	2X, 2Y
0	1	1	3X, 3Y
1	X	X	NONE

X=EITHER 1 OR 0

CHARACTERISTICS

V_{DD}: +3 TO +15 V DC

V_{SS}: 0 V

V_{EE}: –12 TO 0 V DC

ON RESISTANCE:

80 OHM (V_{DD} TO V_{EE} IS 15 V DC)
120 OHM (V_{DD} TO V_{EE} IS 10 V DC)
270 OHM (V_{DD} TO V_{EE} IS 5 V DC)

TP5-2308-011

Differential 4-Channel Multiplexer/Demultiplexer CD4052A
Figure 20

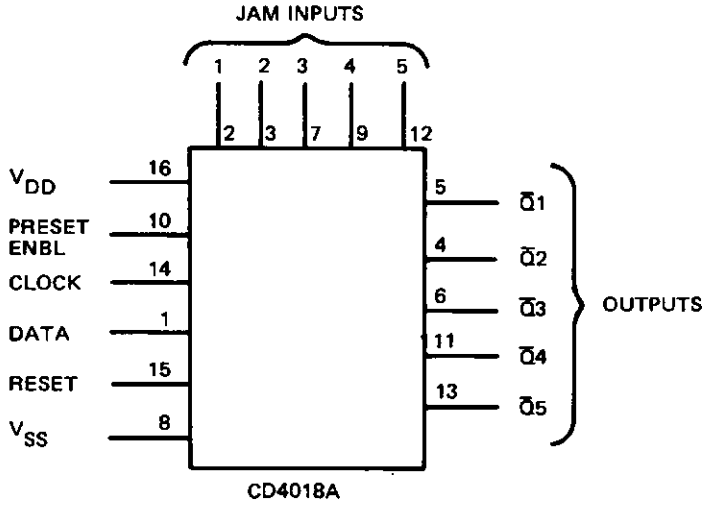
self-steering, control the state of each flip-flop. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset input, respectively.

2.19 Differential 4-Channel Multiplexer/ Demultiplexer CD4052A (Refer to figure 20.)

The CD4052A is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The binary control inputs select one of four pairs of channels to be turned on, and connect the differential analog inputs to the differential outputs.

2.20 Presettable Divide-by-N Counter CD4018A (Refer to figure 21.)

The CD4018A consists of five Johnson-counter stages, buffered $\overline{Q}$ outputs from each stage, and counter preset control gating. Clock, reset, data, preset enable, and five individual jam inputs are provided. A divide-by-10, -8, -6, -4, or -2 counter is implemented by feeding the $\overline{Q}5$, $\overline{Q}4$, $\overline{Q}3$, $\overline{Q}2$, and $\overline{Q}1$ signals, respectively, back to the data input. Divide-by-9, -7, -5, or -3 counter configurations are implemented by using an external gate package to properly gate the feedback connection to the data input. Divide-by functions greater than 10 can be achieved by use of multiple



CHARACTERISTICS

V_{DD}: +3 TO +15 V DC

V_{SS}: 0 V

OUTPUT VOLTAGE:
LOW LEVEL: V_{SS} +0.05 V DC
HIGH LEVEL: V_{DD} −0.05 V DC

CLOCK FREQ: 2.5 MHz TYP (V_{DD} AT +5 V DC)
5 MHz TYP (V_{DD} AT +10 V DC)

TP5-2309-011

Presettable Divide-by-N Counter CD4018A
Figure 21

CD4018A. The counter is advanced one count on a positive clock-signal transition. A high reset signal clears the counter to all zeros. A high preset-enable signal allows information on the jam inputs to preset the counter. Antilock gating is provided to assure the proper counter sequence.

3. TESTING AND TROUBLESHOOTING

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the serial interface card are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 2 check total performance of the serial interface card. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

Table 2. Serial Interface, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	**Note** These testing and troubleshooting procedures are based on using a control unit and an associated local unit. The most effective method of testing and troubleshooting is obtained by installing the questionable serial interface in the control unit. During these tests when a control unit is referred to it is a receiver-exciter control, an exciter control, or a receiver control. When a local unit is referred to it is a receiver-exciter, an exciter, or a receiver. a. Remove top cover of unit containing the serial interface to be tested. b. Remove serial interface. Install it on an extender card and place it in the control unit. c. Set unit LINE SELECTOR switches to 115 V. d. Connect units to 115-V ac power source and set power on. e. Measure dc voltages between the following pins and ground (TP1, brown):		
	J1-23 J1-28 J1-6	+15 ±1.0 V dc. +5 ±0.5 V dc. -15 +1.0 V dc.	Check associated power supply.
	f. Strap local unit for address 0. g. Connect local unit to a control unit.		
2. FSK data levels	**Note** F strap between J1-26 and C48 must be in place. R strap between J1-27 and ground must be removed. a. Connect an audio voltmeter between J1-26 and J1-27.		
(Cont)	b. Apply a ground to U10-2.		

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	c. Note audio voltmeter reading.	0 ±5 dB mW.	Check U34B and associated circuits.
	d. Remove U10-2 ground and apply ground to U10-3.		
	e. Note audio voltmeter reading.	Step c reading ±5 dB mW.	
	f. Remove U10-3 ground.		
3. Serial data command with status request	a. Set local unit front-panel CONT switch to REM.		
	b. Set control unit ADDRESS to 0.		
	Note Local unit is strapped for address 0 recognition. Address strap A must be installed.		
	c. Set control unit front-panel controls as follows: FREQUENCY KHZ to 29999.9 (0). MODE to SSB/CW or USB. BANDWIDTH to USB (receiver only). RF GAIN to full ccw (receiver and receiver-exciter only). AGC to FAST (receiver and receiver-exciter only). MIC to CH A (exciter and receiver-exciter only). KEY to NORM (exciter and receiver-exciter only). PA PWR to STBY (exciter and receiver exciter only). P CAR to OFF (exciter and receiver-exciter only). CONT to NORM.		
	d. Set control unit ADDRESS to 1.		
(Cont)	e. Change any and all of controls in step e.		

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	f. Note response signals on the control unit as follows:		
	EQUIPMENT STATUS indicators	No change in indications.	Check U3, U4, U5, and associated address circuits.
	BANDWIDTH indicators (receiver only).	No change in indications.	
	FREQUENCY KHZ indicators.	No change in indications.	
	g. Set control unit ADDRESS to 0.		
	h. Note response signals on the control unit as follows:		
	EQUIPMENT STATUS indicators.	No fault indications, MODE indicates USB (exciter and receiver-exciter), MODE indicates SSB/CW (receiver only).	Check U7, U6, U8, U9, U20, U21, U11, U12, U34, and associated circuits.
	BANDWIDTH indicators (receiver only).	Indicates U (USB).	
	FREQUENCY KHZ indicators.	Indicates 29999.9 (0) kHz.	
	Note Do not connect ground lead to J1-30 until frequency indication is normal (29999.9).		
	i. Connect a storage oscilloscope to TP6 (blue). Sweep time = 10 ms. Trigger = TRIGGER. Vert scale = 1 V per division. Horiz sweep = Normal. Display = STORE.		
	j. Connect a jumper from J1-30 to ground.	R/E FAULT indicator flashes at 0.5-Hz rate (2 s on, 2 s off).	
	k. On control unit, change any FREQUENCY KHZ control.	Oscilloscope display should look similar to command word with status request word 1 (refer to figure 22). Each frequency change changes data pattern.	Check U8, U28, U41, U29, U30, and associated circuits.
(Cont)			

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)		**Note** Without special equipment it is impossible to note exact waveform. Look at spacing and bits of data.	
	l. Erase scope and repeat step k as often as necessary to obtain a good result. **Note** 10-MHz and 1-MHz frequency controls change bit pattern of word 1, character 2. 100-kHz and 10-kHz frequency controls change bit pattern of word 1, character 3. 1-kHz and 100-Hz frequency controls change bit pattern of word 1, character 4. 10-Hz and 1-Hz frequency controls (if applicable) change bit pattern of word 1, character 5.		
	m. Erase scope. On control unit, change RF GAIN control position.	Oscilloscope display should look similar to command word with status request, word 2 (refer to figure 22). Each RF GAIN control changes data pattern. Refer to note of step k.	Same as step k.
	n. Erase scope and repeat step m as necessary to obtain a good result. **Note** RF GAIN control changes bit pattern of word 2, character 2. AGC switch changes bit pattern of word 2, character 3. VBFO enable switch (if applicable) changes bit pattern of word 2, character 3. BANDWIDTH control and/or MODE control changes bit pattern of word 2, character 4. MODE control changes bit pattern of word 2, character 5.		
(Cont)			

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	o. Erase scope. On control unit, change PA PWR control position.	Oscilloscope display should look similar to command word with status request word 3 (refer to figure 22.) Each PA PWR control change changes data pattern. Refer to note of step k.	Same as step k.
	p. Erase scope and repeat step o as often as necessary to obtain a good result. **Note** VBFO control (if applicable) changes bit pattern of word 3, character 2. DVBFO 1-kHz and sign controls (if applicable) change bit pattern of word 3, character 2. DVBFO 100-Hz and 10-Hz controls (if applicable) change bit pattern of word 3, character 3. PA PWR control changes bit pattern of word 3, character 5. P CAR switch changes bit pattern of word 3, character 5.		
	q. Erase scope. On control unit, change KEY control position.	Oscilloscope display should look similar to command word with status request word 4. (Refer to figure 22.) Each application or removal of a key changes data pattern. Refer to note of step k.	Same as step k.
	r. Erase scope and repeat step q as often as necessary to obtain a good result.		
	s. Remove jumper from J1-30 to ground.		
4. Serial data status only	a. Repeat steps 3.a. through 3.i.		Same as test 3.
	b. Set local unit front-panel controls as follows: FREQUENCY KHZ to 29999.9 (0). MODE to SSB/CW or USB.		
(Cont)	BANDWIDTH to USB (receiver only).		

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	RF GAIN to full ccw (receiver and receiver-exciter only).		
	AGC to FAST (receiver and receiver-exciter only).		
	MIC to CH A (exciter and receiver-exciter only).		
	KEY to NORM (exciter and receiver-exciter only).		
	PA PWR to STBY (exciter and receiver-exciter only).		
	P CAR to OFF (exciter and receiver-exciter only).		
	CONT to LCL.		
	c. Change any or all of the above front-panel controls on the control unit.		
	d. Note response signals on the control unit.	No changes.	
	e. Set control unit ADDRESS to 0.		
	f. Note response signals on the control unit as follows:		
	EQUIPMENT STATUS indicators.	No fault indications, mode indicates USB (exciter and receiver-exciter), mode indicates SSB/CW (receiver only), BUSY indicator is lit.	
	BANDWIDTH indicators (receiver only).	Indicates U (USB).	
	FREQUENCY KHZ indicators.	Indicates 29999.9 (0) kHz.	
	g. Connect a storage oscilloscope to TP6 (blue).		
	Sweep time = 20 ms. Trigger = INTERNAL. Vert scale = 1 V per division. Horiz sweep = SINGLE SWEEP. Display = STORE.		
	h. Note oscilloscope waveform.	Should look similar to status request only words (refer to figure 22).	
(Cont)			

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	i. Repeat steps g and h as often as necessary to obtain a good result.	**Note** Without special equipment it will be impossible to note exact waveform. Look at spacing and bits of data.	
5. Serial data status only (Cont)	a. Repeat steps 3.a through 3.i. b. Set local unit front-panel controls as follows: FREQUENCY KHZ to 29999.9 (0). MODE to SSB/CW or USB. BANDWIDTH to USB (receiver only). RF GAIN to full ccw (receiver and receiver-exciter only). AGC to FAST (receiver and receiver-exciter only). MIC to CH A (exciter and receiver-exciter only). KEY to NORM (exciter and receiver-exciter only). PA PWR to STBY (exciter and receiver-exciter only). P CAR to OFF (exciter and receiver-exciter only). CONT to LCL. c. Change any or all of the above front-panel controls on the control unit. d. Note response signals on the control unit. e. Set control unit ADDRESS to 0. f. Note response signals on the control unit as follows:	No changes.	Same as test 3.

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	EQUIPMENT STATUS indicators.	No fault indications mode indicates USB (exciter and receiver-exciter), mode indicates SSB/CW (receiver only), BUSY indicator is lit.	
	BANDWIDTH indicators (receiver only).	Indicate U (USB).	
	FREQUENCY KHZ indicators.	Indicates 29999.9 (0) kHz.	
	g. Connect a storage oscilloscope to TP5 (green). Sweep time = 20 ms. Trigger = INTERNAL. Vert scale = 1 V per division. Horiz sweep = SINGLE SWEEP. Display = STORE.		
	h. Note oscilloscope waveform.	Should look similar to monitor word(s)/command word(s) with no status request, (refer to figure 22). **Note** Without special equipment it will be impossible to note exact waveform. Look at spacing and bits of data.	
	i. Repeat steps g and h as often as necessary to obtain a good result.		
6. FSK receiver sensitivity	a. Connect local unit to a control unit through a 40-dB attenuator in both the monitor and data lines.		Check U34A and associated circuits.
	b. Repeat test 3.	Results should be same as test 3 results.	
7. Address recognition	a. Set local unit CONT switch to REM.		
	b. Set control unit ADDRESS to 0.		
	c. Set control unit front-panel controls as follows:		
(Cont)	FREQUENCY KHZ to 29999.9(9).		

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
7. (Cont)	MODE to SSB/CW or USB.		
	BANDWIDTH to USB (receiver only).		
	RF GAIN to full ccw (receiver and receiver-exciter only).		
	AGC to FAST (receiver and receiver-exciter only).		
	MIC to CH A (exciter and receiver-exciter only).		
	KEY to NORM (exciter and receiver-exciter only).		
	PA PWR to STBY (exciter and receiver-exciter only).		
	P CAR to OFF (exciter and receiver-exciter only).		
	CONT to NORM.		
	d. Note response signals on the control unit as follows:		
	EQUIPMENT STATUS indicators.	No fault indications mode indicates USB (exciter, receiver-exciter) or SSB/CW (receiver), PA READY might be lit (exciter, receiver-exciter only).	Check U7, U6, U8, U9, U20, U21, U11, U12, U34, and associated circuits.
	BANDWIDTH indicators (receiver only).	Indicates U (USB).	
	FREQUENCY KHZ indicators.	Indicates 29999.9(9) kHz.	
	e. Set control unit ADDRESS to 1.		
	f. Note response signals on the control unit as follows:		
	EQUIPMENT STATUS indicators.	EXCTR FAULT, RCV FAULT, or R/E FAULT indicator flashes at a 0.25-Hz rate (on 2 seconds, off 2 seconds). All other indications should remain the same.	Check U3, U4, U5, U27, U28, U29, U30, U8, and associated circuits. Check also busy circuit on parallel output.
(Cont)	BANDWIDTH indicators (receiver only).	No change from step d.	

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

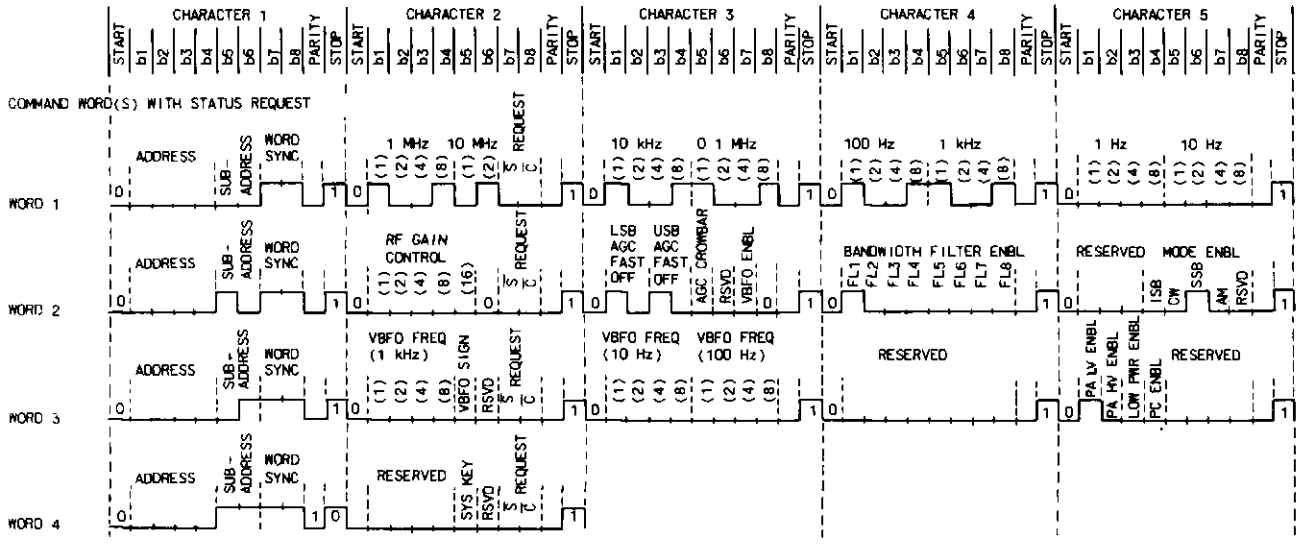
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
7. (Cont)	FREQUENCY KHZ indicators.	No change from step d.	Check U3, U4, U5, U27, U28, U29, U30, U8, and associated circuits. Check also busy circuit on parallel output.
	g. Note response signals on the control unit with the ADDRESS to each position 2 through 15.	Same as step f.	
8. Address	a. Set control unit ADDRESS to 0.		
	b. Ground serial interface pins J1-17 and J1-45.		
	c. Connect an oscilloscope to serial interface pin J1-13.		
	d. Change control unit ADDRESS through all positions 0 through 15 and back to 0 while watching oscilloscope.	A pulse is generated at J1-13 at every change in ADDRESS switch position.	Check U27 and associated circuits.
	e. Remove J1-17 and J1-45 grounds.		
9. Status request	a. Set local unit cont switch to REM.		
	b. Set control unit ADDRESS to 0.		
	c. Connect a dual-trace oscilloscope: One trace to TP6 (blue), and one trace to J1-24.		
	d. Apply a logic 1 pulse to oscilloscope trigger for both traces and A12TP7 (violet) simultaneously.		
	e. Note oscilloscope waveforms.	One trace (TP6) should look similar to status request only words 1 through 4 (refer to figure 22).	If TP6 abnormal check U8, U28, U29, U30, U41, and associated circuits.
		Other trace (J1-24) goes to logic 1 and remains there until status request only word 4 is transmitted and then returns to logic 0.	If J1-24 abnormal check U31, U50, U52, and associated circuits.
	f. Repeat steps c and d as often and as quickly as necessary to obtain a good result.	**Note** With local unit cont switch in LCL position J1-24 remains at logic 1.	

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
10. Word 4 continuous transmit	a. Set control unit ADDRESS to 0.		
	b. Set control unit CONT switch to NORM.		
	c. Connect oscilloscope to TP6 (blue). Sweep time = 20 ms. Trigger = INTERNAL. Vert scale = 1 V per division. Horiz sweep = NORMAL.	Continuous data monitored on oscilloscope should look similar to status request only word, word 4.	Check U37, U38, U48, U40, U41, U9, and associated circuits.
	d. Apply a ground to J1-30.	Continuous data on oscilloscope is terminated.	Check U17-U18, U19, U23, U24, U25, U26, and associated circuits.
	e. Remove J1-30 ground.		
11. Data loop back	a. Set control unit address to 0.		
	b. Disconnect control unit from local unit.		
	c. Set control unit CONT switch to TEST.		
	d. Connect a dual-trace storage oscilloscope with upper trace to TP6 (blue) and lower trace to TP5 (green).		
	e. Set oscilloscope as follows: Sweep time = 20 ms. Trigger = INTERNAL. Vert scale = 1 V per division. Horiz sweep = NORMAL.	Continuous data monitored on both traces of oscilloscope should look similar to status request only word, word 4, (refer to figure 27).	Check U47, U38, U48, U40, U41, U9, and associated circuits.
	f. Apply a ground to J1-30.	Continuous data on oscilloscope.	Same as step e.
	g. Set control unit front-panel controls as follows: FREQUENCY KHZ to 29999.0 (9). MODE to SSB/CW or USB. BANDWIDTH to USB (receiver only). RF GAIN to full ccw (receiver and receiver-exciter only). AGC to FAST (receiver and receiver-exciter only). MIC to CH A (exciter and receiver-exciter only). KEY to NORM (exciter and receiver-exciter only). PA PWR to STBY (exciter and receiver-exciter only). P CAR to OFF (exciter and receiver-exciter only).		
(Cont)			

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
11. (Cont)	h. Set oscilloscope display to STORE.		
	i. Erase display. Set FREQUENCY KHZ to 29999.9(9).	Both oscilloscope traces are identical and look similar to command word with status request, word 1. (Refer to figure 22.)	Same as step e.
	j. Erase display. Set MODE control to AM.	Both oscilloscope traces are identical and look similar to command word with status request, word 2. (Refer to figure 22.)	
	k. Erase display. Set PA PWR to HIGH PWR.	Both oscilloscope traces are identical and look similar to command word with status request, word 3. (Refer to figure 22.)	
	l. Erase display. Set KEY control to LOCK.	Both oscilloscope traces are identical and look similar to command word with status request, word 4. (Refer to figure 22.)	Same as step e.
	m. Set control unit CONT switch to NORM.		
	n. Repeat steps h through k.	Upper trace same as steps h through k. Lower trace, straight line.	
	o. Remove ground from J1-30.		
12. Baud rate check	a. Note baud rate strapped in unit.	Reference.	
	b. Strap baud rate for 75.		
	c. Repeat test 10.	Same as test 10 except monitor word spacing increases as baud rate decreases and vice versa.	Same as test 10.
	d. Strap baud rate for 19 200.		
	e. Repeat test 10.		
	f. Return to baud rate strapping referenced in step a.		



NOTES:

(1) RECEIVER-EXCITER CONTROL AND/OR RECEIVER-EXCITER SWITCH POSITIONS FOR THE TYPICAL WORDS SHOWN.

FREQUENCY kHz	- 29999.9
MODE	- USB
RF GAIN	- FULL CCW
AGC	- FAST
MIC	- CH A
KEY	- NORM
PA PWR	- STBY
P CAR	- OFF
CONT	- NORM (RECEIVER-EXCITER CONTROL) AND REM (RECEIVER-EXCITER), OR LCL (RECEIVER-EXCITER)

(2) FOR EXCITER CONTROLS AND/OR EXCITERS, ALL RECEIVE FUNCTIONS ARE LOGIC 0 BITS OF DATA.

(3) FOR RECEIVER CONTROLS AND/OR RECEIVERS, ALL EXCITER FUNCTIONS ARE LOGIC 0 BITS OF DATA.

TP5-4943-015

Command and Monitor Word Waveforms
Figure 22

4. ALIGNMENT/ADJUSTMENT

4.1 Control Data Strapping (Refer to figure 23.)

4.1.1 FSK Control

a. Remove all R and MIL straps.
b. Set all F straps in place.
c. Set Y strap in place.
d. Set baud rate straps in place. Set baud rate for 75, 150, 300, or 600 bauds (refer to paragraph 4.2).
e. If address recognition required, strap for address (refer to paragraph 4.5).
f. If parity recognition required, strap for parity (refer to paragraph 4.4).

4.1.2 EIA RS-232C Control

a. Remove all F and MIL straps.
b. Set all R straps in place.
c. Set Y strap in place.
d. Set baud rate straps in place, for any baud rate (refer to paragraph 4.2).
e. If address recognition required, strap for address (refer to paragraph 4.5).
f. If parity recognition required, strap for parity (refer to paragraph 4.4).

4.1.3 MIL-STD-188C Control

a. Remove all F straps.
b. Set all R straps in place.
c. Set MIL strap in place.
d. Set Y strap in place.
e. Set baud rate straps in place, for any baud rate (refer to paragraph 4.2).
f. If address recognition required, strap for address (refer to paragraph 4.5).
g. If parity recognition required, strap for parity (refer to paragraph 4.4).

4.2 Baud Rate Strapping

Strap for applicable baud rate as shown in table 3.

4.3 Test Strapping

For test purposes only, remove Y strap. For normal operation, Y strap must be set in place.

4.4 Parity Strapping

4.4.1 Odd Parity

For odd parity recognition, remove E strap and set O strap in place.

4.4.2 Even Parity

For even parity recognition, remove O strap and set E strap in place.

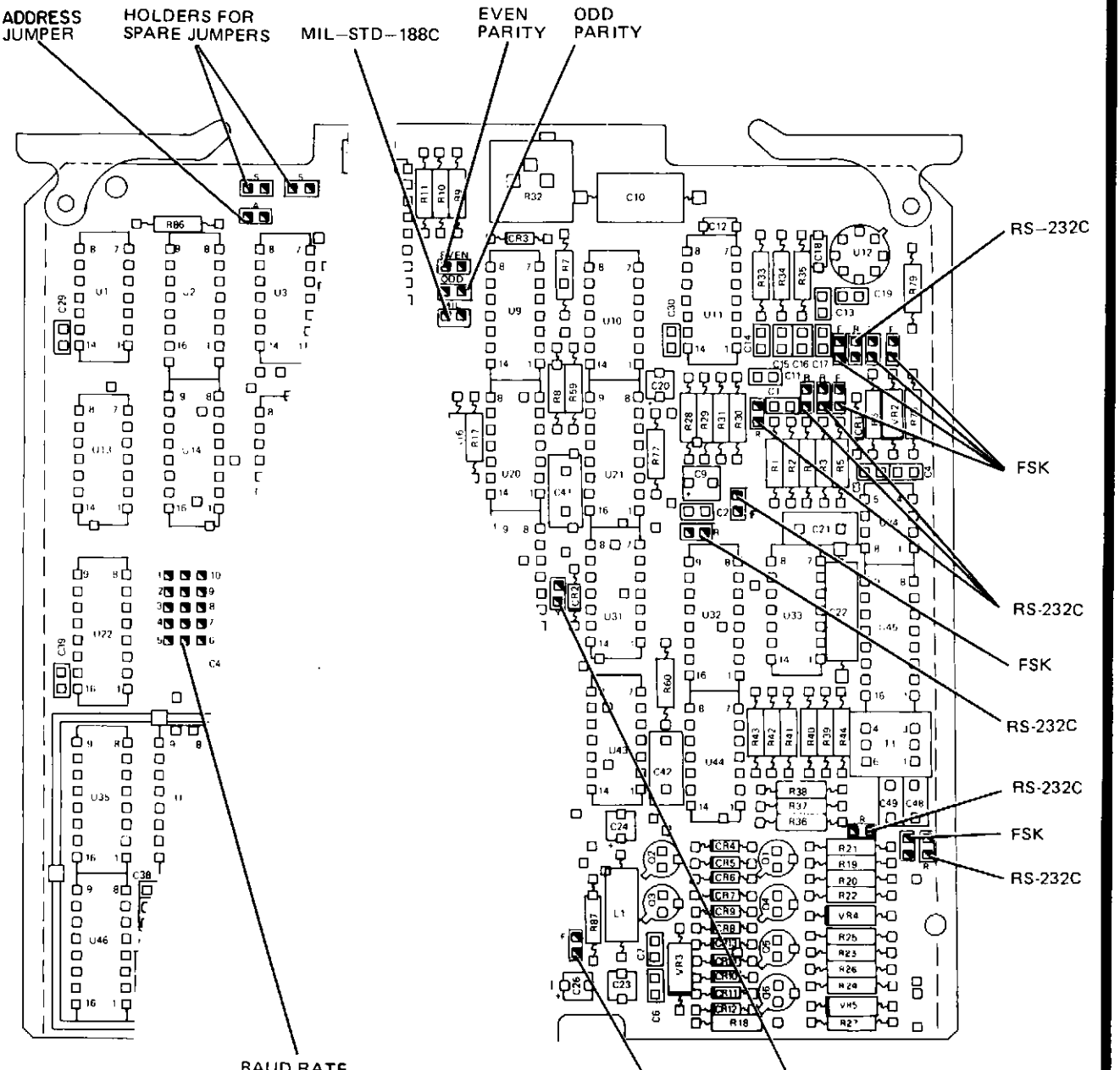
4.4.3 No Parity

If parity recognition is not required, remove both the O and E straps.

Table 3. Baud Rate Strapping.

BAUD RATE (BAUDS)	BAUD STRAP	FSK	RS-232C OR MIL-STD-188C USING	
			CONTROL	PROCESSOR
75	10 to center	X	X	
150	9 to center	X	X	
300	8 to center	X	X	
600	7 to center	X	X	
1200	6 to center		X	X
2400	5 to center			X
4800	4 to center			X
9600	3 to center			X
19 200	2 to center			X
External	1 to center	*	*	*

*Any rate from 75 to 19 200 bauds (baud is 1/16 of applied frequency). FSK cannot exceed 600 bauds.



RATE	JUMPER CENTER TO PIN
75	10
150	9
300	8
600	7
1200	6
2400	5
4800	4
9600	3
19,200	2
EXT CLOCK	1

TP5-1569-019

Serial Interface Strapping
Figure 23

4.5 Address Recognition Strapping

a. If an address is to be recognized, set A strap in place.
b. Strap unit rear connector for specific address recognition as shown in unit installation section.

4.6 Adjustment of FSK Detector Symmetry

a. Perform test setup of table 2, test 1.
b. Strap card for FSK signaling (refer to paragraph 4.1.1).
c. Strap card for 1200 bauds (refer to paragraph 4.2).
d. Strap for odd parity (refer to paragraph 4.4.1).
e. Apply a 0-dB mW FSK signal with a symmetrical 1:1 (mark, space) data pattern between P1-54 and P1-55.
f. Using an oscilloscope, monitor the waveform at TP5 (green) to ground (TP1, brown).
g. Adjust R32 to obtain best symmetry of the waveform at TP5.

5. REPAIR

Repair of the serial interface card is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

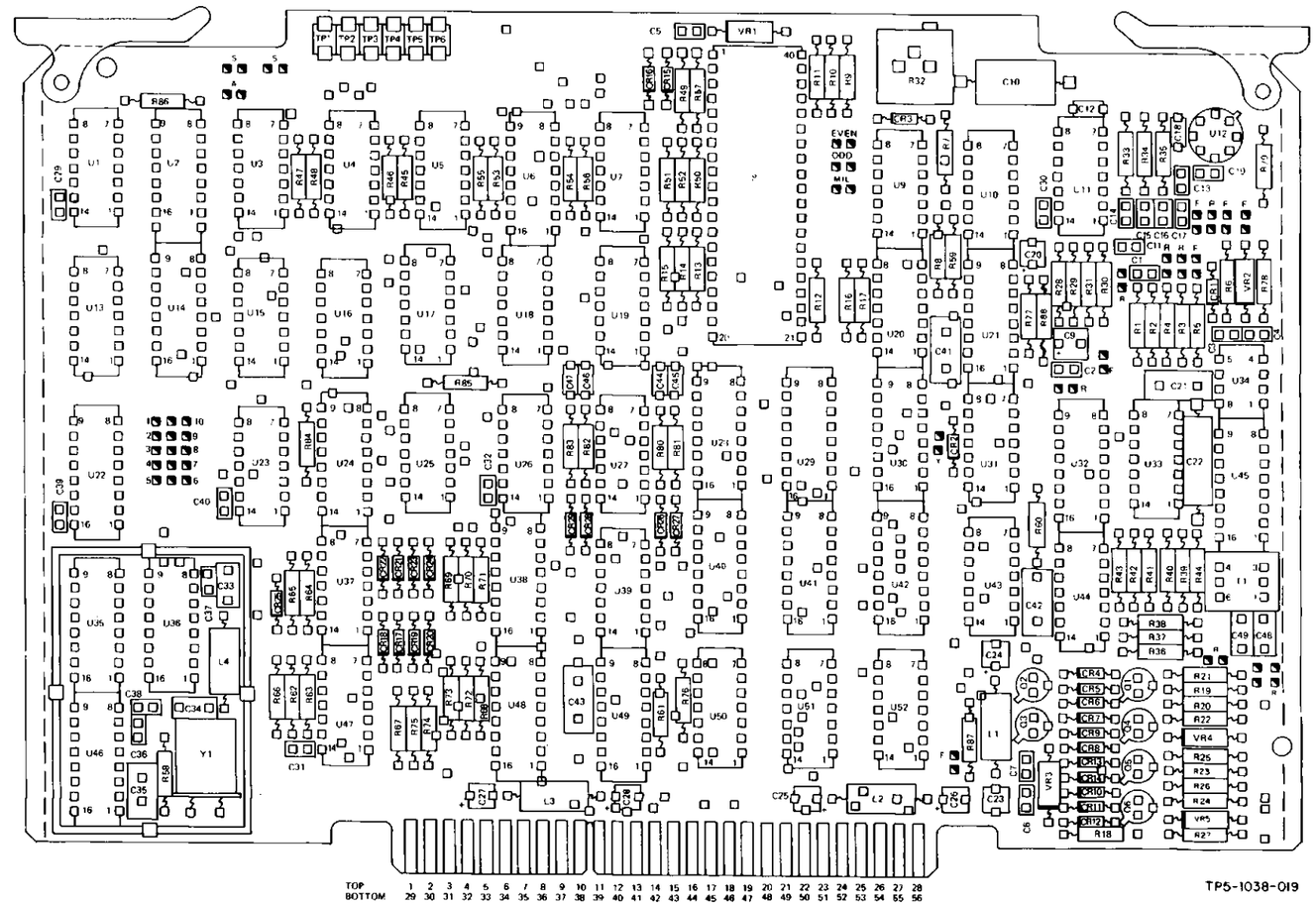
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figure 24). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description is listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Serial Interface	635-0742-001	REV J



Serial Interface, Schematic Diagram
Figure 24 (Sheet 1 of 6)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	SERIAL INTERFACE 635-0742-001		
CR1-CR29	SEMICOND DEVICE, 1N4454	353-3644-010	
C1-C7	CAPACITOR, FXD, CER DIEL, 0.1 µF, 20%, 50V	913-3279-680	
C8	NOT USED		
C9	CAPACITOR, FXD, ELCTLT, 15 µF, 20%, 15V	184-9102-130	
C10	CAPACITOR, FXD, PLSTC DIEL, 0.047 µF, 10%, 200V	933-1039-040	
C11	CAPACITOR, FXD, CER DIEL, 0.1µF, 20%, 50V	913-3279-680	
C12	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C13, C14	CAPACITOR, FXD, CER DIEL, 0.1µF, 20%, 50V	913-3279-680	
C15-C17	CAPACITOR, FXD, CER DIEL, 0.01µF, 20%, 50V	913-3279-110	
C18	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C19	CAPACITOR, FXD, CER DIEL, 0.1µF, 20%, 50V	913-3279-680	
C20	CAPACITOR, FXD, ELCTLT, 1µF, 20%, 35V	184-9102-350	
C21	CAPACITOR, FXD, MICA DIEL, 470pF, 5%, 500V	912-2864-000	
C22	CAPACITOR, FXD, PLSTC DIEL, 0.0056µF, 10%, 80V	933-1039-320	
C23-C28	CAPACITOR, FXD, ELCTLT, 1µF, 20%, 35V	184-9102-350	
C29-C32	CAPACITOR, FXD, CER DIEL, 0.1µF, 20%, 50V	913-3279-680	
C33, C34	CAPACITOR, FXD, CER DIEL, 1µF, 20%, 50V	913-3279-270	
C35	CAPACITOR, FXD, MICA DIEL, 15pF, 5%, 500V (B3)	912-3839-000	
C35	CAPACITOR, FXD, MICA DIEL, 47pF, 5%, 500V	912-3856-001	
C36-C40	CAPACITOR, FXD, CER DIEL, 0.1µF, 20%, 50V	913-3279-680	
C41	CAPACITOR, FXD, MICA DIEL, 200pF, 10%, 500V	912-2838-000	
C42	CAPACITOR, FXD, MICA DIEL, 200pF, 10%, 500V (A1) (A2) (B2)	912-2838-000	
C42	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 500V	912-3879-000	
C43	CAPACITOR, FXD, MICA DIEL, 200pF, 10%, 500V	912-2838-000	
C44-C47	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C48,C49	CAPACITOR, FXD, CER DIEL, 1µF, 20%, 50V	913-3279-270	
L1-L4	COIL, RF, 1000µH	240-2540-000	
Q1	TRANSISTOR, 2N2907A	352-0551-010	
Q2	TRANSISTOR, 2N2222A	352-0661-020	
Q3	TRANSISTOR, 2N2907A	352-0551-010	
Q4	TRANSISTOR, 2N2222A	352-0661-020	
Q5	TRANSISTOR, 2N2907A	352-0551-010	
Q6	TRANSISTOR, 2N2222A	352-0661-020	
R1,R2	RESISTOR, FXD, CMPSN, 47kΩ, 10%, 1/4W	745-0809-000	
R3	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R4	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R5,R6	RESISTOR, FXD, CMPSN, 0.47MΩ, 10%, 1/4W	745-0845-000	
R7,R8	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R9-R20	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R21	RESISTOR, FXD, CMPSN, 1.5kΩ, 10%, 1/4W	745-0755-000	
R22,R23	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W	745-0749-000	
R24	RESISTOR, FXD, CMPSN, 390Ω, 10%, 1/4W	745-0734-000	
R25	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W	745-0749-000	
R26,R27	RESISTOR, FXD, CMPSN, 680Ω, 10%, 1/4W	745-0743-000	
R28	RESISTOR, FXD, CMPSN, 15kΩ, 10%, 1/4W	745-0791-000	
R29	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R30,R31	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R32	RESISTOR, VAR, WW, 5kΩ, 5%, 3/4W	381-1721-060	
R33-R35	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R36-R38	RESISTOR, FXD, FILM, 20.5kΩ, 1%, 1/8W	705-1059-000	
R39,R40	RESISTOR, FXD, FILM, 48.7kΩ, 1%, 1/8W	705-1077-000	
R41,R42	RESISTOR, FXD, FILM, 10kΩ, 1%, 1/8W	705-1044-000	
R43	RESISTOR, FXD, FILM, 20.5kΩ, 1%, 1/8W	705-1059-000	
R44	RESISTOR, FXD, CMPSN, 560Ω, 10%, 1/4W	745-0740-000	
R45-R48	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R49-R57	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R58	RESISTOR, FXD, CMPSN, 10MΩ, 10%, 1/4W	745-0893-000	
R59	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R60	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W (A1) (A2)	745-0773-000	
R61	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R62-R65	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R66	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R67-R77	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R78	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 14W	745-0781-000	
R79	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	

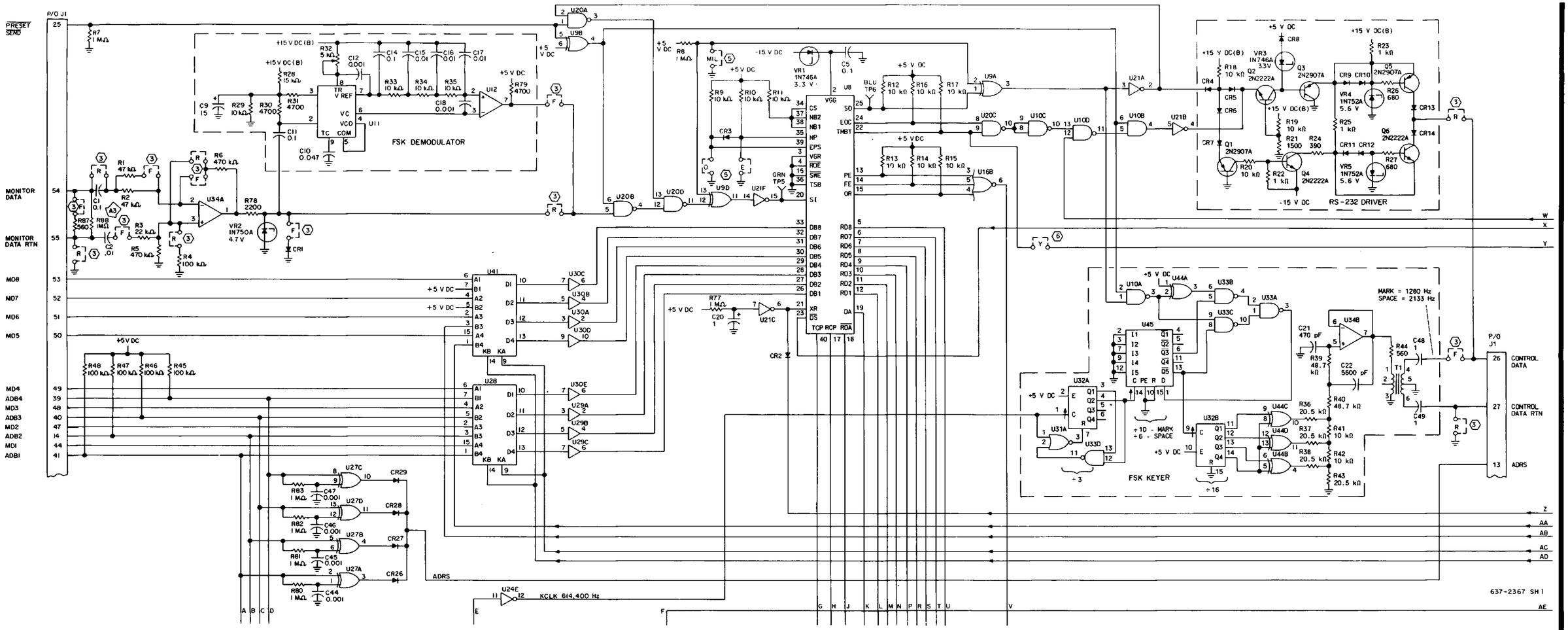
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
R80-R83	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R84	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R85,R86	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R87	RESISTOR, FXD, CMPSN, 560Ω, 10%, 1/4W	745-0740-000	
R88	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W (A3)	745-0857-000	
T1	TRANSFORMER, AF	677-0324-320	
TP1	JACK, TIP, BRN	360-0484-070	
TP2	JACK, TIP, RED	360-0484-020	
TP3	JACK, TIP, ORN	360-0484-050	
TP4	JACK, TIP, YEL	360-0484-060	
TP5	JACK, TIP, GRN	360-0484-040	
TP6	JACK, TIP, BLU	360-0484-080	
U1	INTEGRATED CKT, MC14025CP	351-8159-150	
U2	INTEGRATED CKT, F4029BPC	351-8159-250	
U3	INTEGRATED CKT, MC14001CP	351-8159-020	
U4	INTEGRATED CKT, F4030BPC	351-8159-190	
U5	INTEGRATED CKT, MC14011CP	351-8159-040	
U6	INTEGRATED CKT, F4021BPC	351-8159-230	
U7	INTEGRATED CKT, F4013BPC	351-8159-110	
U8	INTEGRATED CKT, AY5-1013A	351-8173-010	
U9	INTEGRATED CKT, F4030BPC	351-8159-190	
U10	INTEGRATED CKT, MC14011CP	351-8159-040	
U11	INTEGRATED CKT, LM565CN	351-1114-010	
U12	INTEGRATED CKT, LM311H	351-1094-060	
U13	INTEGRATED CKT, MC14025CP	351-8159-150	
U14	INTEGRATED CKT, F4049BPC	351-8159-210	
U15	INTEGRATED CKT, MC14011CP	351-8159-040	
U16	INTEGRATED CKT, MC14025CP	351-8159-150	
U17, U18	INTEGRATED CKT, F4013BPC	351-8159-110	
U19, U20	INTEGRATED CKT, MC14011CP	351-8159-040	
U21	INTEGRATED CKT, F4049BPC	351-8159-210	
U22	INTEGRATED CKT, F4040BPC	351-8159-240	
U23	INTEGRATED CKT, F4024BPC	351-8159-100	
U24	INTEGRATED CKT, F4049BPC	351-8159-210	
U25	INTEGRATED CKT, F4013BPC	351-8159-110	
U26	INTEGRATED CKT, MC14001CP	351-8159-020	
U27	INTEGRATED CKT, F4030BPC	351-8159-190	
U28	INTEGRATED CKT, F4019BPC	351-8159-080	
U29, U30	INTEGRATED CKT, F4050BPC	351-8159-220	
U31	INTEGRATED CKT, MC14001CP	351-8159-020	
U32	INTEGRATED CKT, F4520PC	351-8315-010	
U33	INTEGRATED CKT, MC14011CP	351-8159-040	
U34	INTEGRATED CKT, MC1458P1	351-1071-070	
U35, U36	INTEGRATED CKT, F4027BPC	351-8159-180	
U37	INTEGRATED CKT, F4013BPC	351-8159-110	
U38	MOS, ANLG MXR, F4052PC	351-8227-020	
U39	INTEGRATED CKT, MC14011CP	351-8159-040	
U40	INTEGRATED CKT, F4029BPC	351-8159-250	
U41	INTEGRATED CKT, F4019BPC	351-8159-080	
U42	INTEGRATED CKT, F4049BPC	351-8159-210	
U43	INTEGRATED CKT, MC14001CP	351-8159-020	
U44	INTEGRATED CKT, F4030BPC	351-8159-190	
U45	INTEGRATED CKT, MC14018 BCP	351-8253-010	
U46	INTEGRATED CKT, F4049BPC	351-8159-210	
U47	INTEGRATED CKT, F4013BPC	351-8159-110	
U48	MOS, ANLG MXR, F4052PC	351-8227-020	
U49	INTEGRATED CKT, F4027BPC	351-8159-180	
U50, U51	INTEGRATED CKT, F4013BPC	351-8159-110	
U52	INTEGRATED CKT, MC14011CP	351-8159-040	
VR1	SEMICOND DEVICE, 1N746A	353-2938-000	
VR2	SEMICOND DEVICE, 1N750A	353-2708-000	
VR3	SEMICOND DEVICE, 1N746A	353-2938-000	
VR4, VR5	SEMICOND DEVICE, 1N752A	353-2712-000	
Y1	XTAL UNIT, QTZ, 3.6864 MHz	289-7120-060	

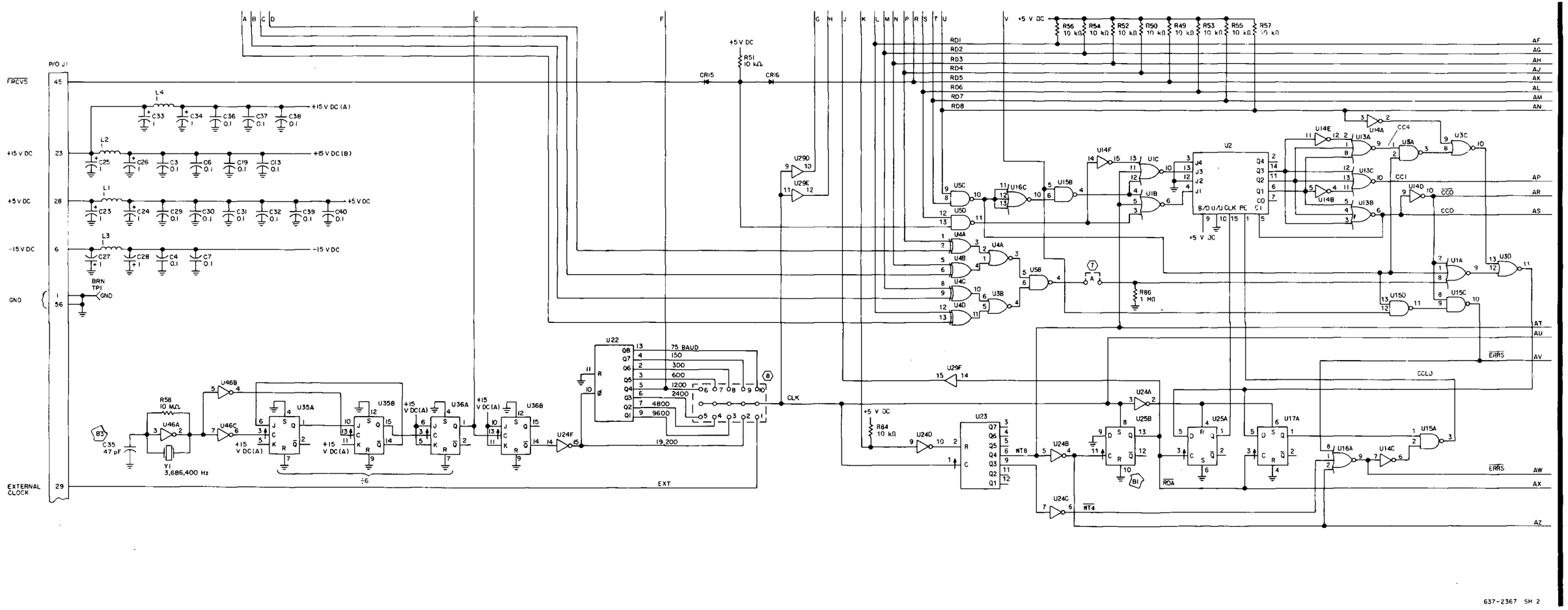
MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Removed C42, 200pF. Removed R60, 4700Ω.	REV B
A2	Added C42, 200pF. Added R60, 4700Ω.	REV C and above
A3	Added R88, 1 MΩ.	REV D
B1	Removed connection from U25B-12 to U17B-11 and U19C-9.	REV F and above
B2	Changed C42 from 200pF to 100pF.	REV G and above.
B3	Removed C35, 15pF from across R58. Added C35, 47pF.	REV J and above

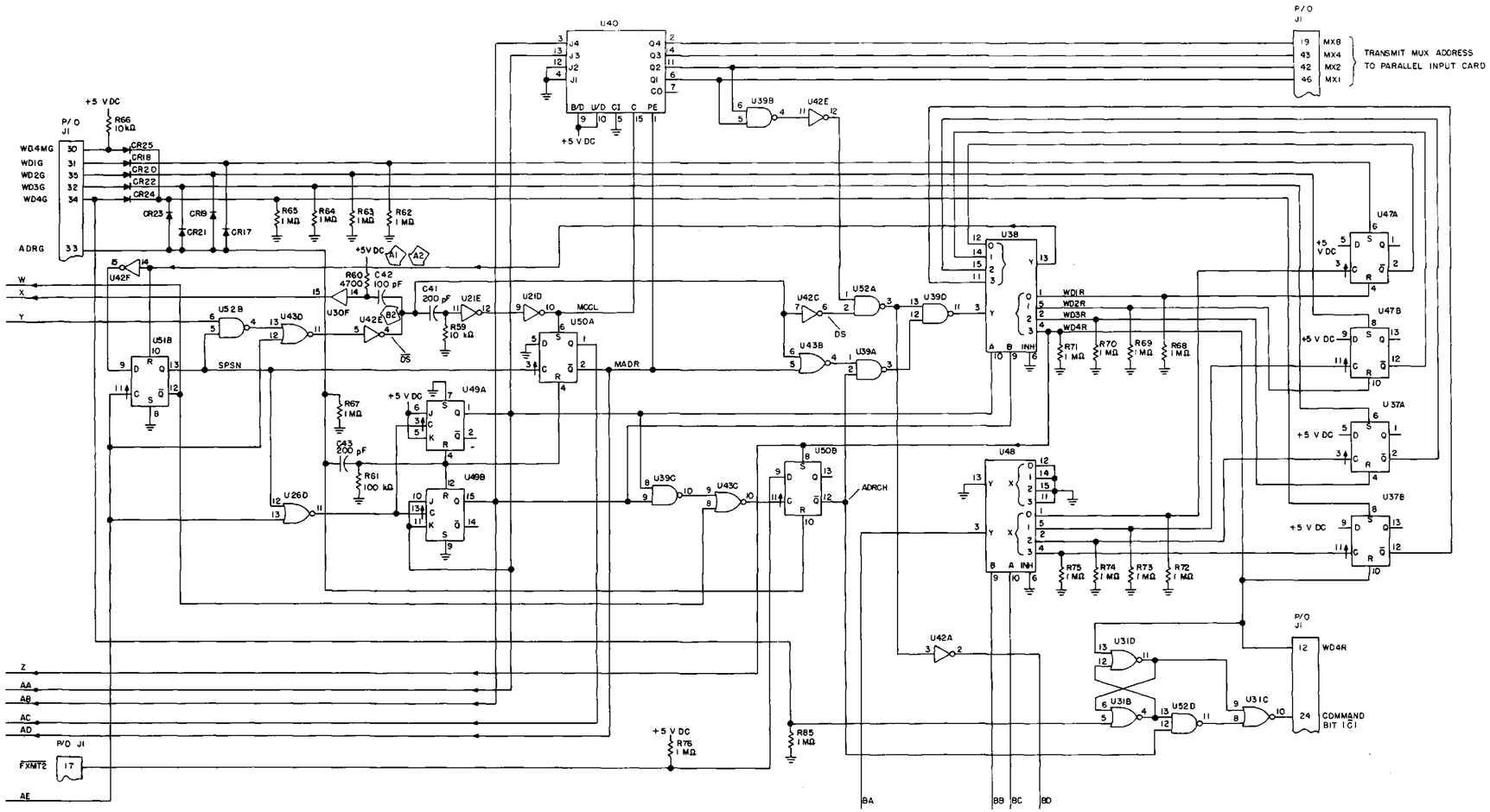
Serial Interface, Schematic Diagram
Figure 24 (Sheet 2)



Serial Interface, Schematic Diagram
Figure 21 (Sheet 3)



Serial Interface, Schematic Diagram
Figure 24 (Sheet 4)



NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, INDUCTANCE VALUES ARE IN MILLIHENRIES AND DIODES ARE TYPE IN4454.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. FOR FSK OPTION, JUMPERS LABELED "F" (QTY 7) ARE INSTALLED. FOR RS-232C OPTION, JUMPERS LABELED R (QTY 7) ARE INSTALLED.
4.
5. "E" STAPPED FOR EVEN PARITY, "O" STRAPPED FOR ODD PARITY, NEITHER STRAPPED FOR NO PARITY, "MIL" STRAPPED FOR MIL-STD-188C DATA LOGIC LEVELS, NOT STRAPPED WHEN USING FSK DATA OPTION, OR RS-232-C DATA LOGIC LEVELS.
6. PINS LABELED "Y" USED FOR TEST PURPOSE ONLY- JUMPER FOR NORMAL OPERATION.
7. PINS LABELED "A" JUMPERED TO ENABLE ADDRESS RECOGNITION. PINS LABELED "S" ARE USED TO HOLD SPARE JUMPERS.
8. BAUD RATE SELECT.

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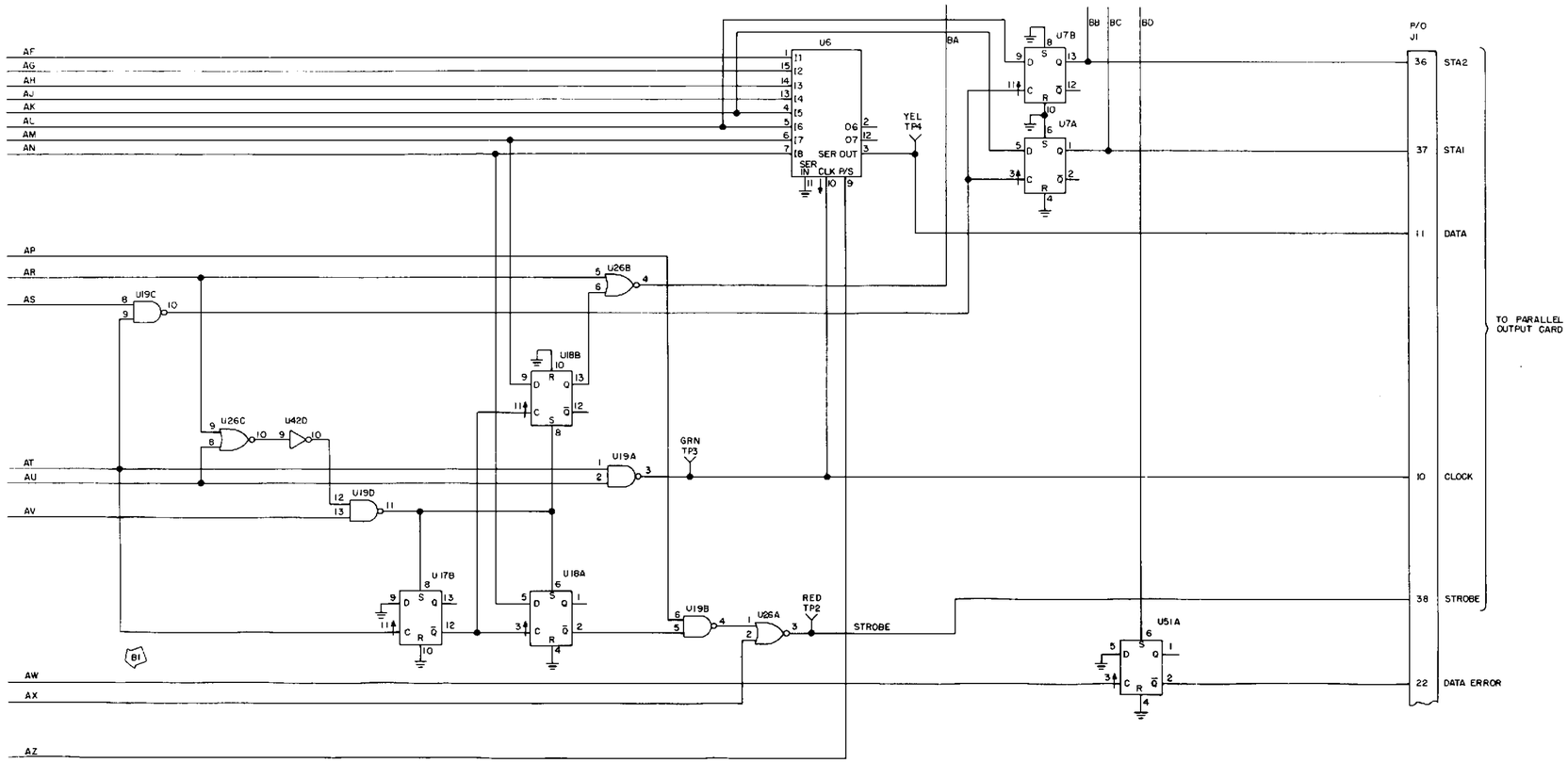
Serial Interface, Schematic Diagram
Figure 24 (Sheet 5)



MICROCIRCUIT POWER AND GROUND CONNECTIONS

U NO.	TYPE	POWER (V DC)				
		+15(A)	+15(B)	+5	GND	-15
U1,U13,U15	MC14025CP			14	7	
U2,U40	F4029BPC			16	8	
U3,U26,U31,U43	MC14001CP			14	7	
U4,U9,U27,U44	F4030BPC			14	7	
U5,U10,U15,U19, U20,U33,U39,U52	MC14011CP			14	7	
U6	F4021BPC			15	8	
U7,U17,U18,U25, U37,U47,U50,U51	F4013BPC			14	7	
U8	AY-5-1013A			1	3	
U11,	LM565CN		10		1	
U12	LH311H		8		4,1	
U14,U21,U24,U42	F4049BPC			1	8	
U46	F4049BPC	1			8	
U22	F4040BPC			16	8	
U23	F4024BPC			14	7	
U28,U41	F4019BPC			16	8	
U29,U30	F4050BPC			1	8	
U32	F4520PC			16	8	
U34	MC1458P1		8			4
U35,U36	F4027BPC	16			8	
U49	F4027BPC			16	8	
U38,U48	F4052PC			16	8 7	
U45	MC14018BCP			16	8	

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Serial Interface, Schematic Diagram
Figure 24 (Sheet 6)

Synthesizer Voltage Regulator (635-0656-001)

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

523-0767974-002211
2nd Edition, 1 June 1978

1. DESCRIPTION

Synthesizer Voltage Regulator 635-0656-001, shown in figure 1, is a 2-layer planar card with a 20-pin edge-on connector (2 layers, 10 pins each).

The synthesizer voltage regulator consists of a +20-V dc series regulator, a +5.2-V dc series regulator, and a loss-of-lock summary monitor.

2. PRINCIPLES OF OPERATION

2.1 General

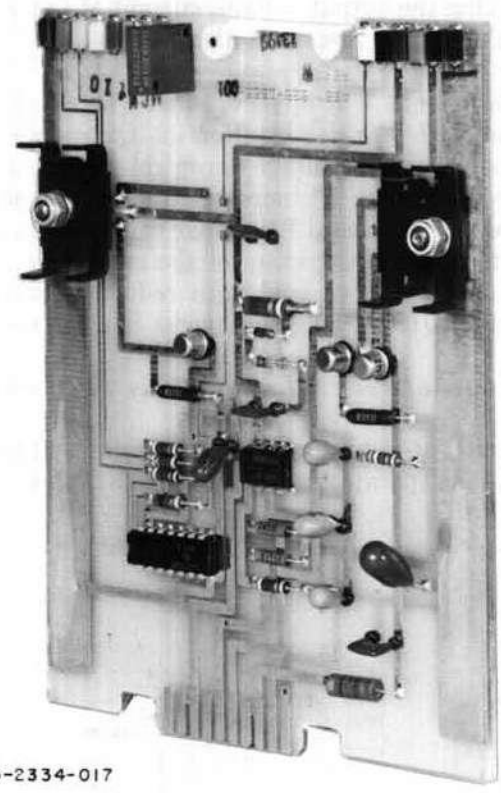
The synthesizer voltage regulator receives +24- and +8-V dc inputs and supplies regulated outputs of +20 and +5.2 V dc.

The synthesizer voltage regulator receives seven monitor inputs and provides one monitor summary output.

2.2 +5.2-V DC Series Regulator (Refer to figure 3.)

The +5.2-V dc series regulator consists of a current/voltage regulator (Q3-Q4), a current control (Q5), a voltage control (U1B), and a reference regulator (VR1).

With +8 and +24 V dc applied, voltage control U1B is enabled. The +24 V dc is applied through R2 to reference regulator VR1. Reference regulator VR1 voltage is applied through R7 to noninverting (reference) input of U1B, and the +5.2-V dc output is applied directly to the inverting input of U1B. Note that R7 is adjusted for an optimum 5.2-V dc regulated output. As the +5.2-V dc output increases, a lower voltage output of U1B is applied to regulator Q3-Q4 base, reducing the output voltage/current of the +5.2-V dc regulator. The inverse is also true.



Synthesizer Voltage Regulator
Figure 1

With +8 V dc applied, current through Q3-Q4 and R6 provides bias for Q5. Q5 supplies an inverted dc output voltage to control Q3-Q4; that is, as the current through R6 increases, the voltage across R6 increases.

NOTICE: This section replaces first edition dated 1 June 1977.

Increased R6 voltage causes Q5 to increase conduction and decrease voltage at Q3-Q4 base. Conduction of Q3-Q4 is decreased, thus reducing current flow through Q1 and R1. The inverse is also true.

2.3 +20-V DC Series Regulator (Refer to figure 3.)

The +20-V dc series regulator consists of current/voltage regulator Q1, current control Q2, and voltage control U1A.

With +24-V dc input applied, and +5.2-V dc regulated output supplied, voltage control U1A is enabled. The +5.2-V dc output is applied to the non-inverting (reference) input of U1A, and the +20-V dc output is supplied through voltage divider R2 and R4 and applied to the inverting input of U1A. As the voltage at the junction of R3-R4 increases, a lower voltage output of U1A is applied to regulator Q1 base, reducing the output voltage/current of the +20-V dc regulator. The inverse is also true.

With the +24 V dc applied, current supplied through Q1 and R1 provides bias for Q2. Q2 supplies an inverted dc output voltage to control Q1; that is, as the current through R1 increases, the voltage across R1 increases. Increased R1 voltage causes Q2 to increase conduction and decrease voltage at Q1 base. Conduction of Q1 is decreased, thus reducing current flow through Q1 and R1. The inverse is also true.

2.4 Loss-of-Lock Monitor (Refer to figure 3.)

The loss-of-lock monitor is a monitor summary circuit that operates as a normal NAND gate. With all loss-of-lock signals in the normal state (all lock signals present), all logic 1 signals are applied to NAND gate U2 providing a logic 0 output from U2. If any lock signal is lost, a logic 0 is applied by the associated decade to the loss-of-lock monitor and a logic 1 loss-of-lock output is supplied. Note that any (or all) logic 0 inputs to U2 provide a logic 1 output from U2.

2.5 Dual Operational Amplifier MC1458P1 (Refer to figure 2.)

The MC1458G consists of two operational amplifiers in one package designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components.

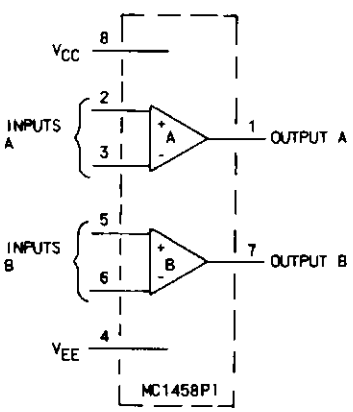
3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the synthesizer voltage regulator are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 1 check total performance of the synthesizer voltage regulator. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.



CHARACTERISTICS
SUPPLY VOLTAGE: V_{CC} +18 V DC MAX
V_{EE} -18 V DC MAX
INPUT DIFF VOLTAGE: ±30 V MAX
INPUT COMMON MODE VOLTAGE:
±15 V MAX (1)
OUTPUT SHORT CIRCUIT DURATION:
CONTINUOUS (2)
INPUT RESISTANCE: 300 kΩ MIN, 2.0 MΩ MAX
OUTPUT RESISTANCE: 75Ω TYPICAL
VOLTAGE GAIN: 15 MIN

NOTES:
(1) FOR SUPPLY VOLTAGE LESS THAN ±15.0 V, MAX INPUT VOLTAGE EQUAL TO SUPPLY VOLTAGE.
(2) SUPPLY VOLTAGE EQUAL TO OR LESS THAN 15 V.

TP5-2285-013

Dual Operational Amplifier MC1458P1
Figure 2

Table 1. Synthesizer Voltage Regulator, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of the unit containing the synthesizer voltage regulator to be tested.		
	b. Remove cover from synthesizer section of unit.		
	c. Remove synthesizer voltage regulator, install it on an extender card, and place it in the unit.		
	d. Set unit LINE SELECTOR switch to 115 V.		
	e. Connect unit to 115-V ac power source and set power on.		
	f. Measure dc voltage from TP10 to TP13 (ground).	+24.0 ±0.5 V dc.	Check unit power supply.
	g. Measure dc voltage from TP11 to TP13 (ground).	-8.0 ±0.04 V dc.	Check unit power supply.
2. +5.2 V dc	a. Measure dc voltage from TP9 to TP13 (ground).	+5.2 ±0.05 V dc.	Adjust R7 for +5.2 ±0.05 V dc. If R7 adjustment does not correct the problem, check U1B, Q3, Q4, Q5, and associated circuit.
3. +20-V dc regulator	a. Measure dc voltage from TP12 to TP13 (ground).	NLT +19.7 V dc, NMT +20.6 V dc.	Check U1A, Q1, Q2, and associated circuit.
4. Loss-of-lock monitor	a. Measure voltage from TP8 to TP13 (ground).	NMT 0.5 V dc.	Check dc voltages at TP1 thru TP7. If all voltages are NLT +3.5 V dc, check U2 and associated circuit. If any voltages are less than +3.5 V dc, check unit synthesizer card associated with the input.
	b. Monitor voltage from TP8 to TP13 for steps c thru j.		
	c. Apply a ground signal to TP1.	NLT +3.5 V dc.	Check U2.
	d. Remove ground from TP1 and apply it to TP2.	NLT +3.5 V dc.	Check U2.
	e. Remove ground from TP2 and apply it to TP3.	NLT +3.5 V dc.	Check U2.
	f. Remove ground from TP3 and apply it to TP4.	NLT +3.5 V dc.	Check U2.
(Cont)	g. Remove ground from TP4 and apply it to TP5.	NLT +3.5 V dc.	Check U2.

Table 1. Synthesizer Voltage Regulator, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	h. Remove ground from TP4 and apply it to TP6.	NLT +3.5 V dc.	Check U2.
	i. Remove ground from TP6 and apply it to TP7.	NLT +3.5 V dc.	Check U2.
	j. Remove ground from TP7.		
5. Shutdown	a. Set power off.		
	b. Remove synthesizer voltage regulator from card extender and reinstall it in the unit.		
	c. Replace cover on synthesizer section of unit.		
	d. Replace top cover of unit.		

4. ALIGNMENT/ADJUSTMENT

Refer to table 1, test 2 for adjustment of R7 (+5.2-V dc regulator).

5. REPAIR

Repair of the synthesizer voltage regulator is accomplished using the standard planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

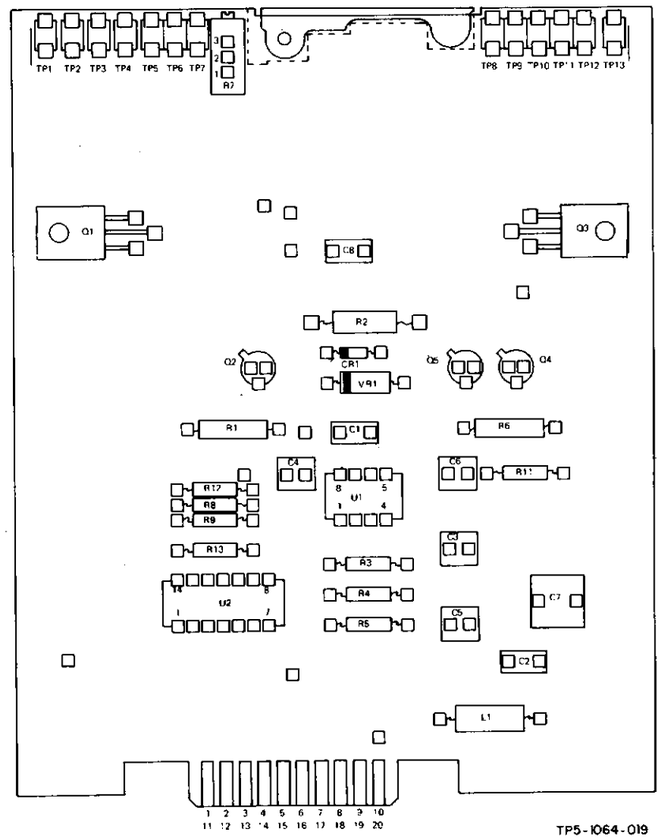
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram, figure 3. The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

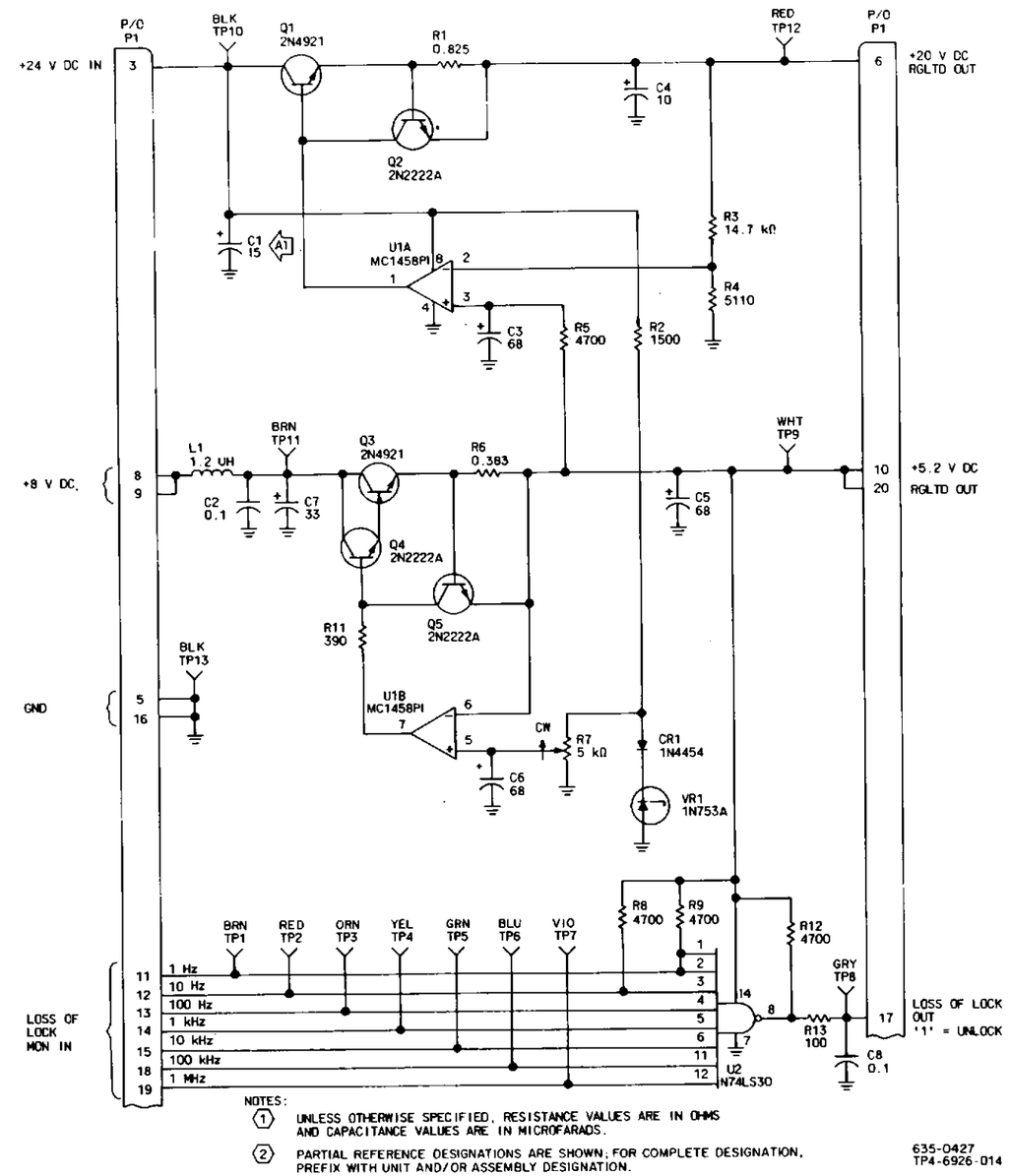
Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points to the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Synthesizer voltage regulator	635-0656-001	REV C





Synthesizer Voltage Regulator, Schematic Diagram
Figure 3 (Sheet 1 of 2)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	SYNTH VOLTAGE REGULATOR 635-0656-001		
CR1	SEMICOND DEVICE, 1N4454	353-3644-010	
C1	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V (A1)	913-3279-200	
C1	CAPACITOR, FXD, ELCTLT, 15μF, 20%, 35V	184-9102-420	
C2	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C3	CAPACITOR, FXD, ELCTLT, 68μF, 20%, 6V	184-9102-040	
C4	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-240	
C5, C6	CAPACITOR, FXD, ELCTLT, 68μF, 20%, 6V	184-9102-040	
C7	CAPACITOR, FXD, ELCTLT, 33μF, 20%, 25V	184-9102-260	
C8	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
L1	COIL, RF, 1.20μH	240-2715-140	
Q1	TRANSISTOR, 2N4921	352-0782-010	
Q2	TRANSISTOR, 2N2222A	352-0661-020	
Q3	TRANSISTOR, 2N4921	352-0782-010	
Q4, Q5	TRANSISTOR, 2N2222A	352-0661-020	
R1	RESISTOR, FXD, WW, 0.825Ω, 1%, 1W	747-1499-340	
R2	RESISTOR, FXD, CMPSN, 1.5kΩ, 10%, 1/2W	745-1359-000	
R3	RESISTOR, FXD, FILM, 14.7kΩ, 1%, 1/8W	705-1052-000	
R4	RESISTOR, FXD, FILM, 5.11kΩ, 1%, 1/8W	705-1030-000	
R5	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R6	RESISTOR, FXD, WW, 0.383Ω, 1%, 1W	747-1499-270	
R7	RESISTOR, VAR, WW, 5kΩ, 5%, 3/4W	381-1721-390	
R8, R9	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R10	NOT USED		
R11	RESISTOR, FXD, CMPSN, 390Ω, 10%, 1/4W	745-0734-000	
R12	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R13	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
TP1	JACK, TIP, BRN	360-0484-070	
TP2	JACK, TIP, RED	360-0484-020	
TP3	JACK, TIP, ORN	360-0484-050	
TP4	JACK, TIP, YEL	360-0484-060	
TP5	JACK, TIP, GRN	360-0484-040	
TP6	JACK, TIP, BLU	360-0484-080	
TP7	JACK, TIP, VIO	360-0484-090	
TP8	JACK, TIP, GRA	360-0484-100	
TP9	JACK, TIP, WHT	360-0484-010	
TP10	JACK, TIP, BLK	360-0484-030	
TP11	JACK, TIP, BRN	360-0484-070	
TP12	JACK, TIP, RED	360-0484-020	
TP13	JACK, TIP, BLK	360-0484-030	
U1	INTEGRATED CKT, MC1458P1	351-1071-070	
U2	INTEGRATED CKT, N74LS30N	351-1523-140	
VR1	SEMICOND DEVICE, 1N753A	353-2714-000	

MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Changed C1 from 0.1μF to 15μF.	REV C and above

Synthesizer Voltage Regulator, Schematic Diagram
Figure 3 (Sheet 2)

Synthesizer Reference (623-2085-001)

Rockwell International

instructions

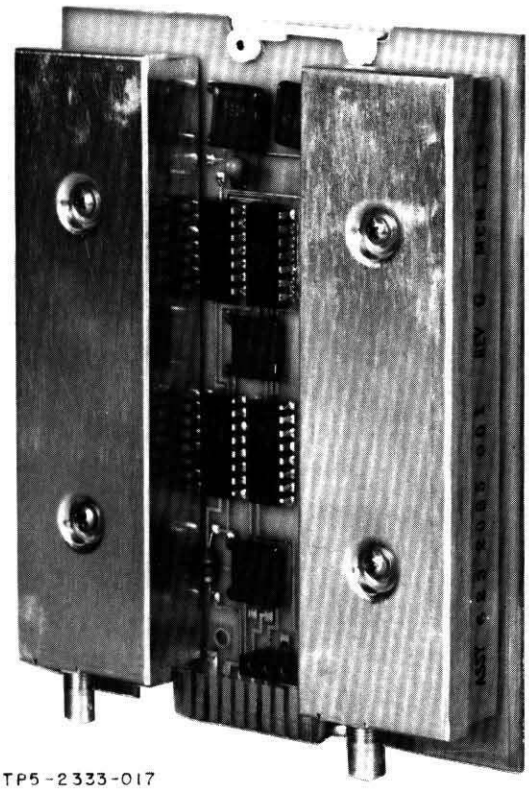
Collins Telecommunications Products Division

Printed in USA

523-0767970-002211
2nd Edition, 1 June 1978

1. DESCRIPTION

Synthesizer Reference 623-2085-001, shown in figure 1, is a module that contains a base 3-layer planar card and two rf secure compartments (metal box construction) that contain two printed wiring boards. It has provisions for mounting an external phase-lock card that is used with an external frequency standard. The base 3-layer planar card contains a 20-pin, edge-on connector (2 layers, 10 pins each).



TP5-2333-017

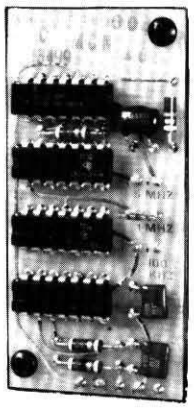
Synthesizer Reference
Figure 1

The synthesizer reference module consists of a reference oscillator, a times 12 multiplier, a divide-by-11 circuit, a divide-by-9 circuit, a divide-by-2 circuit, and provisions for using the optional external phase-lock card.

1.1 External Phase-Lock (Optional)

External Phase-Lock 635-0655-001, shown in figure 2, is an optional printed wiring board that mounts to the synthesizer reference module and allows an external frequency standard to be used. The external phase-lock card is a 2-layer planar card that uses a 5-pin connector to mate with the synthesizer reference module.

The external phase-lock card consists of a squaring amplifier, a divide-by-10 circuit, a divide-by-5 circuit, a phase discriminator, and provisions to allow using a 100-kHz, 1-MHz, or 5-MHz external frequency standard.



TP5-3193-017

External Phase-Lock
Figure 2

NOTICE: This section replaces first edition dated 1 June 1977.

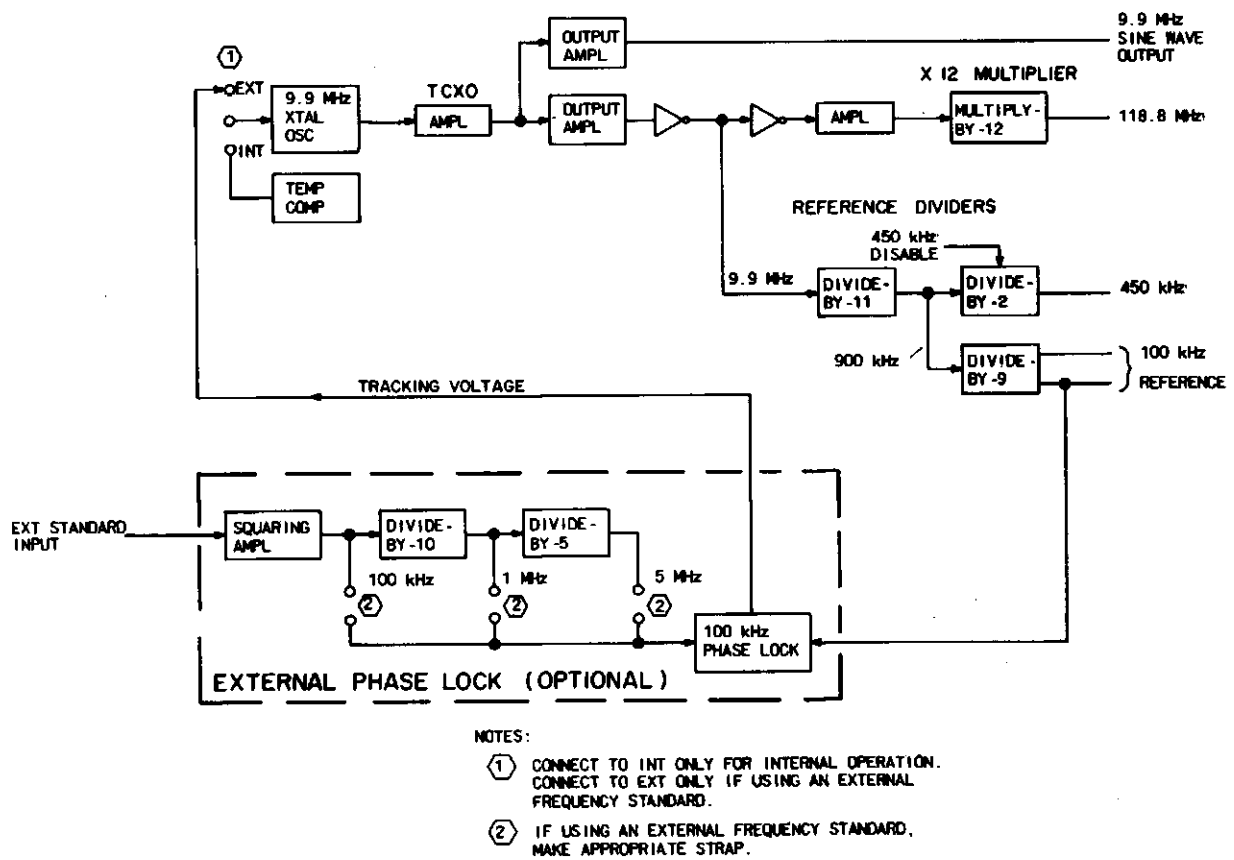
2. PRINCIPLES OF OPERATION

2.1 General (Refer to figure 3.)

The synthesizer reference module receives input voltages and a 450-kHz enable/disable signal and generates a 9.9-MHz sine-wave output, a 118.8-MHz output, a 450-kHz output, and a 100-kHz reference signal output. The 9.9-MHz, 118.8-MHz, and 450-kHz outputs are used as injection inputs to the rf translator and if amplifiers, and the 100-kHz output is used as a reference for generating the variable injection frequencies. In addition, if the external phase-lock card is used, the synthesizer reference module outputs are frequency/temperature stabilized by an external 100-kHz, 1-MHz, or 5-MHz frequency standard.

2.2 TCXO (Refer to figure 9.)

The tcxo is a voltage-controlled, temperature-compensated crystal oscillator. When used with its internal compensation circuit, RT1 through RT3 provide a temperature-compensated voltage control signal to the crystal oscillator. The crystal oscillator supplies a 9.9-MHz signal through one output amplifier to the rf translator for fixed 9.9-MHz signal



Synthesizer Reference, Block Diagram
Figure 3

injection. The crystal oscillator supplies the 9.9-MHz signal through a second output amplifier to an inverter.

The 9.9-MHz signal from the inverter is supplied to the reference dividers and through a second inverter to the times 12 multiplier.

2.3 Times 12 Multiplier (Refer to figure 9.)

The 9.9-MHz signal is received by the times 12 multiplier, multiplied and applied to crystal filter Y1 (118.8 MHz), and produces an output 12 times the frequency of the applied input. The 118.8-MHz output is supplied to the rf translator for fixed 118.8-MHz signal injection.

2.4 Reference Dividers (Refer to figure 9.)

2.4.1 Divide-by-11

The 9.9-MHz signal is received by the divide-by-11 circuit, divided (900 kHz), and applied to the divide-by-9 and divide-by-2 circuits. The divide-by-11 circuit consists of an up/down decade counter and a D-type flip-flop. Refer to table 1 for the logic truth table of the divide-by-11 circuit. Note that when the ripple clock (cc) output resets the D-type flip-flop, it latches the reset condition until the ripple clock is removed (after the next clock input). This causes the decade counter to be loaded at counter 0 for the last half of clock 9, all of clock 10, and until after clock 11 is applied; then the load (L) logic 0 is removed. Clock 12 and clock 1 are one and the same, producing a divide-by-11 circuit.

2.4.2 Divide-by-9

The 900-kHz signal from the divide-by-11 circuit is received by the divide-by-9 circuit, divided (100 kHz), and applied as a 100-kHz reference signal to the unit under control and the external phase lock (if used). The divide-by-9 circuit consists of an up/down decade counter. Refer to table 2 for a logic truth table of the divide-by-9 circuit. Note that the ripple clock (RC) output loads the decade counter to count 0 during the last half of clock 9 and allows the counter to count 1 at

Table 1. Divide-by-11 Logic Truth Table.

CLOCK INPUT	U1						U3A				
	OUTPUTS						INPUTS			OUTPUTS	
	QA	QB	QC	QD	RC	COUNT	C	D	R	Q	$\bar{Q}$
1	1	0	0	0	1	1	1	1	1	1	0
2	0	1	0	0	1	2	2	1	1	1	0
3	1	1	0	0	1	3	3	1	1	1	0
4	0	0	1	0	1	4	4	1	1	1	0
5	1	0	1	0	1	5	5	1	1	1	0
6	0	1	1	0	1	6	6	1	1	1	0
7	1	1	1	0	1	7	7	1	1	1	0
8	0	0	0	1	1	8	8	1	1	1	0
9	1	0	0	1	1	9	9	1	1	1	0
9.5	0	0	0	0	*0	0	9.5	0	0	0	1
10	0	0	0	0	1	0	10	1	1	0	1
11	0	0	0	0	1	0	11	1	1	1	0
12/1	1	0	0	0	1	1	12/1	1	1	1	0

*RC logic 0 appears only for one-half clock cycle time and returns to logic 1 (U1 is reset to start count at 1).

Table 2. Divide-by-9 Logic Truth Table.

CLOCK INPUT	U2					
	OUTPUTS					
	QA	QB	QC	QD	RC	COUNT
1	1	0	0	0	1	1
2	0	1	0	0	1	2
3	1	1	0	0	1	3
4	0	0	1	0	1	4
5	1	0	1	0	1	5
6	0	1	1	0	1	6
7	1	1	1	0	1	7
8	0	0	0	1	1	8
9	1	0	0	1	1	9
9.5	0	0	0	0	*0	0
10/1	1	0	0	0	1	1

*RC logic 0 appears only for one-half clock cycle time and returns to logic 1 (U1 is reset to start count at 1).

clock 10. Clock 10 and clock 1 are one and the same, producing a divide-by-9 circuit.

2.4.3 Divide-by-2

The 900-kHz signal from the divide-by-11 circuit is received by the divide-by-2 circuit, divided (450 kHz), and applied as a 450-kHz carrier reinsertion signal to the unit under control. The divide-by-2 circuit consists of a D-type flip-flop. Refer to table 3 for a logic truth table of the divide-by-2 circuit. Note that a logic 0 on the set input disables the divide-by-2 circuit (latches it in the set condition).

2.5 External Phase-Lock (Refer to figure 10.)

The external phase-lock card receives an external frequency standard (5 MHz, 1 MHz, or 100 kHz) and a tcxo 100-kHz reference signal for use in generation of a tracking voltage output for control of the synthesizer reference tcxo. The external phase lock must be internally strapped for the appropriate external frequency standard.

Table 3. Divide-by-2, Logic Truth Table.

INPUTS			OUTPUTS	
Clock	D	S	Q	$\bar{Q}$
⟶1	0	1	0	1
No change	1	1	No change	
⟶1	1	1	1	0
No change	0	1	No change	
⟶1	0	1	0	1
X	X	0	1	0

⟶1 = change from logic 0 to logic 1
1 = logic 1
0 = logic 0
X = no effect

2.5.1 100-kHz External Standard

When a 100-kHz external standard is used, it is supplied through the squaring amplifier to the phase detector. A 100-kHz internal reference standard is also applied to the phase detector. The 100-kHz signals are phase compared and a resultant tcxo dc input signal is supplied by the external phase lock.

2.5.2 1-MHz External Standard

When a 1-MHz external standard is used, it is supplied through squaring amplifier to the divide-by-10 circuit. The 100-kHz output of the divide-by-10 circuit is supplied as a 100-kHz external standard to the phase detector. Refer to paragraph 2.5.1 for operation using the 100-kHz external standard.

The divide-by-10 circuit uses a decade counter consisting of a divide-by-2 and a divide-by-5 counter connected to produce a divide-by-10 circuit. Refer to paragraph 2.7 for details on this decade counter.

2.5.3 5-MHz External Standard

When a 5-MHz external standard is used, it is supplied through squaring amplifier to divide-by-10 circuit. The 500-kHz output of the divide-by-10 circuit is supplied to the divide-by-5 circuit, and the 100-kHz output of the divide-by-5 circuit is supplied as a 100-kHz external standard to the phase detector. Refer to paragraph 2.5.1 for operation using the 100-kHz external standard.

The divide-by-10 and divide-by-5 circuits use decade counters consisting of a divide-by-2 and a divide-by-5 counter connected to produce divide-by-10 and divide-by-5 circuits. Refer to paragraph 2.7 for details on this decade counter.

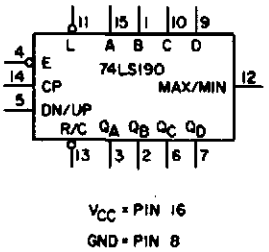
2.6 Up/Down Decade Counter 74LS190 (Refer to figure 4.)

The up/down decade counters used in the synthesizer reference module are provided with an enable control presetting facility, single line up/down control, cascading for multidecade operation, and buffered inputs. The 74LS190 is a 4-bit decade counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when input conditions are met. This mode of operation will eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters.

A high at the enable input inhibits counting. A low at the enable input and a low-to-high clock transition triggers the four master/slave flip-flops. The enable input should be changed only when the clock is high. The down/up input determines the direction of the count. When low, the count goes up; when high, the count goes down.

These counters are fully programmable. The outputs may be preset to any state by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the state of the clock input. This feature allows the counters to be used as modulo N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low level output pulse equal in width to the low level portion of the clock input when an overflow or underflow condition exists. The counters can be cascaded easily by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.



Up/Down Decade Counter 74LS190
Figure 4

Table 4. Up/Down Decade Counter 74LS190, Logic Truth Table.

PROGRAMMABLE INPUTS				COUNT	BCD OUTPUTS			
A	B	C	D		QA	QB	QC	QD
0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	0	0	0
0	1	0	0	2	0	1	0	0
1	1	0	0	3	1	1	0	0
0	0	1	0	4	0	0	1	0
1	0	1	0	5	1	0	1	0
0	1	1	0	6	0	1	1	0
1	1	1	0	7	1	1	1	0
0	0	0	1	8	0	0	0	1
1	0	0	1	9	1	0	0	1

E (enable): logic 0 enables counter; logic 1 inhibits counter.

L (load): logic 0 programs the bcd output count to be set at the bcd count of the programmable inputs; the next clock pulse counts one higher/lower (up/down).

DU (down/up): logic 0 counts up; logic 1 counts down.

CP (clock pulse): logic 0-to-logic 1 transition advances counter.

RC (ripple clock): logic 0 pulse equal to 1/2 clock cycle when an overflow occurs.

MM (maximum/minimum count): logic 1 pulse equal to full clock cycle when an overflow or underflow occurs.

2.7 Decade Counter 74LS90 (Refer to table 5.)

The 74LS90 used in the external phase-lock card is a high-speed, monolithic decade counter consisting of

four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-2 counter and a divide-by-5 counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logic 0 or to a binary coded decimal (bcd) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated into the three following independent count modes:

a. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the bcd count sequence truth table shown above. In addition to a conventional 0 reset, inputs are provided to reset a bcd 9-count for 9's complement decimal applications.

Table 5. Decade Counter 74LS90, Logic Truth Table.

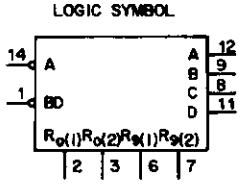
*BCD COUNT SEQUENCE				
COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

**RESET/COUNT							
RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	Count			
0	X	0	X	Count			
0	X	X	0	Count			
X	0	0	X	Count			

*Output A connected to input BD for BCD count.
**X indicates that either a logical 1 or a logical 0 may be present.

b. If a symmetrical divide-by-10 count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of 10, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-10 square wave is obtained at output A.

c. For operation as a divide-by-2 counter and a divide-by-5 counter, no external connections are required. Flip-flop A is used as a binary element for the divide-by-2 function. The BD input is used to obtain binary divide-by-5 operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

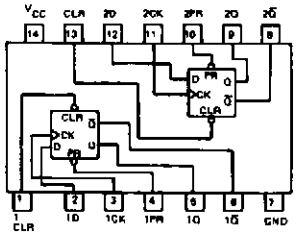


TP5-2326-012

Decade Counter 74LS90
Figure 5

2.8 Dual D-Type Flip-Flop With Preset and Clear 74LS74 (Refer to table 6.)

The 74LS74 consists of dual high-speed, D-type flip-flops. Information at D input is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either high or low level, the D-input signal has no effect.



TP5-2327-011

Dual D-Type Flip-Flop With Preset and Clear 74LS74
Figure 6

Table 6. Dual D-Type Flip-Flop With Preset and Clear 74LS74, Logic Truth Table.

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	*H	*H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the synthesizer reference module are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 7 check total performance of the synthesizer reference. The test procedures in table 8 check total performance of the external phase-lock. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

Table 7. Synthesizer Reference, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of the unit containing the synthesizer reference that is to be tested.		
	b. Remove cover from the synthesizer section of the unit.		
	c. Remove synthesizer reference and install it on an extender card and place it in the unit.		
	d. Set unit LINE SELECTOR switch to 115 V.		
	e. Connect unit to 115-V ac power source and set power on.		
	f. Measure dc voltage from J1-14 and J1-4 to J1-9 (ground).	+5.2 ±0.2 V dc.	Check unit synthesizer voltage regulator.
	g. Measure dc voltage from J1-12 to J1-9 (ground).	NLT +19.5 V dc, NMT +20.8 V dc.	Check unit synthesizer voltage regulator.
	h. Set unit MODE switch to ISB.		
2. 100-kHz reference outputs	a. Using a frequency counter, measure the output between J1-17 and J1-18 (ground).	100 ±0.1 kHz.	
	b. Using an oscilloscope, check the square-wave outputs of J1-17 and J1-18 (ground).	Negative swing (logic 0) is NMT 0.5 V dc. Positive swing (logic 1) is NLT +3.0 V dc.	
(Cont)			

Table 7. Synthesizer Reference, Testing and Troubleshooting Procedures (Cont).

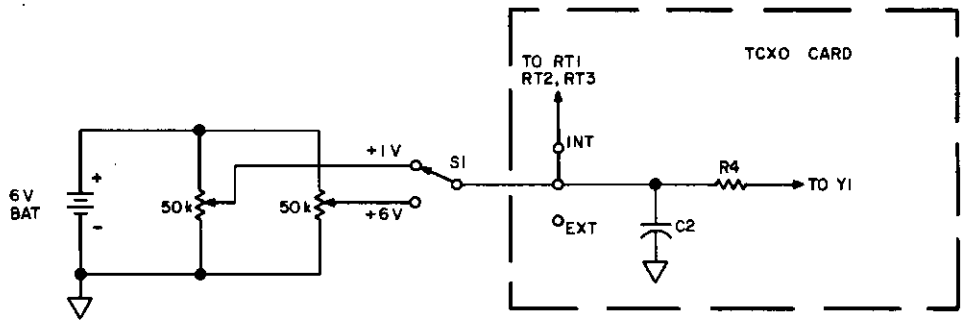
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	c. Using a frequency counter, measure the output between J1-15 and J1-18 (ground).		
	d. Using an oscilloscope, check the square-wave outputs at J1-15 and J1-18 (ground).	Negative swing (logic 0) is NMT 0.5 V dc. Positive swing (logic 1) is NLT +3.0 V dc.	
3. 450-kHz sine-wave output	a. Using an rf voltmeter with a 50-ohm adapter, measure the output between J1-6 and J1-7 (ground).	300 ±75 mV rms.	Check U3B and associated circuit.
	b. Set unit MODE switch to AM.		
	c. Note the output between J1-6 and J1-7 (ground).	≅ 0 mV rms.	Check U3B and unit 450-kHz disable circuit.
	d. Set unit MODE switch to ISB.		
	e. Using a frequency counter, measure the output between J1-6 and J1-7 (ground).	450 ±0.5 kHz.	Check U3A, U3B, and associated circuit.
4. 118.8-MHz sine-wave output	a. Remove shield that covers Y2 (refer to figure 9).		
	b. Using an rf voltmeter with an unloaded probe tip, measure the rf voltage at Y2 output.	Note output.	
	c. Adjust C24 and C28 for maximum output.		
	d. Using an rf voltmeter with a 50-ohm adapter measure the output at P2.		
	e. Adjust C32, C24, and C28 for maximum output.		
	f. Note level after C32, C24, and C28 adjustment.	500 ±100 mV rms.	Adjust A2R27 for 500 mV rms or A2C32 for 500 mV rms if A2R27 not installed.
5. 9.9-MHz sine-wave output (Cont)	a. Using an rf voltmeter with a 50-ohm adapter, measure the output at P3.	300 ±75 mV rms.	Adjust A1R20 for 300-mV rms output. Check that tcxo is strapped to INT. If the above does not correct the results replace A1 tcxo card. (Return tcxo card to factory for repair.)

Table 7. Synthesizer Reference, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	**Note** Field repair of the tcxo card is not recommended; however, if field repair must be accomplished the following additional items of test equipment are required to ensure proper testing and operation. a. Frequency counter, Fluke 1980A (1-Hz accuracy). b. Temperature box, Delta Design MN2800. c. Bias adjustment test box (fabricate per figure 7).		
6. Tcxo card test procedures	**Note** If strong rf fields are present, shielding may be required to meet accuracy requirements.		
	a. Using an oscilloscope with a high-impedance probe, measure the output waveform at Q3-C.	9.9-MHz square wave, symmetrical to with 20%. (Duration of longest half cycle of square wave may not exceed shortest half cycle by more than 20%.)	Check Q1, Q2, Q3, Y1, and associated circuit.
	b. Note the output voltages at Q3-C.	Negative swing (logic 0) is NMT 0.5 V dc. Positive swing (logic 1) is NLT +3.5 V dc.	Check Q3 and associated circuit.
	c. Using an rf voltmeter with a 50-ohm adapter measure the output at P3.	300 ±75 mV rms.	Adjust A1R20 for 300-mV rms output. Check Q2, Q4, and associated circuit.
	d. Connect bias for frequency adjustment using setup in figure 7.		
	e. Adjust +1-V bias control for +2.5 V dc.		
	f. Using the frequency counter, measure the output at P3.	9.9 MHz ±10 Hz.	Select a value of C4 from those listed in parts list to produce 9.9 MHz ±10 Hz. **Note** C1 must be adjustable from 9.9 MHz -10 Hz through 9.9 MHz +10 Hz. If not, select value of C4 to meet this requirement.
(Cont)			

Table 7. Synthesizer Reference, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
6. (Cont)	g. Adjust +1-V bias control for +1.0 V dc.		
	h. Using the frequency counter, measure the output at P3 with the bias set at the +1 V position and with the bias set at the +6 V position.	Note frequency at each bias setting. Sensitivity should be 400 to 550 Hz. (Sensitivity is the difference between the two frequencies.	Select a value of C3 from those listed in parts list to produce 400- to 550-Hz sensitivity. Step f should be repeated if value of C3 is changed.
	i. Remove bias from test setup.		
	j. Using a dvm, check dc bias at R4-C2 junction. (Refer to figures 7 and 8.)	+2.1 to +2.5 V dc.	Adjust R1, R2, and R3 to nominal values. Adjust R3 for +2.5 V dc at R4-C2 junction.
	k. Place tcxo in temperature box.		
	l. Decrease temperature to 0 °C (+32 °F). Allow time for tcxo to stabilize at this temperature.		
	m. Using the frequency counter, measure the output at P3.	9.9 MHz ±4.0 Hz.	Adjust R2 for 9.9 MHz ±1.0 Hz.
	n. Increase temperature to +25 °C (+77 °F).		
	o. Using the frequency counter, measure the output at P3.	9.9 MHz ±4.0 Hz.	Adjust R3 for 9.9 MHz ±1.0 Hz.
	p. Increase temperature to +75 °C (+167 °F).		
	q. Using the frequency counter, measure the output at P3.	9.9 MHz ±4.0 Hz.	Adjust R1 for 9.9 MHz ±1.0 Hz.
	r. If any adjustments are made repeat steps k thru q.	Continue to step s.	If after several tries adjustment fails to pass at all temperature levels, check RT1, RT2, RT3, Y1, and associated circuit.
	s. Using the frequency counter, measure the output at P3 at each of the following temperatures (allow the tcxo to stabilize at each temperature).		
	0 °C (+32 °F) +10 °C (+50 °F) +25 °C (+77 °F) +45 °C (+113 °F) +60 °C (+140 °F) +70 °C (+158 °F) +75 °C (+167 °F)	9.9 MHz ±4.0 Hz.	Perform adjustments in steps k thru q. If after several tries adjustment fails to pass at all temperature levels, check RT1, RT2, RT3, Y1, and associated circuit.
	t. Remove tcxo from temperature box and reinstall in unit.		



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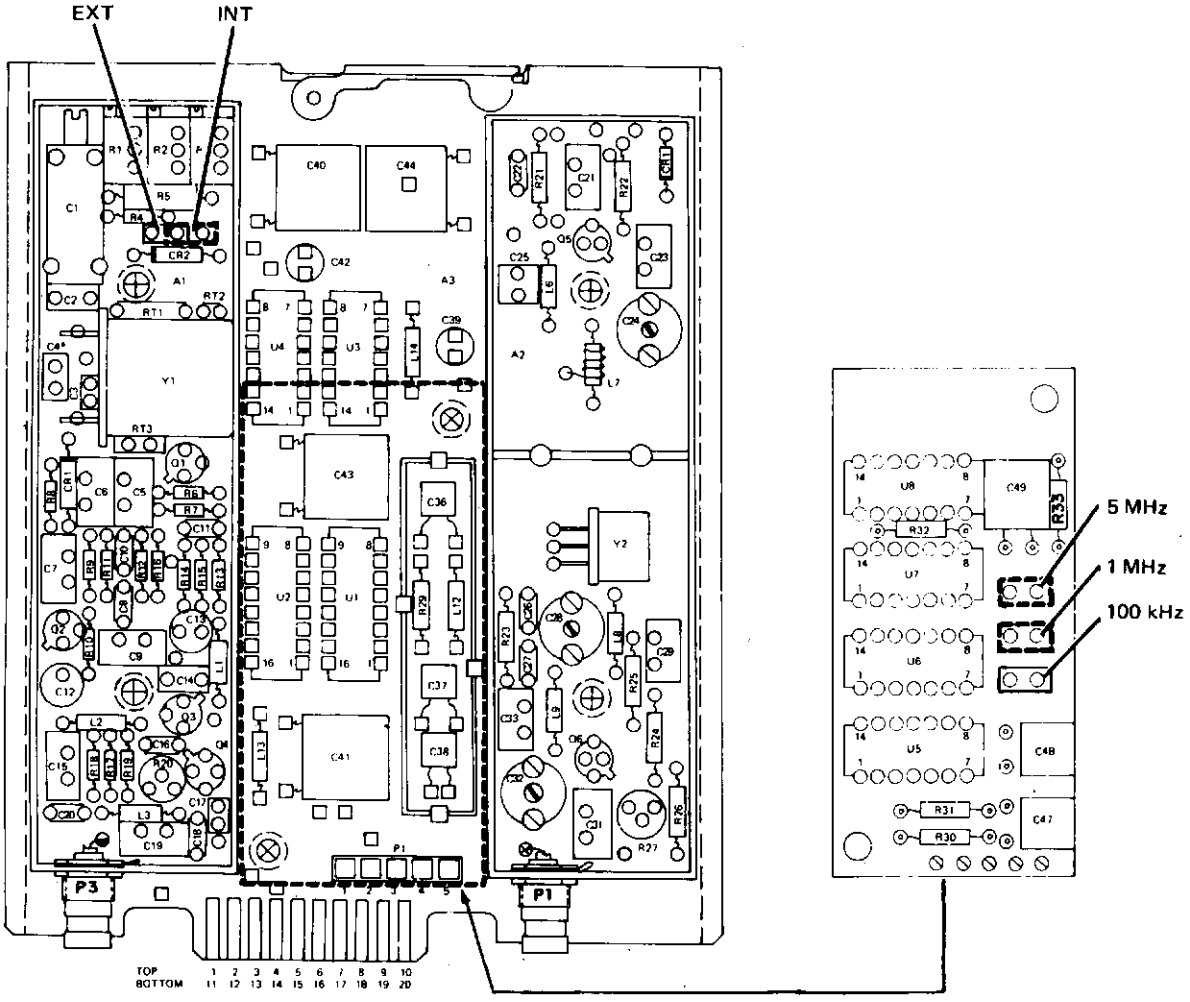
Frequency Adjustment Bias, Test Setup
Figure 7



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Strapping for External Frequency Standard
Figure 8

Table 8. External Phase-Lock, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of the unit containing the external phase-lock that is to be tested.		
	b. Remove cover from the synthesizer section of the unit.		
	c. Remove synthesizer reference (with external phase-lock) and install it on an extender card and place it in the unit.		
	d. Set unit LINE SELECTOR switch to 115 V.		
	e. Connect unit to 115-V ac power source and set power on.		
	f. Measure dc voltage from external phase-lock P1-4 to P1-2 (ground).	+5.2 ±0.2 V dc.	Check unit synthesizer voltage regulator and associated synthesizer reference.
	Note Clip inside tcxo must be in the external position (refer to figure 8).		
2. 5-MHz external reference	a. Set clip on the external phase-lock to the 5-MHz position.		
	b. Connect 5-MHz external standard (0.5 to 1.5 V rms) to J23 EXT STD jack on unit.		
	c. Connect an oscilloscope to U8-8 and observe square wave.	Steady duty ratio, indicating locked condition.	Check U5, U6, U7, and U8.
	d. Ground P1-5 and observe square wave at U8-8.	Unsteady square wave.	Check U8.
	e. Remove P1-5 ground and observe square wave at U8-8.	Steady duty ratio, indicating locked condition.	Check U5, U6, U7, and U8.
3. 1-MHz external reference	a. Set clip on the external phase-lock to the 1-MHz position.		
	b. Connect 1-MHz external standard (0.5 to 1.5 V rms) to J23 EXT STD jack on unit.		
	c. Connect an oscilloscope to U8-8 and observe square wave.	Steady duty ratio, indicating locked condition.	Check U5, U6, and U8.
	d. Ground P1-5 and observe square wave at U8-8.	Unsteady square wave.	Check U8.
	e. Remove P1-5 ground and observe square wave at U8-8.	Steady duty ratio, indicating locked condition.	Check U5, U6, and U8.

Table 8. External Phase-Lock, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. 100-kHz external reference	a. Set clip on the external phase lock to the 100-kHz position.		
	b. Connect 100-kHz external standard (0.5 to 1.5 V rms) to J23 EXT STD jack on unit.		
	c. Connect an oscilloscope to U8-8 and observe square wave.	Steady duty ratio, indicating locked condition.	Check U5 and U8.
	d. Ground P1-5 and observe square wave at U8-8.	Unsteady square wave.	Check U8.
	e. Remove P1-5 ground and observe square wave at U8-8.	Steady duty ratio, indicating locked condition.	Check U5 and U8.

4. REPAIR

Repair of the synthesizer reference module is accomplished using the standard planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

5. PARTS LIST/DIAGRAMS

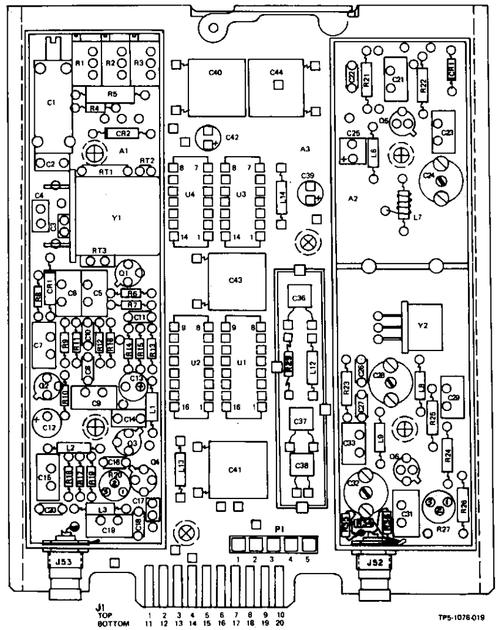
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figures 9 and 10). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

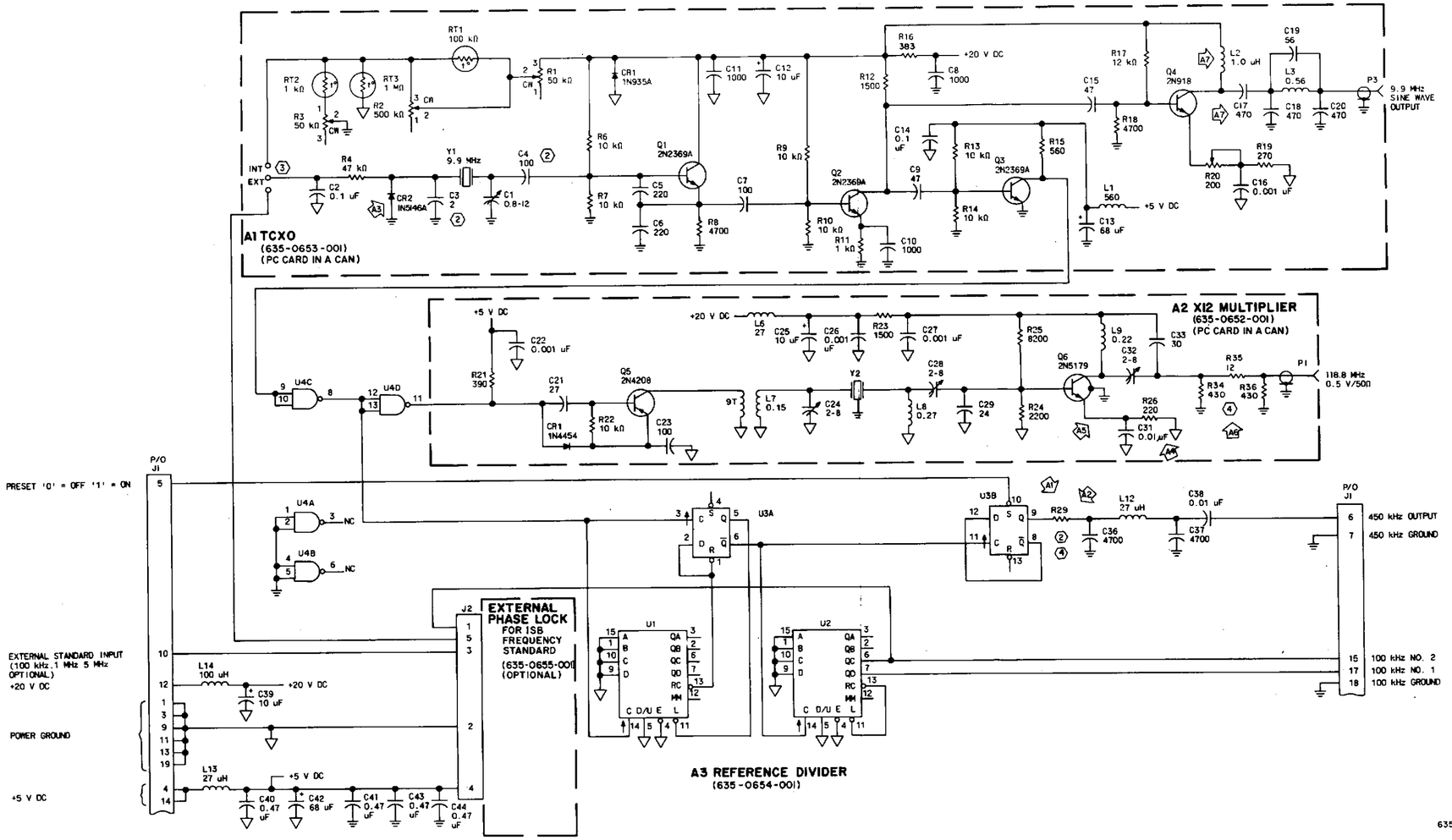
Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Synthesizer reference	623-2085-001	REV E
Times 12 multiplier A2	635-0652-001	REV H
Texo A1	635-0653-001	REV D
Reference divider A3	635-0654-001	REV G
External phase-lock (optional)	635-0655-001	REV D





Synthesizer Reference, Schematic Diagram
Figure 9 (Sheet 1 of 2)

PARTS LIST

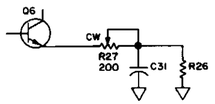
REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	SYNTHESIZER REFERENCE 623-2085-001		
A1	TCXO	635-0653-001	
A2	X12 MULTIPLIER	635-0652-001	
A3	REFERENCE DIVIDER	635-0654-001	
J1-J51	NOT USED		
J52, J53	CONNECTOR, RCPT, ELEC	357-7207-090	
R1-R28	NOT USED		
R29	RESISTOR, FXD, CMPSN (A2) 56Ω thru 180Ω, 5%, 1/4W	635-8926-001	
R30-R33	NOT USED		
R34	RESISTOR, FXD, CMPSN, (A6) 430Ω, 5%, 1/8W	745-1863-400	
R35	RESISTOR, FXD, CMPSN, (A6) 12Ω, 10%, 1/8W	745-2271-000	
R36	RESISTOR, FXD, CMPSN, (A6) 430Ω, 5%, 1/8W	745-1863-400	
	TCXO A1 635-0653-001		
CR1	SEMICOND DEVICE, 1N935A	353-3157-000	
CR2	SEMICOND DEVICE, 1N5147 (A3)	922-6095-170	
CR2	SEMICOND DEVICE, 1N5146A	922-6095-160	
C1	CAPACITOR, VAR, GL DIEL, 0.8 TO 12pF, 750V	922-0487-000	
C2	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C3	CAPACITOR, FXD, CER DIEL, 1.2 THRU 10pF, 5%, 75V	601-3486-001	
C4	CAPACITOR, FXD, MICA DIEL, 82 THRU 220pF, 5%, 50V	601-3485-001	
C5, C6	CAPACITOR, FXD, MICA DIEL, 220pF, 5%, 500V	912-3903-000	
C7	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 500V	912-3879-000	
C8	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C9	CAPACITOR, FXD, MICA DIEL, 47pF, 5%, 500V	912-3856-000	
C10, C11	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C12	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-240	
C13	CAPACITOR, FXD, ELCTLT, 68μF, 20%, 6V	184-9102-040	
C14	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C15	CAPACITOR, FXD, MICA,DIEL, 47pF, 5%, 500V	912-3856-000	
C16	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C17	CAPACITOR, FXD, CER DIEL (A7) 0.01μF, 20%, 50V	913-3279-110	
C17	CAPACITOR, FXD, CER DIEL, 470pF, 10%, 200V	913-4014-000	
C18	CAPACITOR, FXD, CER DIEL, 470pF, 10%, 200V	913-4014-000	
C19	CAPACITOR, FXD, MICA DIEL, 56pF, 5%, 500V	912-3861-000	
C20	CAPACITOR, FXD, CER DIEL, 470pF, 10%, 200V	913-4014-000	
L1	COIL, RF, 560μH	240-2073-050	
L2	COIL, RF, 180μH (A7)	240-2026-000	
L2	COIL, RF, 1.0μH	240-2023-000	
L3	COIL, RF, 0.56μH	240-2020-000	
Q1-Q3	TRANSISTOR, 2N2369A	352-0596-030	
Q4	TRANSISTOR, 2N918	352-0440-000	
RT1	RESISTOR, THRM, 100kΩ, 10%, 4MW	714-1138-010	
RT2	RESISTOR, THRM, 1kΩ, 10%, 2.6MW	714-1138-060	
RT3	RESISTOR, THRM, 1MΩ, 5%, 5.3MW	714-2853-000	
R1	RESISTOR, VAR, 50kΩ, 10%, 1/2W	380-9066-030	
R2	RESISTOR, VAR, 500kΩ, 10%, 1/2W	382-1405-290	
R2	RESISTOR, VAR, 500kΩ, 10%, 1/2W	380-9066-040	
R3	RESISTOR, VAR, 50kΩ, (A), 10%, 1/2W	382-1405-250	
R3	RESISTOR, VAR, 50kΩ, 10%, 1/2W	380-9066-030	
R4	RESISTOR, FXD, CMPSN, 47kΩ, 10%, 1/8W	745-2401-000	
R5	NOT USED		
R6, R7	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/8W	745-2377-000	
R8	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/8W	745-2365-000	
R9, R10	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/8W	745-2377-000	
R11	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/8W	745-2341-000	
R12	RESISTOR, FXD, CMPSN, 1.5kΩ, 10%, 1/8W	745-2347-000	
R13, R14	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/8W	745-2377-000	
R15	RESISTOR, FXD, CMPSN, 560Ω, 10%, 1/8W	745-2332-000	
R16	RESISTOR, FXD, WW, 383Ω, 10%, 1W	747-2183-570	
R17	RESISTOR, FXD, CMPSN, 12kΩ, 10%, 1/8W	745-2380-000	
R18	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/8W	745-2365-000	
R19	RESISTOR, FXD, CMPSN, 270Ω, 10%, 1/8W	745-2320-000	

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
R20	RESISTOR, VAR, 200Ω, 10%, 0.5W	382-0027-050	
Y1	XTAL UNIT, QTZ, 9.900000MHZ	289-7271-010	
	X12 MULTIPLIER A2 635-0652-001		
CR1	SEMICOND DEVICE, 1N4454	353-3644-010	
C1-C20	NOT USED		
C21	CAPACITOR, FXD, MICA DIEL, 27pF, 5%, 500V	912-3844-000	
C22	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C23	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 500V	912-3879-000	
C24	CAPACITOR, VAR, CER DIEL, 2 TO 8pF, 350V	917-1218-000	
C25	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-240	
C26, C27	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C28	CAPACITOR, VAR, CER DIEL, 2 TO 8 pF, 350V	917-1218-000	
C29	CAPACITOR, FXD, MICA DIEL, 24pF, 5%, 500V	912-3843-000	
C30	NOT USED		
C31	CAPACITOR, FXD, MICA DIEL, (A4) 220pF, 5%, 500V	912-3903-000	
C31	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C32	CAPACITOR, VAR, CER DIEL, 2 TO 8 pF, 350V	917-1218-000	
C33	CAPACITOR, FXD, MICA DIEL, 30pF, 5%, 500V	912-3846-000	
L1-L5	NOT USED		
L6	COIL, RF, 27μH	240-2040-000	
L7	COIL, RF, 0.15μH	637-1783-001	
L8	COIL, RF, 0.27μH	240-2016-000	
L9	COIL, RF, 0.22μH	240-2015-000	
Q1-Q4	NOT USED		
Q5	TRANSISTOR, 2N4206	352-0959-020	
Q6	TRANSISTOR, 2N5179	352-0792-020	
R1-R20	NOT USED		
R21	RESISTOR, FXD, CMPSN, 390Ω, 10%, 1/4W	745-0734-000	
R22	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R23	RESISTOR, FXD, CMPSN, 1.5kΩ, 10%, 1/4W	745-0755-000	
R24	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 1/4W	745-0761-000	
R25	RESISTOR, FXD, CMPSN, 8.2kΩ, 10%, 1/4W	745-0782-000	
R26	RESISTOR, FXD, CMPSN, 220Ω, 10%, 1/4W	745-0725-000	
R27	RESISTOR, VAR, 200Ω, 10%, 0.5W, (A5)	382-0027-050	
Y1	NOT USED		
Y2	FILTER, XTAL, BP, 118.8MHZ	293-1315-010	
	REF DIVIDER A3 635-0654-001		
C1-C35	NOT USED		
C36, C37	CAPACITOR, FXD, CER DIEL, 4700pF, 10%, 100V	913-5019-160	
C38	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C39	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-240	
C40, C41	CAPACITOR, FXD, CER DIEL, 0.47μF, 10%, 200V	913-3279-690	
C42	CAPACITOR, FXD, ELCTLT, 68μF, 20%, 6V	184-9102-040	
C43, C44	CAPACITOR, FXD, CER DIEL, 0.47μF, 10%, 200V	913-3279-690	
L1-L11	NOT USED		
L12, L13	COIL, RF, 27μH	240-2040-000	
L14	COIL, RF, 100μH	240-2047-000	
P1	HOUSING, CONN	372-2625-014	
U1, U2	INTEGRATED CKT, SN74LS190N	351-1527-040	
U3	INTEGRATED CKT, SN74LS74N	351-1525-040	
U4	INTEGRATED CKT, 7400N	351-7629-010	

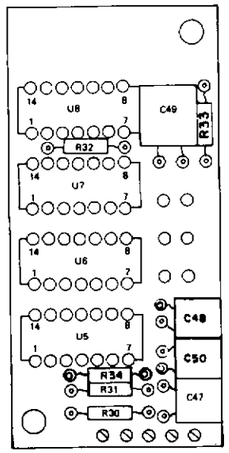
MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
	SYNTH REF 623-2085-001	
A1	Removed A3R29, 47Ω.	635-0654-001, REV C and above
A2	Added R29, test select of 56 to 180Ω (in same location as A3R29 was removed).	623-2085-001, REV C and above
A3	Changed A1CR2 from 1N5147 to 1N5146A.	635-0653-001, REV E and above
A4	Changed A2C31 from 220pF to 0.01μF.	635-0652-001, REV C and above
A5	Removed A2R27, 200Ω variable. Circuit was as shown below.	635-0652-001, REV D and above



A6	Added R34, 430Ω. Added R35, 12Ω. Added R36, 430Ω.	623-2085-001, REV D and above
A7	Changed: C17 from 0.01μF., L2 from 1.8μH to 1.0μH.	635-0653-001, REV F and above
	EXTERNAL PHASE-LOCK 635-0655-001	
A1	Added C50, 0.1μF. Added R34, 2200Ω. Changed R31 from 4700Ω to 2200Ω.	REV C and above

Synthesizer Reference, Schematic Diagram
Figure 9 (Sheet 2)



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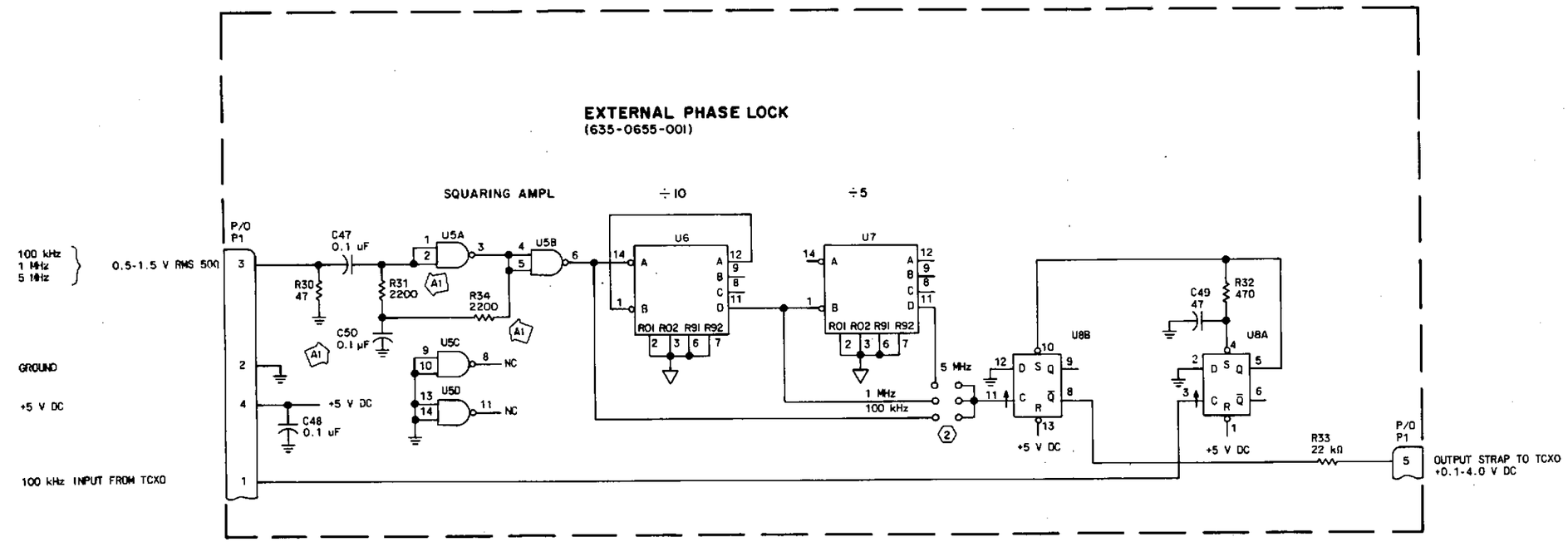


POWER AND GROUND CONNECTIONS

U NO.	TYPE	POWER (V DC)	
		+5	GND
U5	N74LS00A	14	7
U6, U7	SN74LS90N	5	10
U8	SN74LS74N	14	7

(1) UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN PICOFARADS.

(2) OPTIONAL STRAPPING CLIP.

(3) PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.

635-0430 SH 2

External Phase-Lock, Schematic Diagram
Figure 10 (Sheet 1 of 2)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	EXTERNAL PHASE LOCK (OPTION) 635-0655-001		
C1-C46	NOT USED		
C47, C48	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C49	CAPACITOR, FXD, MICA DIEL, 47pF, 5%, 500V	912-3856-000	
C50	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
	(A1)		
R1-R29	NOT USED		
R30	RESISTOR, FXD, CMPSN, 47Ω, 10%, 1/4W	745-0701-000	
R31	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
	(A1)		
R31	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 1/4W	745-0761-000	
R32	RESISTOR, FXD, CMPSN, 470Ω, 10%, 1/4W	745-0737-000	
R33	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R34	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 1/4W	745-0761-000	
	(A1)		
U1-U4	NOT USED		
U5	INTEGRATED CKT, N74LS00A	351-1523-110	
U6, U7	INTEGRATED CKT, SN74LS90N	351-1636-010	
U8	INTEGRATED CKT, SN74LS74N	351-1525-040	

External Phase-Lock, Schematic Diagram
Figure 10 (Sheet 2)

Synthesizer End Decade (635-0657-001)

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

523-0767973-101211
1 June 1977
1st Revision, 1 June 1978

1. DESCRIPTION

Synthesizer End Decade 635-0657-001, shown in figure 1, is a 2-layer planar card with a 20-pin edge-on connector (2-layers, 10 pins each).

The synthesizer end decade consists of a logic circuit, a low-pass filter circuit, a vco circuit, a loss-of-lock (LOL) monitor circuit, and a divide-by-10 output circuit.

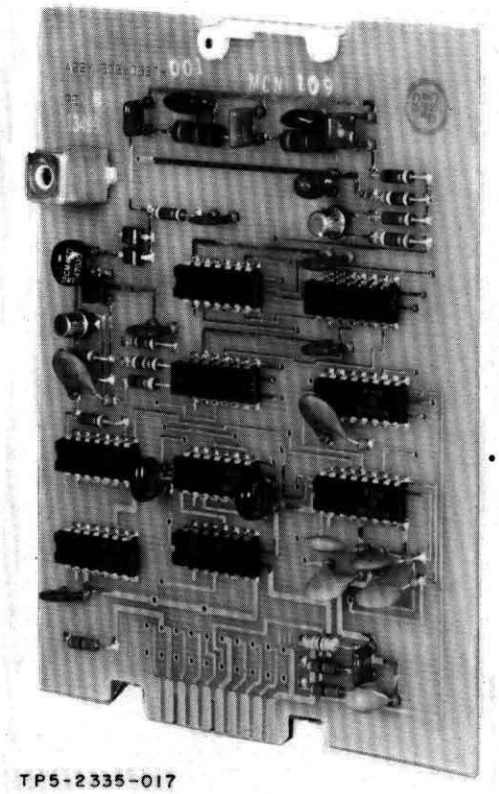
2. PRINCIPLES OF OPERATION

2.1 General (Refer to figure 2.)

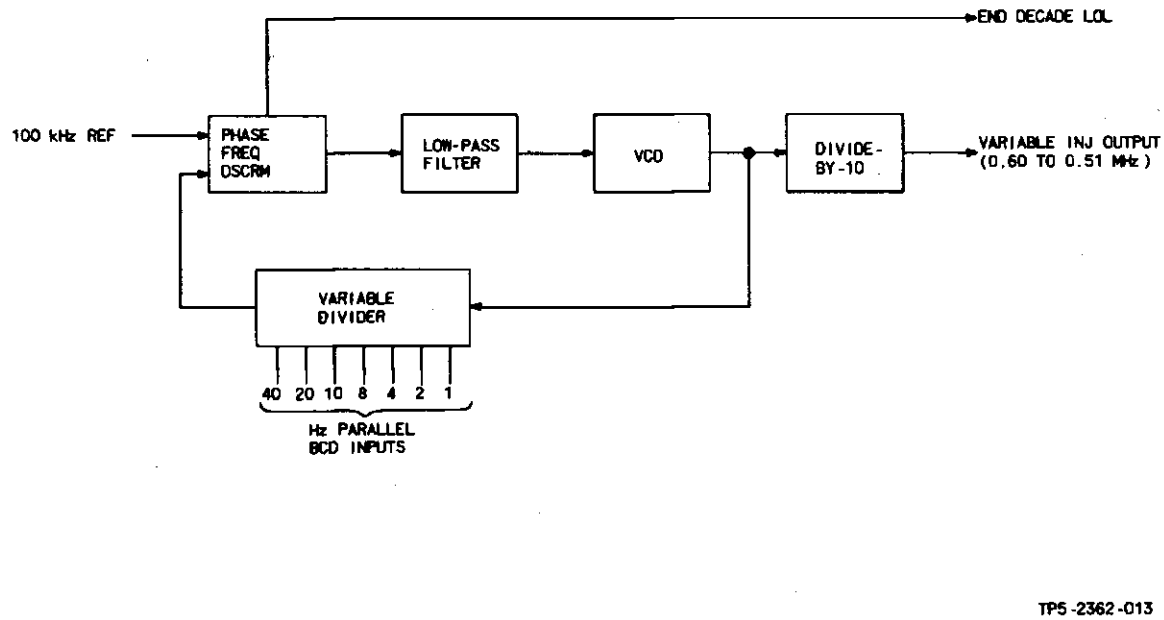
The synthesizer end decade receives 100/10/1-Hz bcd frequency control signals and a 100-kHz reference signal, and generates a 6.0- to 5.1-MHz variable frequency output and a lock signal output (logic 1 for lock).

The logic circuits receive a 100-kHz reference input and a bcd frequency input. The bcd frequency input is used to program a variable frequency divider (divide-by-60 to divide-by-51). The programmed variable divider output (100 kHz) and the 100-kHz reference input are supplied to a phase/frequency discriminator that provides a control voltage proportional to the phase/frequency difference between its inputs.

The vco circuit receives the control voltage signal from the logic circuits and is driven to and locked at the variable frequency as programmed by the variable divider bcd inputs to the logic circuits. The vco output (6.0 to 5.1 MHz) is supplied to the logic circuits for clocking and lock signal generation. The vco output (6.0 to 5.1 MHz) is supplied through a divide-by-10 circuit to rf circuits for additional frequency mixing and generation.



Synthesizer End Decade
Figure 1



Block Diagram
Figure 2

2.2 Logic Circuits

The logic circuits receive a 100-kHz reference input, a vco signal output, and bcd frequency inputs, and supplies a control voltage output signal to the vco.

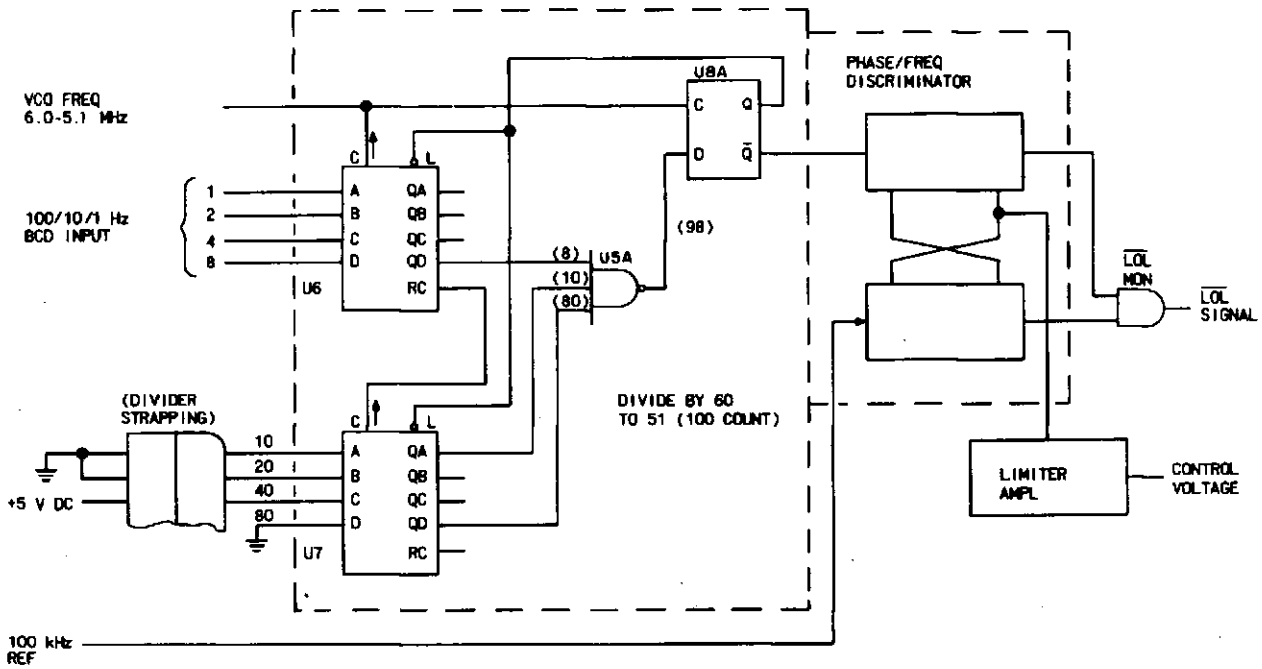
Refer to figure 3. The vco signal output (6.0 to 5.1 MHz) is supplied as the clock input to a programmable variable divider. The output of the programmable variable divider (100 kHz) is supplied to a phase/frequency discriminator and is compared with a 100-kHz reference input. A phase or frequency difference in the discriminator causes a control voltage input increase or decrease to adjust the frequency of the vco. If there is no phase or frequency difference, the discriminator provides a logic 1 lock signal output indicating the vco frequency is locked.

The programmable variable divider is programmed by the bcd frequency inputs. For example, if a bcd input of 0 is applied, the up/down decade counter is programmed to load the count 40 at any time a load signal (logic 0) is applied. Refer to table 1. This programs the variable divider to count from 40 (first count 41) to 100 (last count 100/40).

This causes the output of the variable divider to be 1/60th of the clock input or a divide-by-60 with a bcd input of 0. Note as the bcd input goes up 1, 2, 3, etc, the division ratio goes down -59, -58, -57, etc. Also note, that for the divide-by-circuit to operate as a constant, the last clock 100 must also be the loaded count (in the case of bcd 0, count 40). To do this, prerecognition of count 100 is required. Look-ahead circuit U5A performs this function. At clock 58 (count 98) gate U5A is NANDed and supplies a logic 0 input to U8A-D. With a logic 0 at U8A-D, clock 59 (count 99) causes U8A-Q to go to logic 1 and loads decade counter to bcd input (NANDed output of U5A is removed). At clock 59, U8A-$\overline{Q}$ supplies a pulse to phase/frequency discriminator. Clock 60 (count 40) causes U8A-Q to go to logic 0 and enables decade counter to count on the next clock. Next clock is one above the bcd programmed input. Note that count 99 initiates the output from the divider and count 100 appears only as the bcd programmed input. Refer to figure 4. A 500-Hz programmed input is shown, the same principles apply to any other programmed bcd input.

2.3 VCO Circuits

The vco circuits receive a control voltage from the logic circuits. The control voltage drives the vco to the required vco frequency. The vco signal output is supplied through one buffer amplifier to the logic circuits and through a fixed divide-by-10 output circuit to the unit under control for additional frequency mixing and generation.

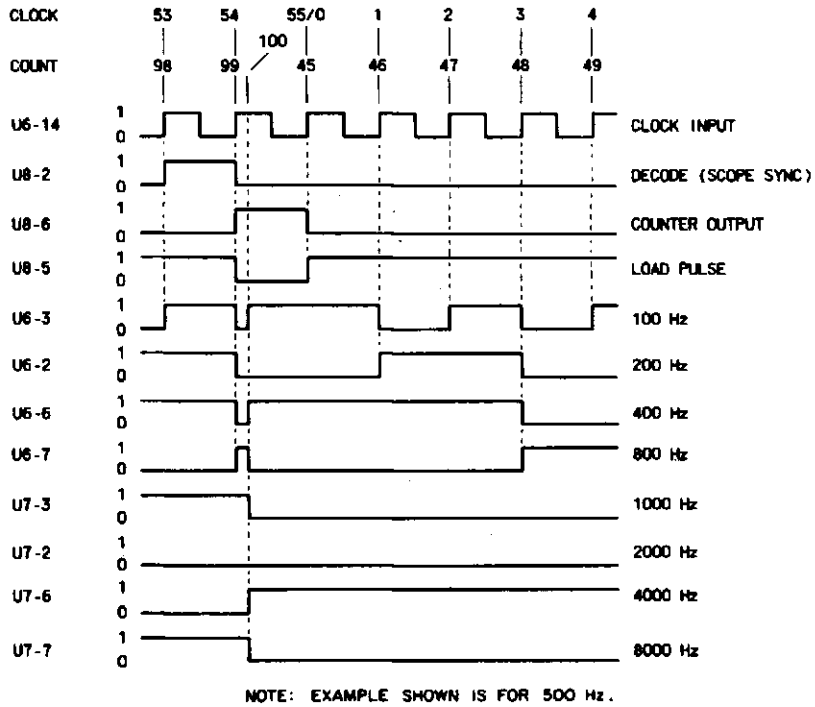


Logic Circuit
Figure 3

Table 1. Variable Divider, Logic Truth Table.

BCD INPUT (100/10/1 Hz)	DIVIDER INPUTS								OUTPUT COUNT	DIVIDE BY	LOOP FREQ (MHz)
	U6				U7						
	A	B	C	D	**A	**B	[1]C	*D			
0	0	0	0	0	0	0	1	0	40	60	6.0
1	1	0	0	0	0	0	1	0	41	59	5.9
2	0	1	0	0	0	0	1	0	42	58	5.8
3	1	1	0	0	0	0	1	0	43	57	5.7
4	0	0	1	0	0	0	1	0	44	56	5.6
5	1	0	1	0	0	0	1	0	45	55	5.5
6	0	1	1	0	0	0	1	0	46	54	5.4
7	1	1	1	0	0	0	1	0	47	53	5.3
8	0	0	0	1	0	0	1	0	48	52	5.2
9	1	0	0	1	0	0	1	0	49	51	5.1

*Internally strapped for logic 0 (ground).
**Externally strapped for logic 0 (ground) at pins 7 and 17.
[1]Externally strapped for logic 1 (+5.2 V dc) at pin 16.



PROGRAMMED BCD INPUTS		
MHz	PIN NO.	LOGIC LEVEL
1	U6-15	1
2	U6-1	0
4	U6-10	1
8	U6-9	0
10	U7-15	FXD 0
20	U7-1	FXD 0
40	U7-10	FXD 1
80	U7-9	FXD 0

TP5-2366-013

Variable Divider, Inputs and Outputs
Figure 4

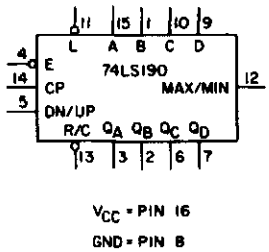
2.4 Up/Down Decade Counter 74LS190 (Refer to table 2.)

The 74LS190 up/down decade counter is a 4-bit decade counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when input conditions are met.

A high at the enable input inhibits counting. A low at the enable input and a low-to-high clock transition triggers the four master/slave flip-flops. The enable input should be changed only when the clock is high. The down/up input determines the direction of the count. When low, the count goes up; when high, the count goes down.

These counters are programmable. The outputs may be preset to any state by placing a low on the load input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the state of the clock input. This allows the counters to be used as modulo-N dividers by modifying the count length with the preset inputs.

Two outputs are available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high level output



TP5-2325-013

Up/Down Decade Counter 74LS190
Figure 5

pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low level output pulse equal in width to the low level portion of the clock input when an overflow or underflow condition exists. The counters are cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Table 2. Up/Down Decade Counter 74LS190, Logic Truth Table.

PROGRAMMABLE INPUTS				COUNT	BCD OUTPUTS			
A	B	C	D		QA	QB	QC	QD
0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	0	0	0
0	1	0	0	2	0	1	0	0
1	1	0	0	3	1	1	0	0
0	0	1	0	4	0	0	1	0
1	0	1	0	5	1	0	1	0
0	1	1	0	6	0	1	1	0
1	1	1	0	7	1	1	1	0
0	0	0	1	8	0	0	0	1
1	0	0	1	9	1	0	0	1

E (enable): logic 0 enables counter; logic 1 inhibits counter.

L (load): logic 0 programs the bcd output count to be set at the bcd count of the programmable inputs; the next clock pulse counts one higher/lower (up/down).

DU (down/up): logic 0 counts up; logic 1 counts down.

CP (clock pulse): logic 0-to-logic 1 transition advances counter.

RC (ripple clock): logic 0 pulse equal to 1/2 clock cycle when an overflow occurs.

MM (maximum/minimum count): logic 1 pulse equal to full clock cycle when an overflow or underflow occurs.

2.5 Decade Counter 74LS90 (Refer to table 3.)

The 74LS90 decade counter is a high-speed, monolithic decade counter consisting of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-2 counter and a divide-by-5 counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logical 0 or to a binary coded decimal (bcd) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

a. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the bcd count sequence truth table shown above. In addition to a conventional 0 reset, inputs are provided to reset a bcd 9 count for 9's complement decimal applications.

b. If a symmetrical divide-by-10 count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of 10, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-10 square wave is obtained at output A.

c. For operation as a divide-by-2 counter and divide-by-5 counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-2 function. The BD input is used to obtain binary divide-by-5 operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

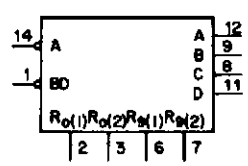
Table 3. Decade Counter 74LS90, Logic Truth Table.

*BCD COUNT SEQUENCE				
COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

**RESET/COUNT							
RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	Count			
0	X	0	X	Count			
0	X	X	0	Count			
X	0	0	X	Count			

*Output A connected to input BD for BCD count.
**X indicates that either a logical 1 or a logical 0 may be present.

LOGIC SYMBOL



TP5-2326-012

Decade Counter 74LS90
Figure 6

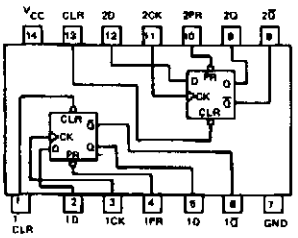
2.6 Dual D-Type Flip-Flop With Preset and Clear 74LS74 (Refer to table 4.)

The 74LS74 consists of dual, high-speed, D-type flip-flops. Information on the D input is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either high or low level, the D-input signal has no effect.

Table 4. Dual D-Type Flip-Flop With Preset and Clear 74LS74, Logic Truth Table.

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	*H	*H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_O	$\overline{Q_O}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_O = the level of Q before the indicated input conditions were established.
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.



Dual D-Type Flip-Flop With Preset and Clear 74LS74
Figure 7

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the synthesizer end decade are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 5 check total performance of the synthesizer end decade. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

Table 5. Synthesizer End Decade, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of the unit containing the synthesizer end decade that is to be tested.		
	b. Remove cover from the synthesizer section of the unit.		
	c. Remove synthesizer end decade, install it on an extender card, and place it in the unit.		
	d. Set unit LINE SELECTOR switch to 115 V.		
(Cont)	e. Connect unit to 115-V ac power source and set power on.		

Table 5. Synthesizer End Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. (Cont)	f. Measure dc voltage from P1-20 and P1-2 to P1-6 (ground).	+5.2 ±0.2 V dc.	Check unit synthesizer voltage regulator.
	g. Measure dc voltage from P1-10 to P1-6 (ground).	NLT +19.5 V dc, NMT +20.8 V dc.	Check unit synthesizer voltage regulator.
2. Test procedures	a. Set the end frequency control to 9.		
	b. Measure dc voltage at cathode end of CR1-CR2. (Refer to figure 8 for CR1-CR2 cathode location.)	9.5 ±0.1 V dc.	Adjust L6 for 9.5 ±0.1 V dc. If L6 adjustment does not correct the problem, check Q1, Q2, and associated circuit.
	c. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	510 ±0.5 kHz.	Adjust L6 for 510 kHz with 10.0 ±0.1 V dc at cathode end of CR1-CR2. If L6 adjustment does not correct the problem, check Q1, Q2, and associated circuit.
	d. Note the frequency counter reading while moving the frequency control from 9 down to 0. (Refer to chart below.)	Note that the frequency reading increases by 10 kHz with each step of the frequency control. Reading should be 600 ±0.5 kHz with frequency control at 0.	Check U6, U7, U8, and associated circuits.
	e. Measure the dc voltage at P1-12.	NLT +3.5 V dc. **Note** RCV FAULT, EXCTR FAULT, or R/E FAULT indicator lighting indicates that result of step f is satisfactory.	Check U3, U4, and U5.
(Cont)	f. Ground P1-5 while noting the voltage of P1-12.	NMT 0.5 V dc.	Check U1, U2, U3, U4, and U5.

Table 5. Synthesizer End Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE			NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	g. Remove P1-5 ground.				
	LOW END FREQ DIGIT	CR1-CR2 DC VOLTAGE	FREQ OUTPUT P1-1 (kHz)		
	9	9.5 ±0.1	510 ±0.5		
	8	10.0 ±0.1	520 ±0.5		
	7	10.5 ±0.1	530 ±0.5		
	6	11.0 ±0.1	540 ±0.5		
	5	11.5 ±0.1	550 ±0.5		
	4	12.0 ±0.1	560 ±0.5		
	3	12.5 ±0.1	570 ±0.5		
	2	13.0 ±0.1	580 ±0.5		
	1	13.5 ±0.1	590 ±0.5		
	0	14.0 ±0.1	600 ±0.5		

4. ALIGNMENT/ADJUSTMENT

Refer to table 5 for adjustment of L6. Perform test 2, steps a through c.

5. REPAIR

Repair of the synthesizer end decade is accomplished using the standard planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

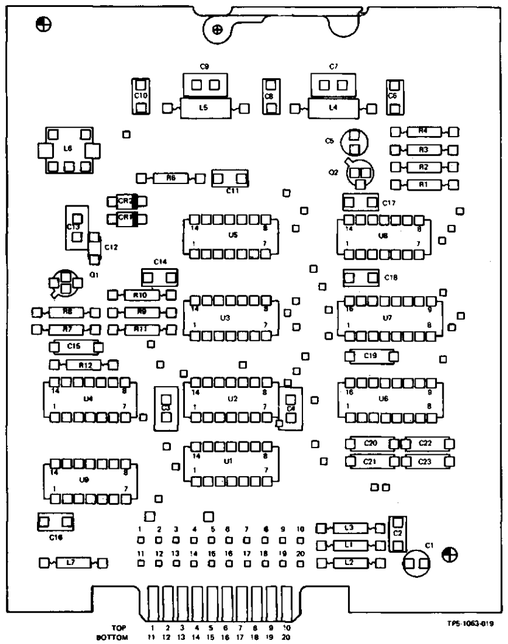
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram, figure 8. The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

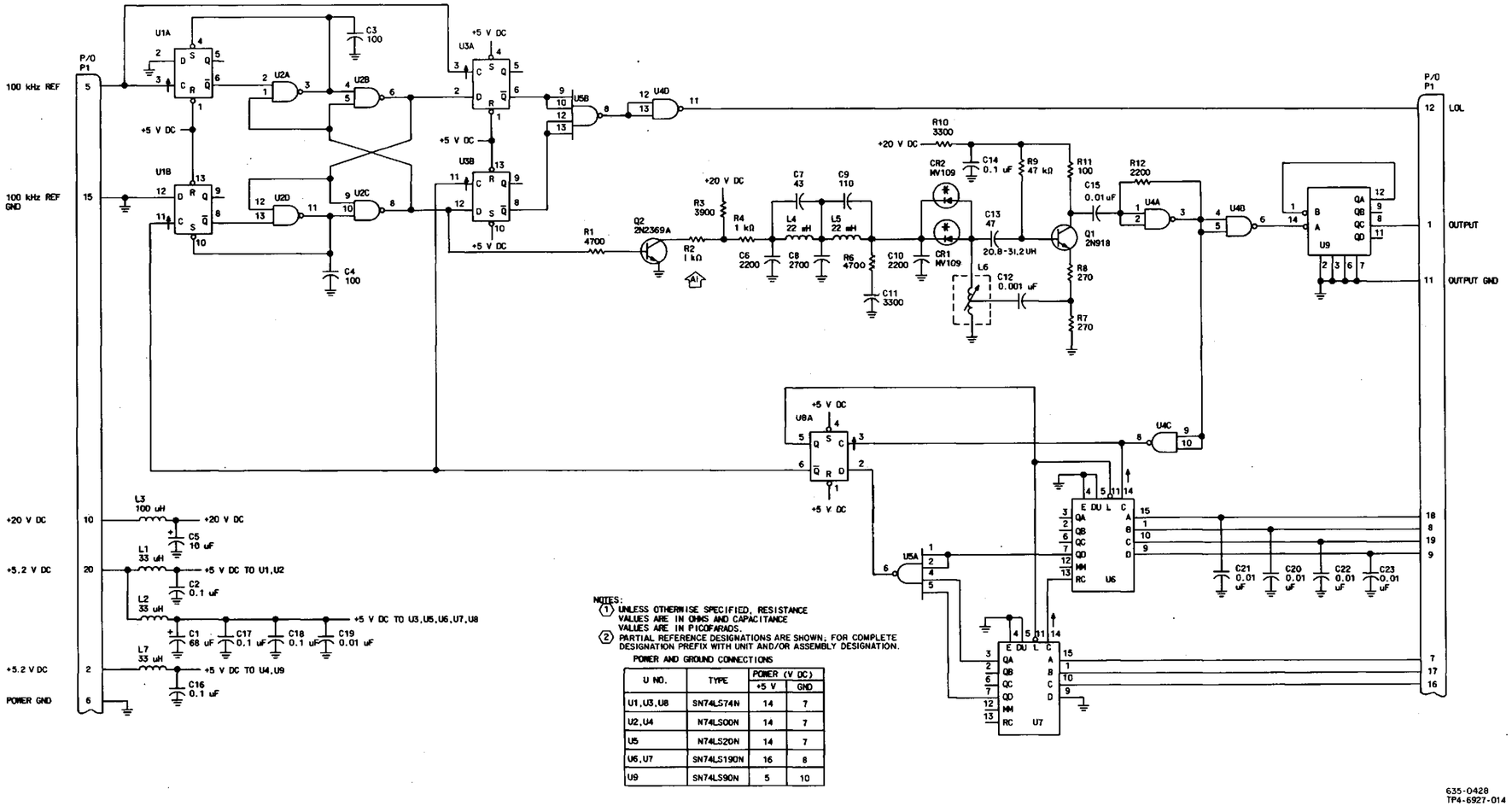
Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description is listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Synthesizer end decade	635-0657-001	REV C





NOTES:
1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN PICOFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.

POWER AND GROUND CONNECTIONS

U NO.	TYPE	POWER (V DC) +5 V	GND
U1,U3,U8	SN74LS74N	14	7
U2,U4	N74LS00N	14	7
U5	N74LS20N	14	7
U6,U7	SN74LS190N	16	8
U9	SN74LS90N	5	10

Synthesizer End Decade, Schematic Diagram
Figure 8 (Sheet 1 of 2)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	SYNTH END DECADE 635-0657-001		
CR1, CR2	SEMICOND DEVICE, MV109	922-6124-040	
C1	CAPACITOR, FXD, ELCTLT, 68μF, 20%, 6V	184-9102-040	
C2	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C3, C4	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 500V	912-3879-000	
C5	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-240	
C6	CAPACITOR, FXD, CER DIEL, 2200pF, 5%, 100V	913-3281-300	
C7	CAPACITOR, FXD, MICA DIEL, 43pF, 5%, 500V	912-3854-000	
C8	CAPACITOR, FXD, CER DIEL, 0.0027μF, 5%, 100V	913-3117-130	
C9	CAPACITOR, FXD, MICA DIEL, 110pF, 5%, 500V	912-3882-000	
C10	CAPACITOR, FXD, CER DIEL, 2200pF, 5%, 100V	913-3281-300	
C11	CAPACITOR, FXD, CER DIEL, 3300pF, 10%, 100V	913-3281-170	
C12	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C13	CAPACITOR, FXD, MICA DIEL, 47pF, 5%, 500V	912-3856-000	
C14	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C15	CAPACITOR, FXD, CER DIEL, 0.01μF, -20%+80%, 100V	913-3680-000	
C16-C18	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C19-C23	CAPACITOR, FXD, CER DIEL, 0.01μF, -20%+80%, 100V	913-3680-000	
L1, L2	COIL, RF, 33μH	240-2041-000	
L3	COIL, RF, 100μF	240-2047-000	
L4, L5	COIL, RF, 22000 μH	240-2715-850	
L6	INDUCTOR, RF, VAR, 20.6-31.2μH	242-0441-050	
L7	COIL, RF, 33μH	240-2041-000	
Q1	TRANSISTOR, 2N918	352-0440-000	
Q2	TRANSISTOR, 2N2369A	352-0596-030	
R1	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R2	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 1/4W (A1)	745-0761-000	
R2	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W (A1)	745-0749-000	
R3	RESISTOR, FXD, CMPSN, 3.9kΩ, 10%, 1/4W	745-0770-000	
R4	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W	745-0749-000	
R5	NOT USED		
R6	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R7, R8	RESISTOR, FXD, CMPSN, 270Ω, 10%, 1/4W	745-0726-000	
R9	RESISTOR, FXD, CMPSN, 47kΩ, 10%, 1/4W	745-0809-000	
R10	RESISTOR, FXD, CMPSN, 3.3kΩ, 10%, 1/4W	745-0767-000	
R11	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R12	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 1/4W	745-0761-000	
U1	INTEGRATED CKT, SN74LS74N	351-1525-040	
U2	INTEGRATED CKT, N74LS00N	351-1523-110	
U3	INTEGRATED CKT, SN74LS74N	351-1525-040	
U4	INTEGRATED CKT, N74LS00N	351-1523-110	
U5	INTEGRATED CKT, N74LS20N	351-1523-130	
U6, U7	INTEGRATED CKT, SN74LS190N	351-1527-040	
U8	INTEGRATED CKT, SN74LS74N	351-1525-040	
U9	INTEGRATED CKT, SN74LS90N	351-1636-010	

MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Changed R2 from 2200Ω to 1kΩ.	REV C and above

Synthesizer End Decade, Schematic Diagram
Figure 8 (Sheet 2)

Synthesizer Decade (623-2080-001, -002, -003, -004)

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

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1 June 1977
2nd Revision, 1 January 1979

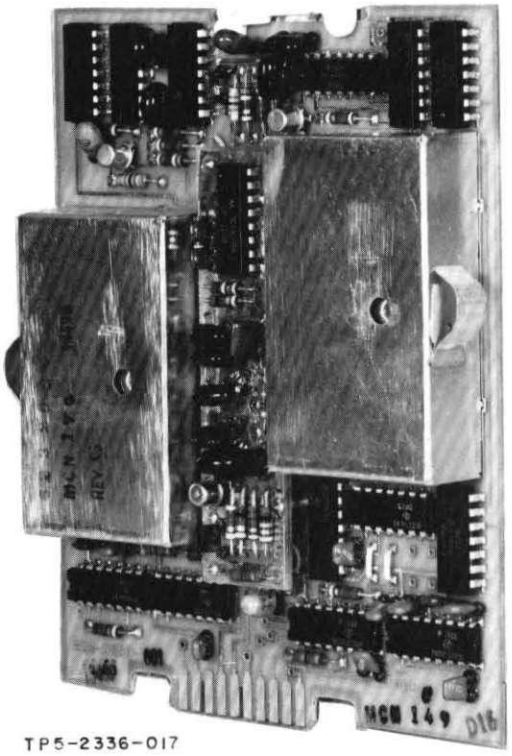
1. DESCRIPTION.

Synthesizer Decades 623-2080-001, -002, -003, -004, shown in figure 1 and listed in table 1, are 2-layer planar cards with 20-pin edge-on connectors (2 layers, 10 pins each). The modules differ only in strapping and frequency control/output, as indicated on the schematic, figure 14.

Table 1. Cards Covered by These Instructions.

CARD TYPE	COLLINS PART NO
100-kHz synthesizer decade	623-2080-001
10-kHz synthesizer decade	623-2080-002
1-kHz synthesizer decade	623-2080-003
100/10-Hz synthesizer decade	623-2080-004

The synthesizer decade module consists of translator logic, translator vco, output mixer, output logic, output vco, low-pass filter circuits, a divide-by-10 output circuit, and a loss-of-lock (LOL) monitor circuit.



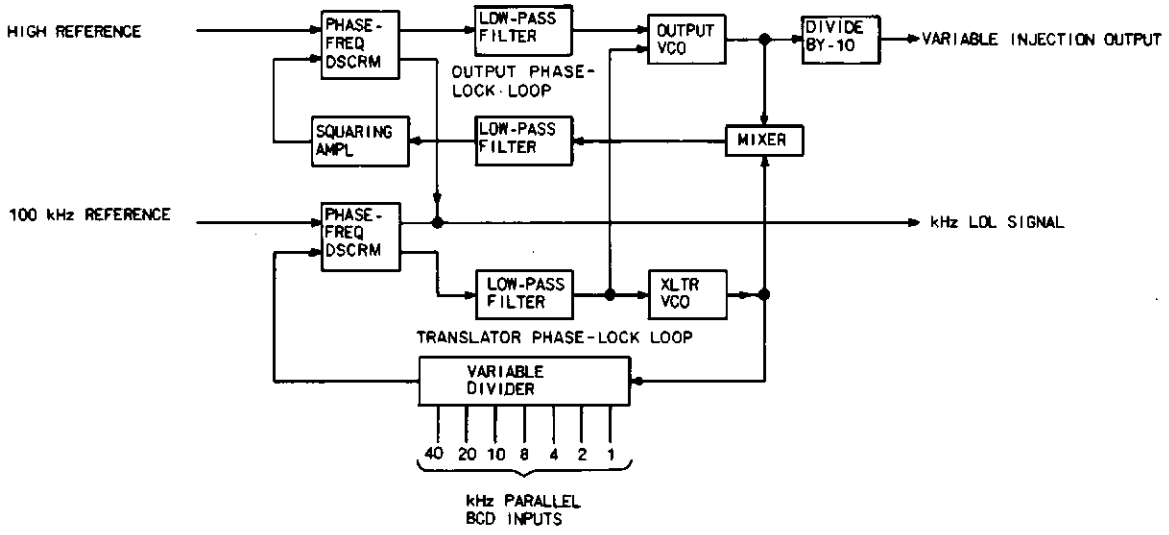
Synthesizer Decade
Figure 1

2. PRINCIPLES OF OPERATION

2.1 General (Refer to figure 2.)

The synthesizer decade module receives bcd frequency control signals, a 100-kHz reference signal, and a high-reference signal, and generates a variable injection signal output and a lock signal output (logic 1 for lock). The variable injection signal output is used as the high-reference signal in the next frequency step in the generation of a 79.35001- to 109.35-MHz variable injection signal output.

The translator logic circuits receive a 100-kHz reference input, a translator vco signal, and a bcd frequency input. The bcd frequency input is used to



Synthesizer Decade, Block Diagram
Figure 2

program a variable frequency divider (division ratio depends on strapping and bcd inputs). The programmed variable frequency divider output (100 kHz) and the 100-kHz reference input are supplied to a phase/frequency discriminator that provides a control voltage proportional to the phase/frequency difference between its inputs.

The translator vco circuit receives the control voltage signal from the translator logic circuits and is driven to and phase-locked at the variable frequency as programmed by the variable divider bcd inputs to the translator logic circuits. The translator vco output is supplied to the translator logic circuits for clocking and lock signal generation. The translator vco output is supplied to the output mixer circuits for frequency mixing.

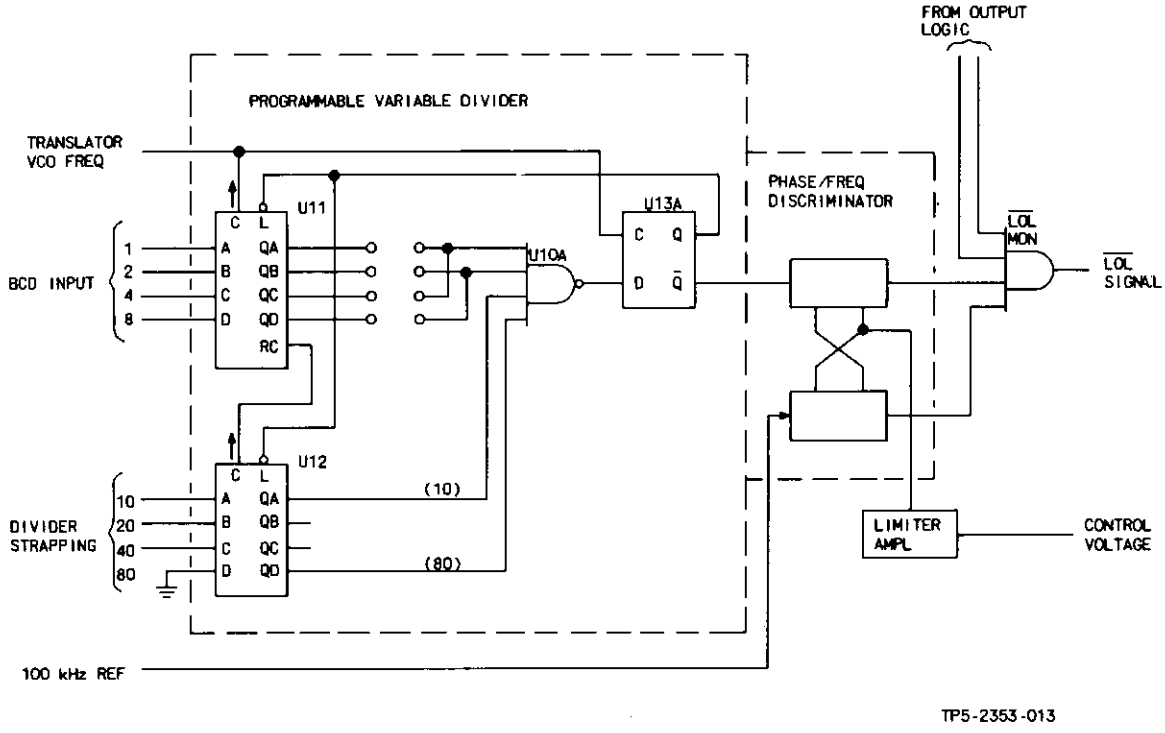
The output mixer circuit receives the translator signal input and the output vco signal input, mixes them, and supplies a reference input to the phase/frequency discriminator. In the phase/frequency discriminator the mixer reference input is compared with the high-reference input and produces an output control voltage.

The output vco circuit receives the output control voltage signal from the output logic circuits and the translator tracking voltage from the translator vco circuits. The translator tracking voltage provides a reference voltage for the output vco, and the output control voltage drives the output vco until it is locked at the variable injection frequency. The output vco output is supplied to a fixed divide-by-10 output circuit. The fixed divide-by-10 circuit output is supplied as a reference to the following decade or output module.

2.2 Translator Logic Circuits

The translator logic circuits receive a 100-kHz reference input, a translator vco signal output, and bcd frequency inputs, and supplies a control voltage output signal to the translator vco.

Refer to figure 3. The translator vco signal output (table 2) is supplied as the clock input to a programmable variable divider. The output of the programmable variable divider (100 kHz) is supplied to a phase/frequency discriminator and is compared with a 100-kHz reference input. A phase or frequency difference in the discriminator causes a control voltage input increase or decrease to adjust the frequency of the vco. If there is no phase or frequency difference, the discriminator provides a logic 1 lock signal output indicating the vco frequency is locked.



Translator Logic Circuits
Figure 3

Table 2. Decade Versus VCO Inputs/Outputs.

DECADE	TRANSLATOR VCO FREQ (MHz)	HIGH REF INPUT FREQ TO OUTPUT VCO (MHz)	OUTPUT VCO FREQ BEFORE DIVIDER (MHz)
100 kHz	9.5 to 8.6	0.85 to 0.750001	10.35 to 9.350001
10 kHz	7.8 to 6.9	0.70 to 0.60001	8.50 to 7.50001
1 kHz	6.4 to 5.5	0.60 to 0.5001	7.00 to 6.0001
100 Hz	5.4 to 4.5	0.60 to 0.501	6.00 to 5.001
10 Hz	5.4 to 4.5	0.60 to 0.51	6.00 to 5.01

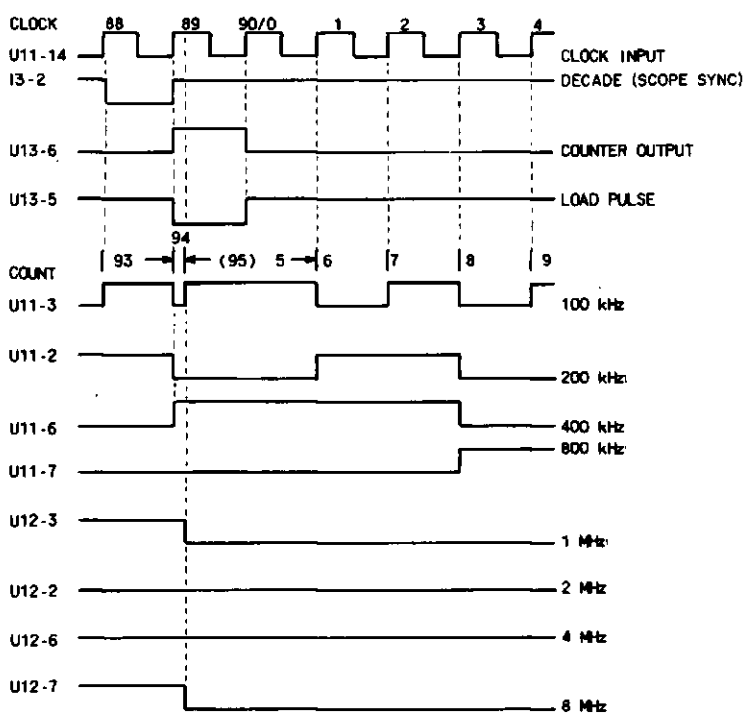
Note

The above high-reference inputs are shown as they would be in a 1-Hz tuned synthesizer. In a 10-Hz tuned synthesizer, there would be no 10-Hz decade and the 100-Hz high-reference input would be 0.60 to 0.51 MHz, the 1-kHz high-reference input would be 0.60 to 0.501 MHz, etc. In a 100-Hz tuned synthesizer, there would be no 100-Hz decade and the 1-kHz high reference would be 0.60 to 0.51 MHz, the 10-kHz high reference would be 0.70 to 0.601 MHz, etc. Output vco frequency at 100-kHz output has the following tuning characteristics.

9.35	0	0	0	1
100 kHz 10 kHz	kHz	100 Hz	10 Hz	Hz

The programmable variable divider is programmed by the bcd frequency inputs. Refer to table 3. For example, if a bcd input of 0 is applied, the up/down decade counter is programmed to load the count 0 at any time a load signal (logic 0) is applied. This programs the variable divider to count from 0 (first count 1) to 95 (last count 95/0). This causes the output of the variable divider to be 1/95th of the clock input or a divide-by-95 with a bcd input of 0. Note that, as the bcd input goes up 1, 2, 3, etc, the division ratio goes down -94, -93, -92, etc. Also note that, for the divide-by circuit to operate as a constant, the last count 95 also must be the loaded count (in the case of bcd 0, count 0). To do this, prerecognition of count 95 is required. Look-ahead circuit of U10A performs this function. At clock 93 (count 93), gate U10A is ANDed and supplies a logic 0 input to U13A-D. With a logic 0 at U13A-D, clock 94 (count 94) causes U13A-$\overline{Q}$ to go to logic 0 and loads decade counter to bcd input (ANDed output U10A is removed). At clock 94, U13A-Q supplies a pulse to the phase/frequency discriminator. Clock 95 (count 00) causes U13A-Q to go to logic 1 and enables decade counter to count on the next clock. Next clock is one above the bcd programmed input. Note that count 94 initiates the output from the divider and count 95 appears only as the bcd programmed input. Refer to figure 4. A 500-kHz programmed input is shown; the same principles apply to any other programmed bcd input.

The preceding discussion pertained to the 100-kHz decade card. Differences between the cards can be seen in figures 5 through 8 and tables 3 through 6. Note that the internal strapping changes and the external input divider strapping changes cause a change in the programmable variable divider.



PROGRAMMED BCD INPUTS		
100 kHz	PIN NO.	LOGIC LEVEL
1	U11-15	1
2	U11-1	0
4	U11-10	1
8	U11-9	0
10	U12-15	FXD 0
20	U12-1	FXD 0
40	U12-10	FXD 0
80	U12-9	FXD 0

NOTE:
EXAMPLE SHOWN IS FOR 500 kHz.

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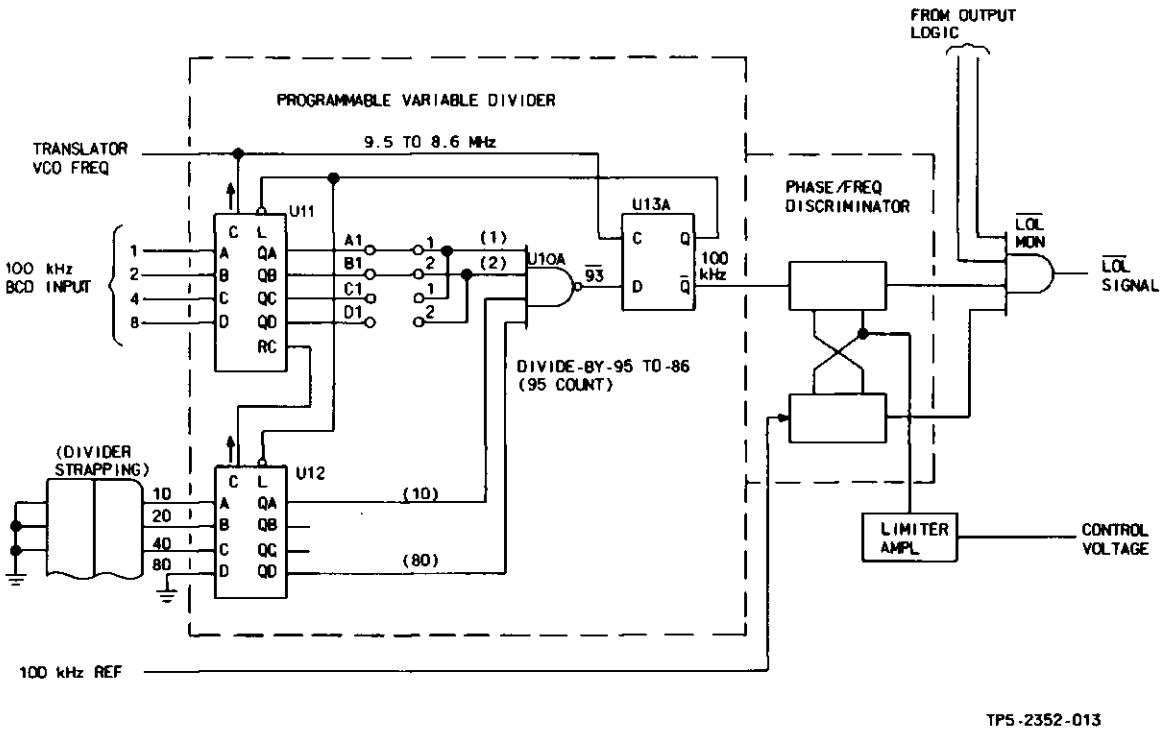
Variable Divider, Inputs and Outputs
Figure 4

Table 3. 100-kHz Decade, Logic Truth Table.

BCD INPUT (100 kHz)	DIVIDER INPUTS								OUTPUT COUNT	DIVIDE-BY	LOOP FREQ (MHz)
	U11				U12						
	A	B	C	D	**A	**B	**C	*D			
0	0	0	0	0	0	0	0	0	0	95	9.5
1	1	0	0	0	0	0	0	0	1	94	9.4
2	0	1	0	0	0	0	0	0	2	93	9.3
3	1	1	0	0	0	0	0	0	3	92	9.2
4	0	0	1	0	0	0	0	0	4	91	9.1
5	1	0	1	0	0	0	0	0	5	90	9.0
6	0	1	1	0	0	0	0	0	6	89	8.9
7	1	1	1	0	0	0	0	0	7	88	8.8
8	0	0	0	1	0	0	0	0	8	87	8.7
9	1	0	0	1	0	0	0	0	9	86	8.6

*Internally strapped for logic 0 (ground).
**Externally strapped for logic 0 (ground) at pins 7, 16, and 17.

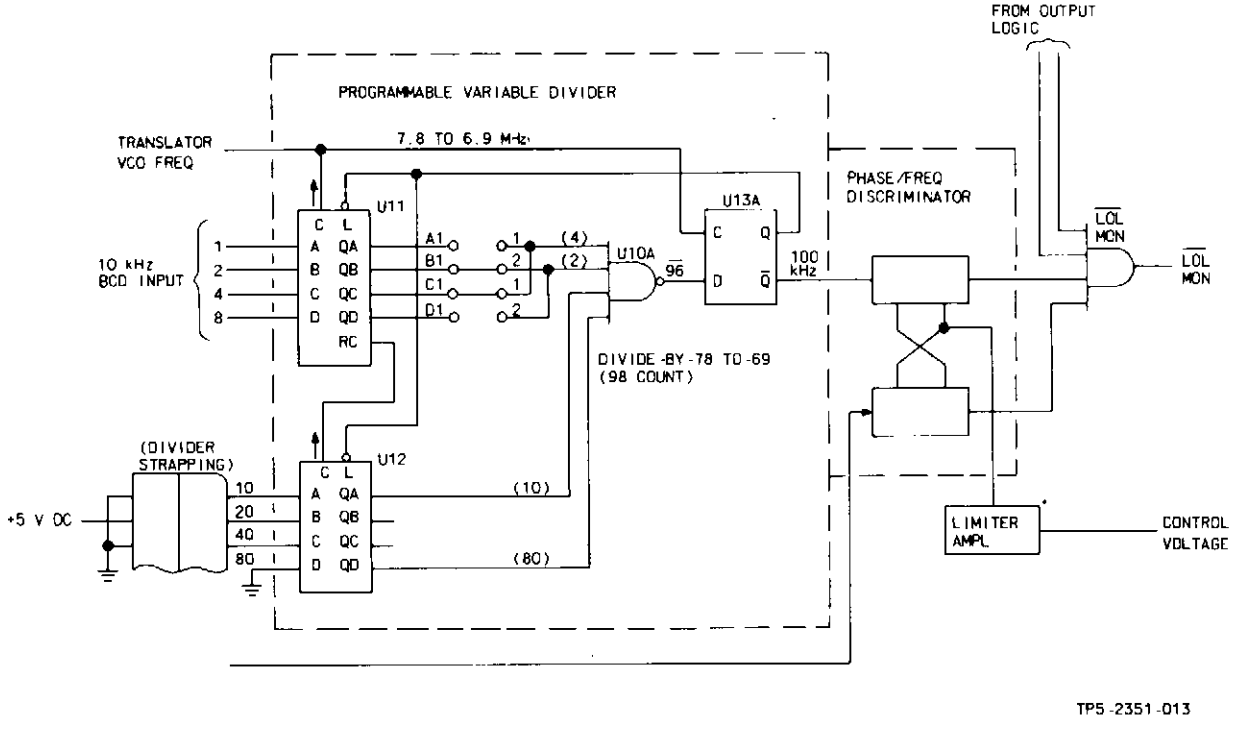


100-kHz Decade Translator, Logic Circuit
Figure 5

Table 4. 10-kHz Decade, Logic Truth Table.

BCD INPUT (10 kHz)	DIVIDER INPUTS								OUTPUT COUNT	DIVIDE-BY	LOOP FREQ (MHz)
	U11				U12						
	A	B	C	D	**A	[1]B	**C	*D			
0	0	0	0	0	0	1	0	0	20	78	7.8
1	1	0	0	0	0	1	0	0	21	77	7.7
2	0	1	0	0	0	1	0	0	22	76	7.6
3	1	1	0	0	0	1	0	0	23	75	7.5
4	0	0	1	0	0	1	0	0	24	74	7.4
5	1	0	1	0	0	1	0	0	25	73	7.3
6	0	1	1	0	0	1	0	0	26	72	7.2
7	1	1	1	0	0	1	0	0	27	71	7.1
8	0	0	0	1	0	1	0	0	28	70	7.0
9	1	0	0	1	0	1	0	0	29	69	6.9

*Internally strapped for logic 0 (ground).
**Externally strapped for logic 0 (ground) at pins 7 and 16.
[1]Externally strapped for logic 1 (+5.2 V dc) at pin 17.

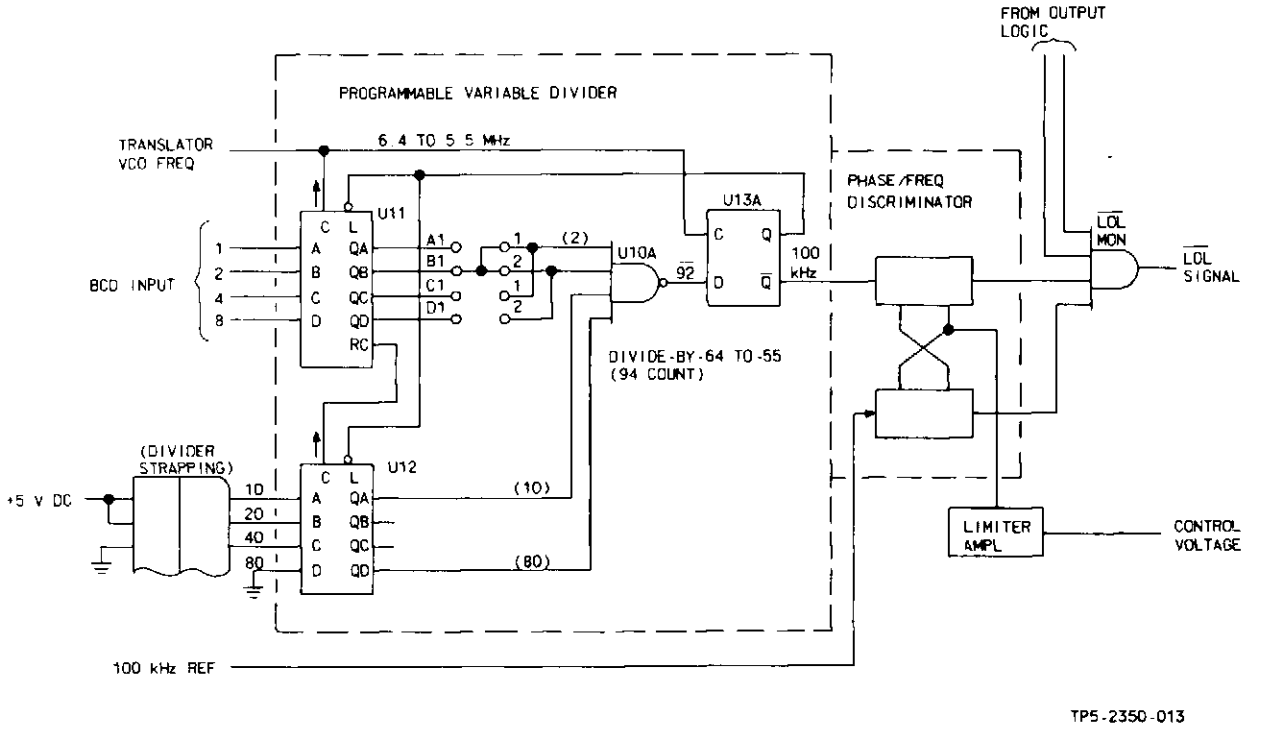


10-kHz Decade Translator, Logic Circuit
Figure 6

Table 5. 1-kHz Decade, Logic Truth Table.

BCD INPUT (1 kHz)	DIVIDER INPUTS								OUTPUT COUNT	DIVIDE-BY	LOOP FREQ (MHz)
	U11				U12						
	A	B	C	D	[1]A	[1]B	**C	*D			
0	0	0	0	0	1	1	0	0	30	64	6.4
1	1	0	0	0	1	1	0	0	31	63	6.3
2	0	1	0	0	1	1	0	0	32	62	6.2
3	1	1	0	0	1	1	0	0	33	61	6.1
4	0	0	1	0	1	1	0	0	34	60	6.0
5	1	0	1	0	1	1	0	0	35	59	5.9
6	0	1	1	0	1	1	0	0	36	58	5.8
7	1	1	1	0	1	1	0	0	37	57	5.7
8	0	0	0	1	1	1	0	0	38	56	5.6
9	1	0	0	1	1	1	0	0	39	55	5.5

*Internally strapped for logic 0 (ground).
**Externally strapped for logic 0 (ground) at pin 16.
[1]Externally strapped for logic 1 (+5.2 V dc) at pins 7 and 17.

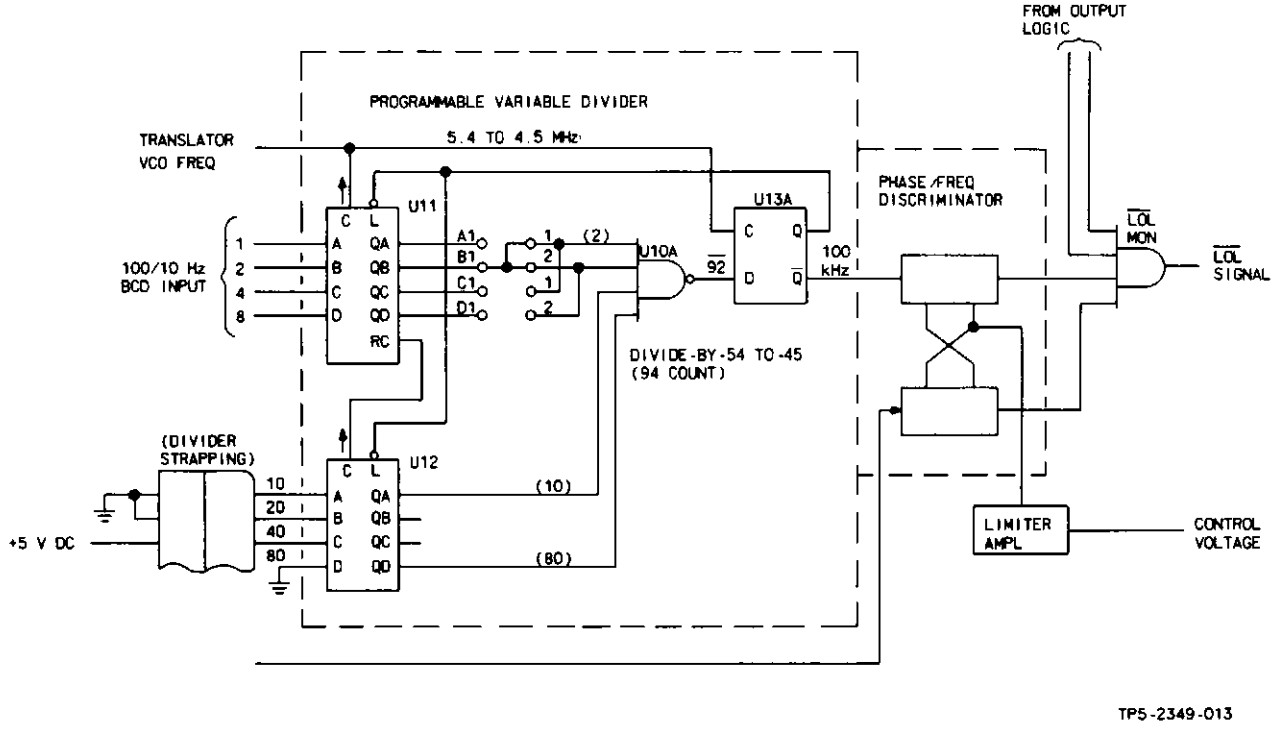


1-kHz Decade Translator, Logic Circuit
Figure 7

Table 6. 100/10-Hz Decade, Logic Truth Table.

BCD INPUT (100/10 Hz)	DIVIDER INPUTS								OUTPUT COUNT	DIVIDE-BY	LOOP FREQ (MHz)
	U11				U12						
	A	B	C	D	**A	**B	[1]C	*D			
0	0	0	0	0	0	0	1	0	40	54	5.4
1	1	0	0	0	0	0	1	0	41	53	5.3
2	0	1	0	0	0	0	1	0	42	52	5.2
3	1	1	0	0	0	0	1	0	43	51	5.1
4	0	0	1	0	0	0	1	0	44	50	5.0
5	1	0	1	0	0	0	1	0	45	49	4.9
6	0	1	1	0	0	0	1	0	46	48	4.8
7	1	1	1	0	0	0	1	0	47	47	4.7
8	0	0	0	1	0	0	1	0	48	46	4.6
9	1	0	0	1	0	0	1	0	49	45	4.5

*Internally strapped for logic 0 (ground).
**Externally strapped for logic 0 (ground) at pins 7 and 17.
[1]Externally strapped for logic 1 (+5.2 V dc) at pin 16.



100/10-Hz Decade Translator, Logic Circuit
Figure 8

2.3 Translator VCO Circuits

The translator vco circuits receive a control voltage from the translator logic circuits. The control voltage drives the vco to the required translator frequency. The translator signal output is supplied through one buffer amplifier to the output mixer circuits and the translator logic circuits.

2.4 Output Mixer Circuits

The output mixer circuits receive a translator signal input (table 2) from the translator vco. The translator vco signal is mixed with the output vco frequency (table 2) and a resulting difference frequency (table 2, same as high-reference input) is supplied to the output logic circuits.

2.5 Output Logic Circuits

The output logic circuits receive the output mixer difference frequency and a high-reference input signal (table 2), and supply a control voltage output signal to operate the output vco.

Refer to figure 9. The output mixer difference frequency is supplied through a squaring amplifier to a phase/frequency discriminator. This frequency is compared with the high-reference input signal. A phase or frequency difference in the discriminator causes the control voltage to increase or decrease to adjust the frequency of the vco. If there is no phase or frequency difference, the discriminator provides a logic 1 lock signal output and the vco frequency locks.

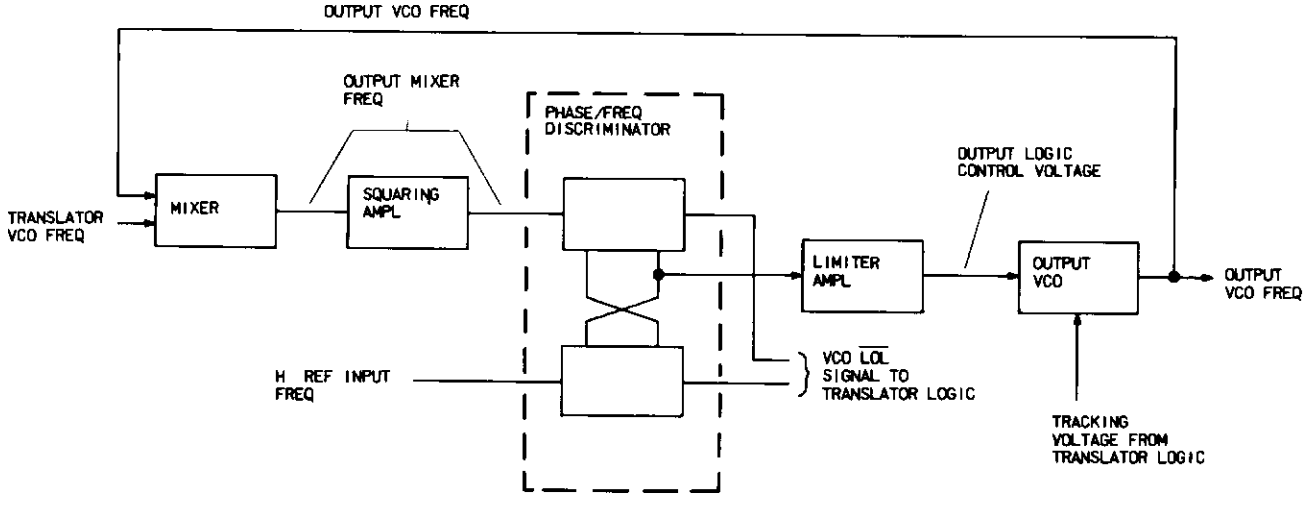
2.6 Output VCO Circuits

The output vco circuits receive a control voltage from the output logic circuits and a tracking voltage from the translator logic circuits. The tracking voltage from the translator logic circuits provides a reference for the output vco, and the control voltage from the output logic circuits drives the output vco to the required output vco frequency. The output vco frequency is supplied through a fixed divide-by-10 circuit and provides a reference frequency to the unit under control for additional frequency mixing and generation. Note that the tracking voltage from the translator logic circuits is used as a reference for the output vco, thus summing the translator frequency information and the output vco frequency information.

2.7 Up/Down Decade Counter 74LS190 (Refer to table 7.)

The 74LS190 up/down decade counter is a 4-bit decade counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when input conditions are met.

A high at the enable input inhibits counting. A LOC at the enable input and a low-to-high clock transition triggers the four master/slave flip-flops. The enable input should be changed only when the clock is high. The down/up input determines the direction of the count. When low, the count goes up; when high, the count goes down.



Output Logic Circuits
Figure 9

Table 7. Up/Down Decade Counter, Logic Truth Table.

PROGRAMMABLE INPUTS				COUNT	BCD OUTPUTS			
A	B	C	D		QA	QB	QC	QD
0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	0	0	0
0	1	0	0	2	0	1	0	0
1	1	0	0	3	1	1	0	0
0	0	1	0	4	0	0	1	0
1	0	1	0	5	1	0	1	0
0	1	1	0	6	0	1	1	0
1	1	1	0	7	1	1	1	0
0	0	0	1	8	0	0	0	1
1	0	0	1	9	1	0	0	1

E (enable): logic 0 enables counter; logic 1 inhibits counter.

L (load): logic 0 programs the bcd output count to be set at the bcd count of the programmable inputs; the next clock pulse counts one higher/lower (up/down).

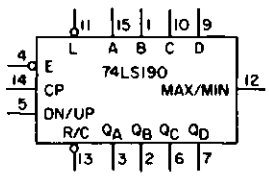
DU (down/up): logic 0 counts up; logic 1 counts down.

CP (clock pulse): logic 0-to-logic 1 transition advances counter.

RC (ripple clock): logic 0 pulse equal to 1/2 clock cycle when an overflow occurs.

MM (maximum/minimum count): logic 1 pulse equal to full clock cycle when an overflow or underflow occurs.

These counters are programmable. The outputs may be preset to any state by placing a low on the load input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the state of the clock input. This allows the counters to be used as modulo-N dividers by modifying the count length with the preset inputs.



V_{CC} = PIN 16

GND = PIN 8

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Up/Down Decade Counter 74LS190
Figure 10

Two outputs are available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters are cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

2.8 Decade Counter 74LS90 (Refer to table 8.)

The 74LS90 decade counter is a high-speed, monolithic decade counter consisting of four dual-rack, master-slave flip-flops internally interconnected to provide a divide-by-2 counter and a divide-by-5 counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logical 0 or to a binary coded decimal (bcd) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes.

a. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the bcd count sequence in table 8. In addition to a conventional 0 reset, inputs are provided to reset a bcd 9 count for nine's complement decimal applications.
b. If a symmetrical divide-by-10 count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of 10, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-10 square wave is obtained at output A.
c. For operation as a divide-by-2 counter and divide-by-5 counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-2 function. The BD input is used to obtain binary divide-by-5 operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

Table 8. Decade Counter 74LS90, Logic Truth Table.

*BCD COUNT SEQUENCE				
COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

**RESET/COUNT							
RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	Count			
0	X	0	X	Count			
0	X	X	0	Count			
X	0	0	X	Count			

*Output A connected to input BD for BCD count.
**X indicates that either a logical 1 or a logical 0 may be present.

2.9 *Dual D-Type Flip-Flop With Preset and Clear 74LS74 (Refer to table 9.)*

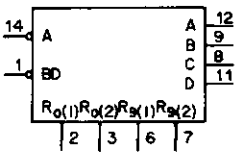
The 74LS74 consists of dual high-speed D-type flip-flops. Information on the D input is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either high or low level, the D-input signal has no effect.

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 *Test Equipment and Power Requirements*

Test equipment and power sources required to test, troubleshoot, and repair the synthesizer decade are listed in the maintenance section of this instruction book.

LOGIC SYMBOL

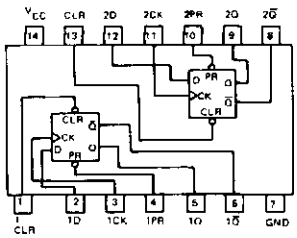


TP5-2326-012

Decade Counter 74LS90
Figure 11

3.2 *Testing*

The test procedures in table 10 check total performance of the synthesizer decade. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.



TP5-2327-011

Dual D-Type Flip-Flop With Preset and Clear 74LS74
Figure 12

Table 9. Dual D-Type Flip-Flop With Preset and Clear 74LS74, Logic Truth Table.

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	*H	*H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_O	$\overline{Q_O}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_O = the level of Q before the indicated input conditions were established.
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of the unit containing the synthesizer decade that is to be tested.		
	b. Remove cover from the synthesizer section of the unit.		
	c. Remove synthesizer decade and install it on an extender card and place it in the unit.		
	d. Set unit LINE SELECTOR switch to 115 V.		
	e. Connect unit to 115-V ac power source and set power on.		
	f. Measure dc voltage from P1-20 and P1-2 to P1-6 (ground).	+5.2 ±0.2 V dc.	Check unit synthesizer voltage regulator.
	g. Measure dc voltage from P1-10 to P1-6 (ground).	NLT +19.5 V dc, NMT +20.8 V dc.	Check unit synthesizer voltage regulator.
2. 100-kHz decade 623-2080-001	**Note** CR1, CR2, CR3, and CR4 are located under metal can shields. These shields must be in place during testing and adjustments. Refer to figure 13 for test point locations on the rear of the synthesizer decade.		
	a. Using a frequency counter, measure the high reference input between P1-14 and P1-4 (ground).	800 ±50 kHz. Note actual frequency.	Check unit 10-kHz decade.
	b. Set FREQUENCY KHZ control on front panel to 09900.00 (or 09900.0).		
	c. Measure the dc voltage at the cathode end of CR3-CR4. (Refer to note and chart at end of test 2 for voltages and output frequencies at different 100-kHz settings.)	10.0 ±0.1 V dc.	Adjust L9 for 10.0 ±0.1 V dc. If L9 adjustment does not correct the problem, check Q4, Q5, and associated circuit.
	d. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	940 ±5 kHz. (Actual should equal 935 kHz plus one-tenth of the difference between 850 kHz and the actual frequency in step a.)	Adjust L7 for actual frequency required with 1.5 V dc at anode end of CR1-CR2. If L7 adjustment does not correct the problem, check Q1, Q2, and associated circuits.
(Cont)			

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	e. Measure the dc voltage at the anode end of CR1-CR2.	1.5 ±0.5 V dc.	Same as step d.
	f. Note the dc voltage at the anode end of the anode end of CR1-CR2 while moving the 100-kHz frequency control from 9 down to 0.	NLT 1.0 V dc and NMT 2.0 V dc at any frequency control setting.	Adjust L7 so that all settings fall into the 1.0- to 2.0-V dc reading.
	g. Set FREQUENCY KHZ control on front panel to 09000.00 (or 09000.0).		
	h. Using a frequency counter, measure the high reference input between P1-14 and P1-4 (ground).	850 ±0.5 kHz.	Check unit 10-kHz decade.
	i. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	1035 ±0.5 kHz.	Check U11, U12, U13, and associated circuits.
	j. Set FREQUENCY KHZ control on front panel to 09900.00 (or 09900.0).		
	k. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	945 ±0.5 kHz.	Check U11, U12, U13, and associated circuits.
	l. Measure the dc voltage at P1-12 to ground.	NLT +3.5 V dc. **Note** RCV FAULT, EXCTR FAULT, or R/E FAULT indicator lighting indicates that result of step m is satisfactory.	Check U3, U8, U9, and U10.
	m. Ground P1-5 while noting the voltage at P1-12.	NMT 0.5 V dc.	Check U6, U7, U8, U9, and U10.
	n. Remove P1-5 ground.		
	o. Set front-panel PWR switch off.		
	p. Remove 10-kHz decade from unit under test.		
	q. Set front-panel PWR switch on.		
	r. Measure the dc voltage at P1-12 to ground.	NMT 0.5 V dc.	Check U1, U2,U3, and U10.
(Cont)	s. Set front-panel PWR switch off.		

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	t. Replace 10-kHz decade in unit under test.		

Note

The following chart is shown with an input frequency of 850 ±5 kHz. The actual output frequency with any input frequency can be determined using the following formula.

$$AF = LF - 10\text{ kHz} + \frac{850\text{ kHz} - IF}{10}$$

AF = actual output frequency at P1-1.

LF = output frequency listed in chart for associated 100-kHz frequency digit.

IF = actual input frequency.

100-kHz FREQ DIGIT	CR3-CR4 DC VOLTAGE	FREQ OUTPUT P1-1 (kHz)
9	10.00 ±0.1	945 ±0.5
8	*10.30	955 ±0.5
7	*10.55	965 ±0.5
6	*10.85	975 ±0.5
5	*11.15	985 ±0.5
4	*11.40	995 ±0.5
3	*11.70	1005 ±0.5
2	*11.95	1015 ±0.5
1	*12.25	1025 ±0.5
0	*12.50	1035 ±0.5

Note

Table shown with an input frequency of 850 ±5 kHz [front-panel FREQUENCY KHZ setting of 09X00.00 (or 09X00.0)].

*Reference voltage only. Voltages will vary from board to board.

3. 10-kHz decade 623-2080-002	**Note** CR1, CR2, CR3, and CR4 are located under metal can shields. These shields must be in place during testing and adjustments. Refer to figure 13 for test point locations on the rear of the synthesizer decade.		
	a. Using a frequency counter, measure the high reference input between P1-14 and P1-4 (ground).	650 ±50 kHz. Note actual frequency.	Check unit 1-kHz decade.
(Cont)	b. Set FREQUENCY KHZ control on front panel to 09990.00 (or 09990.0).		

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	c. Measure the dc voltage at the cathode end of CR3-CR4 (refer to note and chart at end of test 3 for voltages and output frequencies at different 10-kHz settings).	10.45 ±0.1 V dc.	Adjust L9 for 10.00 ±0.1 V dc. If L9 adjustment does not correct the problem, check Q4, Q5, and associated circuit.
	d. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	755 ±5 kHz. (Actual should equal 750 kHz plus one-tenth of the difference between 700 kHz and the actual frequency in step a.)	Adjust L7 for actual frequency required with 1.5 V dc at anode end of CR1-CR2. If L7 adjustment does not correct the problem, check Q1, Q2, and associated circuits.
	e. Measure the dc voltage at the anode end of CR1-CR2.	1.5 ±0.5 V dc.	Same as step d.
	f. Note the dc voltage of the anode end of CR1-CR2 while moving the 10-kHz frequency control from 9 down to 0.	NLT 1.0 V dc and NMT 2.0 V dc at any frequency control setting.	Adjust L7 so that all settings fall into the 1.0- to 2.0-V dc reading.
	g. Set FREQUENCY KHZ control on front panel to 09900.00 (or 09900.0).		
	h. Using a frequency counter, measure the high reference input between P1-14 and P1-4 (ground).	700 ±0.5 kHz.	Check unit 1-kHz decade.
	i. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	850 ±0.5 kHz.	Check U11, U12, U13, and associated circuits.
	j. Set FREQUENCY KHZ control on front panel to 09990.00 (or 09990.0).		
	k. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	760 ±0.5 kHz.	Check U11, U12, U13, and associated circuits.
	l. Measure the dc voltage at P1-12 to ground.	NLT +3.5 V dc. **Note** RCV FAULT, EXCTR FAULT, or R/E FAULT indicator lighting indicates that result of step m is satisfactory.	Check U3, U8, U9, and U10.
(Cont)	m. Ground P1-5 while noting the voltage at P1-12.	NMT 0.5 V dc.	Check U6, U7, U8, U9, and U10.

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	n. Remove P1-5 ground.		
	o. Set front-panel PWR switch off.		
	p. Remove 1-kHz decade from unit under test.		
	q. Set front-panel PWR switch on.		
	r. Measure the dc voltage at P1-12 to ground.	NMT 0.5 V dc.	Check U1, U2, U3, and U10.
	s. Set front-panel PWR switch off.		
	t. Replace 1-KHZ decade in unit under test.		

Note

The following chart is shown with an input frequency of 700 ±5 kHz. The actual output frequency with any input frequency can be determined using the following formula.

$$AF = LF - 10\text{ kHz} + \frac{700\text{ kHz} - IF}{10}.$$

AF = actual output frequency at P1-1.

LF = output frequency listed in chart for associated 10-kHz frequency digit.

IF = actual input frequency.

10-kHz FREQ DIGIT	CR3-CR4 DC VOLTAGE	FREQ OUTPUT P1-1 (kHz)
9	10.00 ±0.1	760 ±0.5
8	*10.30	770 ±0.5
7	*10.55	780 ±0.5
6	*10.85	790 ±0.5
5	*11.10	800 ±0.5
4	*11.40	810 ±0.5
3	*11.75	820 ±0.5
2	*12.00	830 ±0.5
1	*12.35	840 ±0.5
0	*12.65	850 ±0.5

Note

Table shown with an input frequency of 700 ±5 kHz [front-panel FREQUENCY KHZ setting of 099X0.00 (or 099X0.0)].

*Reference voltage only. Voltages will vary from board to board.

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. 1-kHz decade 623-2080-003	**Note** CR1, CR2, CR3, and CR4 are located under metal can shields. These shields must be in place during testing and adjustments. Refer to figure 13 for test point locations on the rear of the synthesizer decade.		
	a. Using a frequency counter, measure the high reference input between P1-14 and P1-4 (ground).	550 ±50 kHz. Note actual frequency.	Check unit 100-kHz decade.
	b. Set FREQUENCY KHZ control on front panel to 09999.00 (or 09999.0).		
	c. Measure the dc voltage at the cathode end of CR3-CR4 (refer to note and chart at end of test 4 for voltages and output frequencies at different 1-kHz settings).	10.0 ±0.1 V dc.	Adjust L9 for 10.0 ±0.1 V dc. If L9 adjustment does not correct the problem, check Q4, Q5, and associated circuit.
	d. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	605 ±5 kHz. (Actual should equal 600 kHz plus one-tenth of the difference between 610 kHz and the actual frequency in step a.)	Adjust L7 for actual frequency required with 1.5 V dc at anode end of CR1-CR2. If L7 adjustment does not correct the problem, check Q1, Q2, and associated circuits.
	e. Measure the dc voltage at the anode end of CR1-CR2.	1.5 ±0.5 V dc.	Same as step d.
	f. Note the dc voltage at the anode end of CR1-CR2 while moving the 1-kHz frequency control from 9 down to 0.	NLT 1.0 V dc and NMT 2.0 V dc at any frequency control setting.	Adjust L7 so that all settings fall into the 1.0- to 2.0-V reading.
	g. Set FREQUENCY KHZ control on front panel to 09990.00 (or 09990.0).		
	h. Using a frequency counter, measure the high reference input between P1-14 and P1-4 (ground).	600 ±0.5 kHz.	Check unit 100-kHz decade.
	i. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	700 ±0.5 kHz.	Check U11, U12, U13, and associated circuits.
(Cont)	j. Set FREQUENCY KHZ control on front panel to 09999.00 (or 09999.0).		

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	k. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	610 ±0.5 kHz.	Check U11, U12, U13, and associated circuits.
	l. Measure the dc voltage at P1-12 to ground.	NLT +3.5 V dc. **Note** RCV FAULT, EXCTR FAULT, or R/E FAULT indicator lighting indicates that result of step m is satisfactory.	Check U3, U8, U9, and U10.
	m. Ground P1-5 while noting the voltage at P1-12.	NMT 0.5 V dc.	Check U6, U7, U8, U9, and U10.
	n. Remove P1-5 ground.		
	o. Set front-panel PWR switch off.		
	p. Remove decade in 100-Hz slot (A18) from unit under test.		
	q. Set front-panel PWR switch on.		
	r. Measure the dc voltage at P1-12 to ground.	NMT 0.5 V dc.	Check U1, U2, U3, and U10.
	s. Set front-panel PWR switch off.		
	t. Replace decade in 100-Hz slot (A18) in unit under test.		
	Note The following chart is shown with an input frequency of 600 ±5 kHz. The actual output frequency with any input frequency can be determined using the following formula. $AF = LF - 10\text{ kHz} + \frac{600\text{ kHz} - IF}{10}$. AF = actual output frequency at P1-1. LF = output frequency listed in chart for associated 1-kHz frequency digit. IF = actual input frequency.		
(Cont)			

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)			
5. 100/10-Hz decade 623-2080-004	**Note** CR1, CR2, CR3, and CR4 are located under metal can shields. These shields must be in place during testing and adjustments. Refer to figure 13 for test-point locations on the rear of the synthesizer decade.		
	a. Using a frequency counter, measure the high reference input between P1-14 and P1-4 (ground).	550 ±50 kHz. Note actual frequency.	Check unit 10-Hz decade or end decade.
	b. If decade installed in 100-Hz slot (A18), set FREQUENCY KHZ control to 09999.90 (or 09999.9). If decade installed in 10-Hz slot (A17), set FREQUENCY KHZ control to 09999.99.		
	c. Measure the dc voltage at the cathode end of CR3-CR4 (refer to note and chart at end of test 5 for voltages and output frequencies at different 100- or 10-Hz settings).	9.5 ±0.1 V dc.	Adjust L9 for 9.5 ±0.1 V dc. If L9 adjustment does not correct the problem, check Q4, Q5, and associated circuit.
(Cont)			

1-kHz FREQ DIGIT	CR3-CR4 DC VOLTAGE	FREQ OUTPUT P1-1 (kHz)
9	10.00 ±0.1	610 ±0.5
8	*10.40	620 ±0.5
7	*10.85	630 ±0.5
6	*11.25	640 ±0.5
5	*11.70	650 ±0.5
4	*12.10	660 ±0.5
3	*12.55	670 ±0.5
2	*12.95	680 ±0.5
1	*13.40	690 ±0.5
0	*13.80	700 ±0.5

Note

Table shown with an input frequency of 600 ±5 kHz [front-panel FREQUENCY KHZ setting of 0999X.00 (or 0999X.0)].

*Reference voltage only. Voltages will vary from board to board.

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	d. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	515 ±5 kHz. (Actual should equal 510 kHz plus one-tenth of the difference between 600 kHz and the actual frequency in step a.)	Adjust L7 for actual frequency required with 1.5 V dc at anode end of CR1-CR2. If L7 adjustment does not correct the problem, check Q1, Q2, and associated circuits.
	e. Measure the dc voltage at the anode end of CR1-CR2.	1.5 ±0.5 V dc.	Same as step d.
	f. Note the dc voltage at the anode end of CR1-CR2 while moving the 100- or 10-Hz frequency control from 9 down to 0 (Change 100-Hz control if installed as 100-Hz decade or 10-Hz control if installed as 10-Hz decade).	NLT 1.0 V dc and NMT 2.0 V dc at any frequency control setting.	Adjust L7 so that all settings fall into the 1.0- to 2.0-V dc reading.
	g. If decade installed in 100-Hz slot (A18), set FREQUENCY KHZ control on front panel to 09999.00 (or 09999.0). If decade installed in 10-Hz slot, set FREQUENCY KHZ control on front panel to 09999.90.		
	h. Using a frequency counter, measure the high reference input between P1-14 and P1-4 (ground).	600 ±0.5 kHz.	Check unit 10-Hz decade or end decade.
	i. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	600 ±0.5 kHz.	Check U11, U12, U13, and associated circuits.
	j. If decade installed in 100-Hz slot (A18), set FREQUENCY KHZ control on front panel to 09999.90 (or 09999.9). If decade installed in 10-Hz slot (A18), set FREQUENCY KHZ control on front panel to 09999.99.		
	k. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	510 ±0.5 kHz.	Check U11, U12, U13, and associated circuits.
	l. Measure the dc voltage at P1-12 to ground.	NLT +3.5 V dc. **Note** RCV FAULT, EXCTR FAULT, or R/E FAULT indicator lighting indicates that result of step m is satisfactory.	Check U3, U8, U9, and U10.
(Cont)	m. Ground P1-5 while noting the voltage at P1-12.	NMT 0.5 V dc.	Check U6, U7, U8, U9, and U10.

Table 10. Synthesizer Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	n. Remove P1-5 ground.		
	o. Set front-panel PWR switch off.		
	p. If testing decade installed in 100-Hz slot (A18), remove decade in 10-Hz (A17) slot from unit under test. If testing decade installed in 10-Hz slot (A17), remove end decade from unit under test.		
	q. Set front-panel PWR switch on.		
	r. Measure the dc voltage at P1-12 to ground.	NMT 0.5 V dc.	Check U1, U2, U3, and U10.
	s. Set front-panel PWR switch off.		
	t. Replace decade that was removed in step p.		

The following chart is shown with an input frequency of 600 ±5 kHz. The actual output frequency with any input frequency can be determined using the following formula.

$$AF = LF - 10\ kHz + \frac{600\ kHz - IF}{10}.$$

AF = actual output frequency at P1-1.

LF = output frequency listed in chart for associated 100- or 10-Hz frequency digit.

IF = actual input frequency.

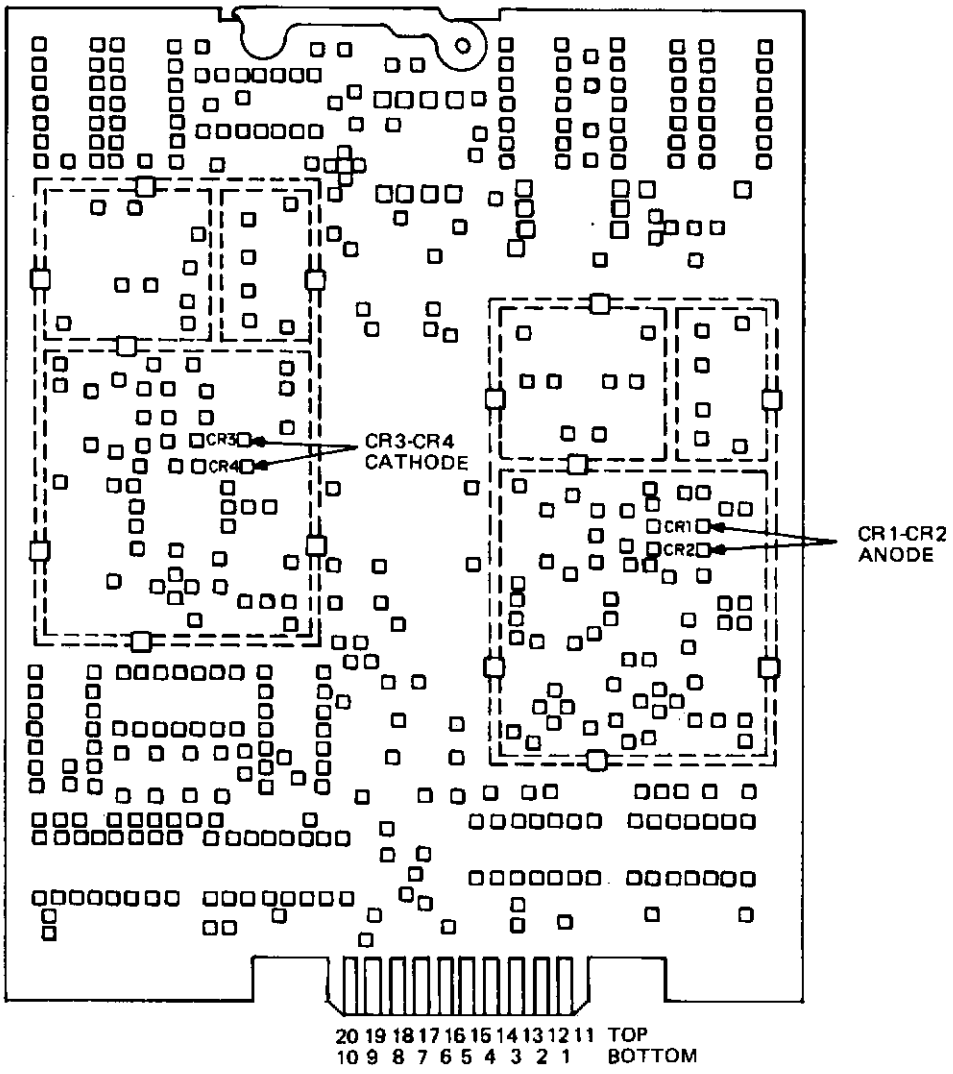
*100/10-Hz FREQ DIGIT	CR3-CR4 DC VOLTAGE	FREQ OUTPUT P1-1 (kHz)
9	10.0 ±0.1	510 ±0.5
8	**10.5	520 ±0.5
7	**11.0	530 ±0.5
6	**11.5	540 ±0.5
5	**12.0	550 ±0.5
4	**12.5	560 ±0.5
3	**13.0	570 ±0.5
2	**13.5	580 ±0.5
1	**14.0	590 ±0.5
0	**14.5	600 ±0.5

*If decade installed in 100-Hz (A18) slot, 100-Hz frequency digit position. If decade installed in 10-Hz (A17) slot, 10-Hz frequency digit position.

**Reference voltage only. Voltages will vary from board to board.

Note

Table shown with an input frequency of 600 ±5 kHz.



TP5-3056-011

Synthesizer Decade, Rear View
Figure 13

4. ALIGNMENT/ADJUSTMENT

4.1 L7 and L9 Selection, and Decade Strapping

Note

L7 and L9 can be replaced only by removing the metal cans that cover them. In emergency repairs L7, L9, and strapping can be changed on any synthesizer decade 623-2080-( ) to make the required decade (100 kHz, 10 kHz, 1 kHz, or 100/10 Hz). When L7, L9, and straps are installed as follows, the indicated decade is constructed. Testing and adjustments must be made to ensure proper operation.

4.1.1 100-kHz Decade 623-2080-001

a. Install L7, 6.75 to 11.25 μH, (242-0441-030).
b. Install L9, 6.75 to 11.25 μH, (242-0441-030).
c. Strap A to 1 and B to 2.

4.1.2 10-kHz Decade 623-2080-002

a. Install L7, 6.75 to 11.25 μH, (242-0441-030).
b. Install L9, 12.0 to 18.0 μH, (242-0441-040).
c. Strap B to 2 and C to 1.

4.1.3 1-kHz Decade 623-2080-003

a. Install L7, 12.0 to 18.0 μH, (242-0441-040).
b. Install L9, 20.8 to 31.2 μH, (242-0441-050).
c. Strap B to 2 and 1 to 2.

4.1.4 100/10-Hz Decade 623-2080-004

a. Install L7, 20.8 to 31.2 μH, (242-0441-050).
b. Install L9, 20.8 to 31.2 μH, (242-0441-050).
c. Strap B to 2 and 1 to 2.

4.2 Adjustment of L7 and L9

Note

If either L7 or L9 is replaced, both must be adjusted. Metal can shields must be installed before making these adjustments.

Refer to table 8. Perform the test procedures applicable to the associated decade.

a. For L7 and L9 adjustment in 100-kHz decade, perform test 2, steps a through d.
b. For L7 and L9 adjustment in 10-kHz decade, perform test 3, steps a through d.
c. For L7 and L9 adjustment in 1-kHz decade, perform test 4, steps a through d.
d. For L7 and L9 adjustment in 100/10-Hz decade, perform test 5, steps a through d.

5. REPAIR

Repair of the synthesizer decade is accomplished using the standard planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

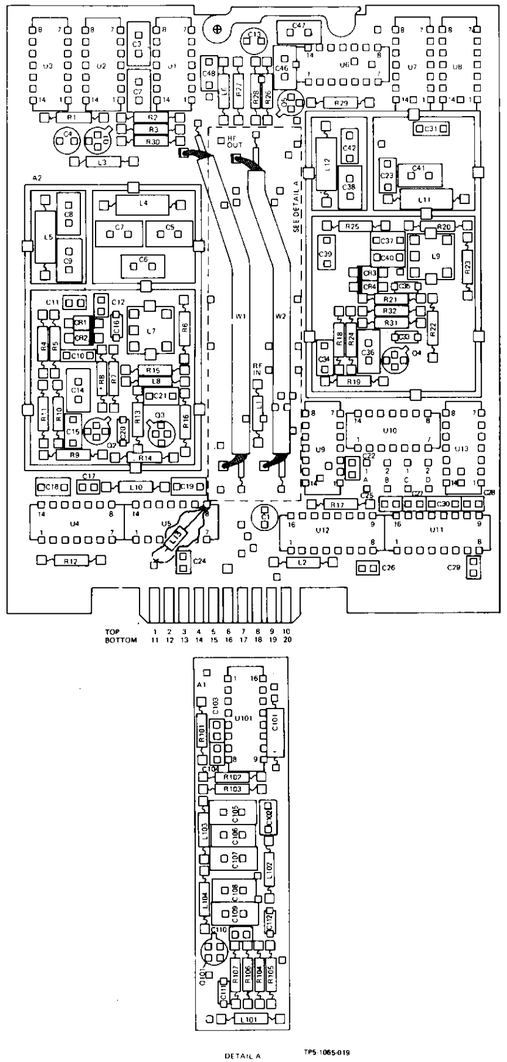
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figure 14). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

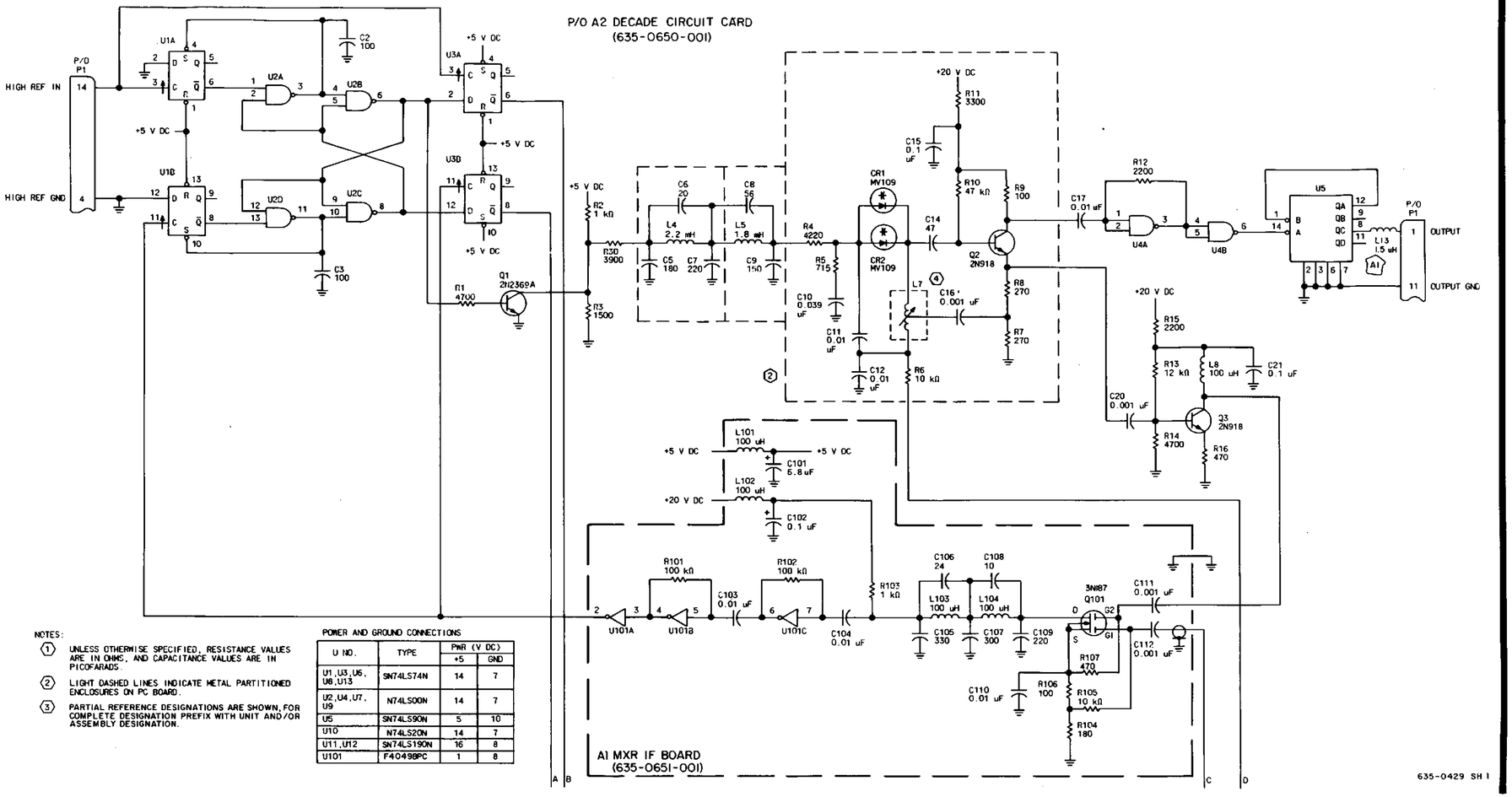
Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
100-kHz synthesizer decade	623-2080-001	REV E
10-kHz synthesizer decade	623-2080-002	REV E
1-kHz synthesizer decade	623-2080-003	REV E
100/10-Hz synthesizer decade	623-2080-004	REV E
Decade circuit card	635-0650-001	REV K
Mixer if board	635-0651-001	REV A





NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, AND CAPACITANCE VALUES ARE IN PICOFARADS.
2. LIGHT DASHED LINES INDICATE METAL PARTITIONED ENCLOSURES ON PC BOARD.
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.

POWER AND GROUND CONNECTIONS

U NO.	TYPE	PWR (V DC)	
		+5	GND
U1,U3,U6, U8,U13	SN74LS74N	14	7
U2,U4,U7, U9	N74LS00N	14	7
U5	SN74LS90N	5	10
U10	N74LS20N	14	7
U11,U12	SN74LS190N	16	8
U101	F4049BPC	1	8

Synthesizer Decade, Schematic Diagram
Figure 14 (Sheet 1 of 3)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	SYNTH 100-kHz DECADE 623-2080-001		A
	SYNTH 10-kHZ DECADE 623-2080-002		B
	SYNTH 1-kHZ DECADE 623-2080-003		C
	SYNTH 100/10-Hz DECADE 623-2080-004		D
A1	MIXER/IF BOARD	635-0651-001	
A2	DECADE BOARD	635-0650-001	
L1-L6	NOT USED		
L7	COIL, RF, VAR, 6.75-11.25μH	242-0441-030	A,B
L7	COIL, RF, VAR, 12-18μH	242-0441-040	C
L7	COIL, RF, VAR, 20.8-31.2μH	242-0441-050	D
L8	NOT USED		
L9	COIL, RF, VAR, 6.75-11.25μH	242-0441-030	A
L9	COIL, RF, VAR, 12-18μH	242-0441-040	B
L9	COIL, RF, VAR, 20.8-31.2μH	242-0441-050	C,D
	MIXER/IF BOARD A1 635-0651-001		
C101	CAPACITOR, FXD, ELCTLT, 6.8μF, 10%, 6V	184-9086-020	
C102	CAPACITOR, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C103,C104	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C105	CAPACITOR, FXD, MICA DIEL, 330pF, 5%, 100V	912-3915-000	
C106	CAPACITOR, FXD, MICA DIEL, 24pF, 5%, 500V	912-3843-000	
C107	CAPACITOR, FXD, MICA DIEL, 300pF, 5%, 300V	912-3912-000	
C108	CAPACITOR, FXD, MICA DIEL, 10pF, 0.5pF, 500V	912-3837-000	
C109	CAPACITOR, FXD, MICA DIEL, 220pF, 5%, 500V	912-3903-000	
C110	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C111,C112	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
L101-L104	COIL, RF, 100μH	240-2047-000	
Q101	TRANSISTOR, 3N187	352-0093-010	
R101,R102	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R103	RESISTOR, FXD, CMPSN, 1KΩ, 10%, 1/4W	745-0749-000	
R104	RESISTOR, FXD, CMPSN, 180Ω, 10%, 1/4W	745-0722-000	
R105	RESISTOR, FXD, CMPSN, 10KΩ, 10%, 1/4W	745-0785-000	
R106	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R107	RESISTOR, FXD, CMPSN, 470Ω, 10%, 1/4W	745-0737-000	
U101	INTEGRATED CKT, F4049BPC	351-8159-210	
	DECADE BOARD A2 635-0650-001		
CR1-CR4	SEMICOND DEVICE, MV109	922-6124-040	
C1	CAPACITOR, FXD, ELCTLT, 68μF, 20%, 6V	184-9102-040	
C2, C3	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 500V	912-3879-000	
C4	CAPACITOR, FXD, ELCTLT, 68μF, 20%, 6V	184-9102-040	
C5	CAPACITOR, FXD, MICA DIEL, 180pF, 5%, 500V	912-3897-000	
C6	CAPACITOR, FXD, MICA DIEL, 20pF, 5%, 500V	912-3841-000	
C7	CAPACITOR, FXD, MICA DIEL, 220pF, 5%, 500V	912-3903-000	
C8	CAPACITOR, FXD, MICA DIEL, 56pF, 5%, 500V	912-3861-000	
C9	CAPACITOR, FXD, MICA DIEL, 150pF, 5%, 500V	912-3891-000	
C10	CAPACITOR, FXD, CER DIEL, 0.039μF, 10%, 100V	913-5019-390	
C11,C12	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C13	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-240	
C14	CAPACITOR, FXD, MICA DIEL, 47pF, 5%, 500V	912-3856-000	
C15	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C16	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C17	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C18,C19	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C20	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C21	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C22	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C23	CAPACITOR, FXD, CER DIEL, 0.0027μF, 5%, 100V	913-3117-130	
C24-C29	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C30,C31	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C32	NOT USED		
C33	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C34	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C35	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C36	CAPACITOR, FXD, MICA DIEL, 47pF, 5%, 500V	912-3856-000	
C37	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C38	CAPACITOR, FXD, MICA DIEL, 43pF, 5%, 500V	912-3854-000	
C39	CAPACITOR, FXD, CER DIEL, 3300pF, 10%, 100V	913-3281-170	

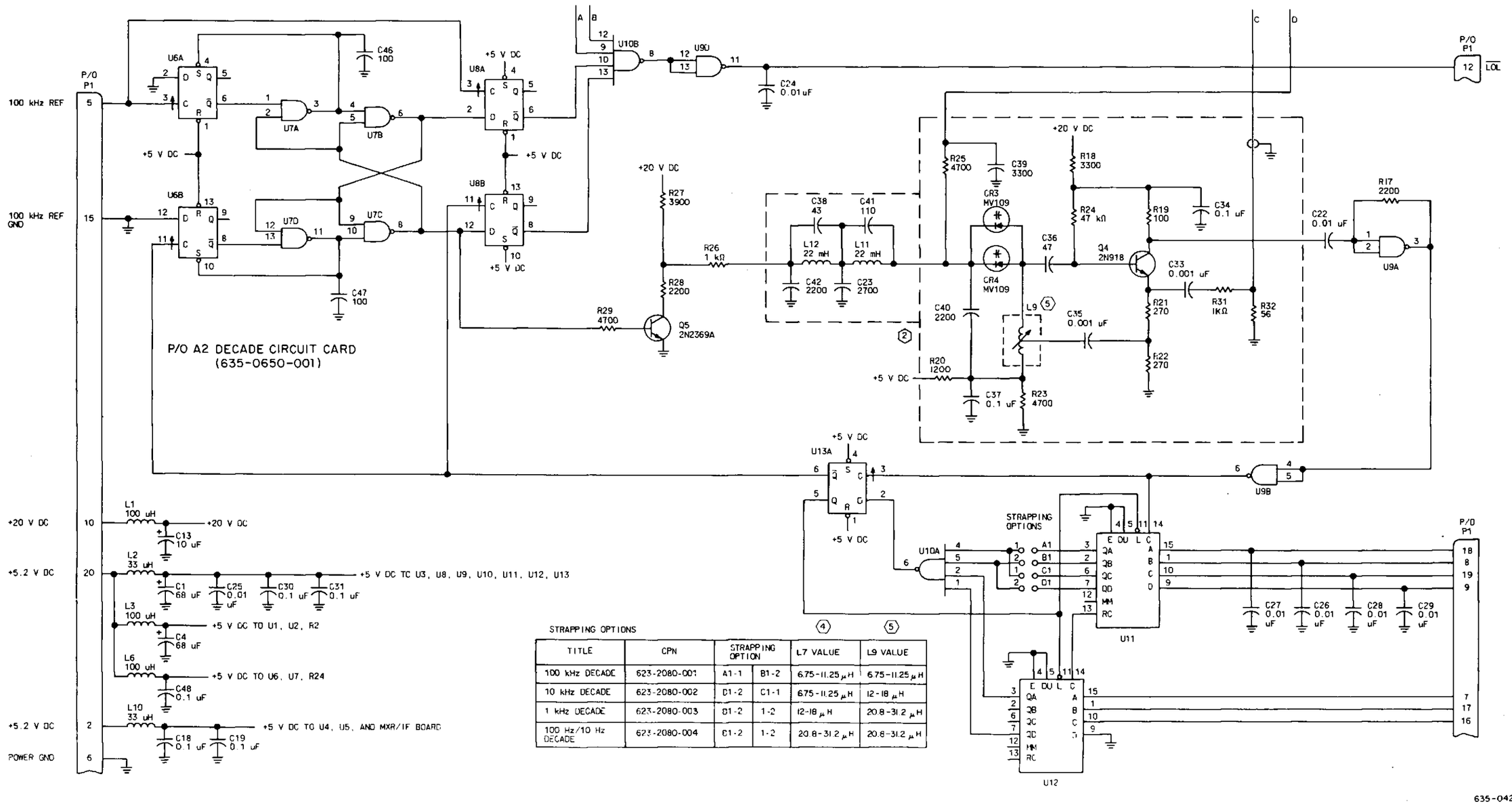
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART	USABLE ON CODE
C40	CAPACITOR, FXD, CER DIEL, 2200pF, 10%, 100V	913-3281-160	
C41	CAPACITOR, FXD, MICA DIEL, 110pF, 5%, 500V	912-3882-000	
C42	CAPACITOR, FXD, CER DIEL, 2200pF, 10%, 100V	913-3281-160	
C43-C45	NOT USED		
C46,C47	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 500V	912-3879-000	
C48	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
L1	COIL, RF, 100μH	240-2047-000	
L2	COIL, RF, 33μH	240-2041-000	
L3	COIL, RF, 100μH	240-2047-000	
L4	COIL, RF, 2200μH	240-2715-530	
L5	COIL, RF, 1800μH	240-2715-520	
L6	COIL, RF, 100μH	240-2047-000	
L7	NOT USED		
L8	COIL, RF, 100μH	240-2047-000	
L9	NOT USED		
L10	COIL, RF, 33μH	240-2041-000	
L11,L12	COIL, RF, 22,000μH	240-2715-650	
L13	COIL, RF, 1.5μH (A1)	240-2025-000	
Q1	TRANSISTOR, 2N2369A	352-0596-030	
Q2-Q4	TRANSISTOR, 2N918	352-0440-000	
Q5	TRANSISTOR, 2N2369A	352-0596-030	
R1	RESISTOR, FXD, CMPSN, 4.7KΩ, 10%, 1/4W	745-0773-000	
R2	RESISTOR, FXD, CMPSN, 1KΩ, 10%, 1/4W	745-0749-000	
R3	RESISTOR, FXD, CMPSN, 1.5KΩ, 10%, 1/4W	745-0755-000	
R4	RESISTOR, FXD, FILM, 4.22KΩ, 1%, 1/8W	705-1026-000	
R5	RESISTOR, FXD, FILM, 715Ω, 1%, 1/8W	705-0989-000	
R6	RESISTOR, FXD, CMPSN, 10KΩ, 10%, 1/4W	745-0785-000	
R7,R8	RESISTOR, FXD, CMPSN, 270Ω, 10%, 1/4W	745-0728-000	
R9	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R10	RESISTOR, FXD, CMPSN, 47KΩ, 10%, 1/4W	745-0809-000	
R11	RESISTOR, FXD, CMPSN, 3.3KΩ, 10%, 1/4W	745-0767-000	
R12	RESISTOR, FXD, CMPSN, 2.2KΩ, 10%, 1/4W	745-0761-000	
R13	RESISTOR, FXD, CMPSN, 12KΩ, 10%, 1/4W	745-0788-000	
R14	RESISTOR, FXD, CMPSN, 4.7KΩ, 10%, 1/4W	745-0773-000	
R15	RESISTOR, FXD, CMPSN, 2.2KΩ, 10%, 1/4W	745-0761-000	
R16	RESISTOR, FXD, CMPSN, 470Ω, 10%, 1/4W	745-0737-000	
R17	RESISTOR, FXD, CMPSN, 2.2KΩ, 10%, 1/4W	745-0761-000	
R18	RESISTOR, FXD, CMPSN, 3.3KΩ, 10%, 1/4W	745-0767-000	
R19	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R20	RESISTOR, FXD, CMPSN, 1.2KΩ, 10%, 1/4W	745-0752-000	
R21,R22	RESISTOR, FXD, CMPSN, 270Ω, 10%, 1/4W	745-0728-000	
R23	RESISTOR, FXD, CMPSN, 4.7KΩ, 10%, 1/4W	745-0773-000	
R24	RESISTOR, FXD, CMPSN, 47KΩ, 10%, 1/4W	745-0809-000	
R25	RESISTOR, FXD, CMPSN, 4.7KΩ, 10%, 1/4W	745-0773-000	
R26	RESISTOR, FXD, CMPSN, 1KΩ, 10%, 1/4W	745-0749-000	
R27	RESISTOR, FXD, CMPSN, 3.9KΩ, 10%, 1/4W	745-0770-000	
R28	RESISTOR, FXD, CMPSN, 2.2KΩ, 10%, 1/4W	745-0761-000	
R29	RESISTOR, FXD, CMPSN, 4.7KΩ, 10%, 1/4W	745-0773-000	
R30	RESISTOR, FXD, CMPSN, 3.9KΩ, 10%, 1/4W	745-0770-000	
R31	RESISTOR, FXD, CMPSN, 1KΩ, 10%, 1/4W	745-0749-000	
R32	RESISTOR, FXD, CMPSN, 56Ω, 10%, 1/4W	745-0704-000	
U1	INTEGRATED CKT, SN74LS74N	351-1525-040	
U2	INTEGRATED CKT, N74LS00N	351-1523-110	
U3	INTEGRATED CKT, SN74LS74N	351-1525-040	
U4	INTEGRATED CKT, N74LS00N	351-1523-110	
U5	INTEGRATED CKT, SN74LS90N	351-1636-010	
U6	INTEGRATED CKT, SN74LS74N	351-1525-040	
U7	INTEGRATED CKT, N74LS00N	351-1523-110	
U8	INTEGRATED CKT, SN74LS74N	351-1525-040	
U9	INTEGRATED CKT, N74LS00N	351-1523-110	
U10	INTEGRATED CKT, N74LS20N	351-1523-130	
U11,U12	INTEGRATED CKT, SN74LS190N	351-1527-040	
U13	INTEGRATED CKT, SN74LS74N	351-1525-040	

MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Added A2L13, 1.5μH	635-0650-001 REV K and above

Synthesizer Decade, Schematic Diagram
Figure 14 (Sheet 2)



STRAPPING OPTIONS

TITLE	CPN	STRAPPING OPTION		L7 VALUE	L9 VALUE
100 kHz DECADE	623-2080-001	A1-1	B1-2	6.75-11.25 μH	6.75-11.25 μH
10 kHz DECADE	623-2080-002	D1-2	C1-1	6.75-11.25 μH	12-18 μH
1 kHz DECADE	623-2080-003	B1-2	1-2	12-18 μH	20.8-31.2 μH
100 Hz/10 Hz DECADE	623-2080-004	C1-2	1-2	20.8-31.2 μH	20.8-31.2 μH

Synthesizer Decade, Schematic Diagram
Figure 14 (Sheet 3)

Synthesizer Output (635-4930-001)

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

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2nd Revision, 1 January 1979

1. DESCRIPTION

Synthesizer Output 635-4930-001, shown in figure 1, is a module that contains a base 2-layer planar card, four rf secure compartments (metal box construction), and five printed wiring boards. The base 2-layer planar card contains a 20-pin edge-on connector (2 layers, 10 pins each).

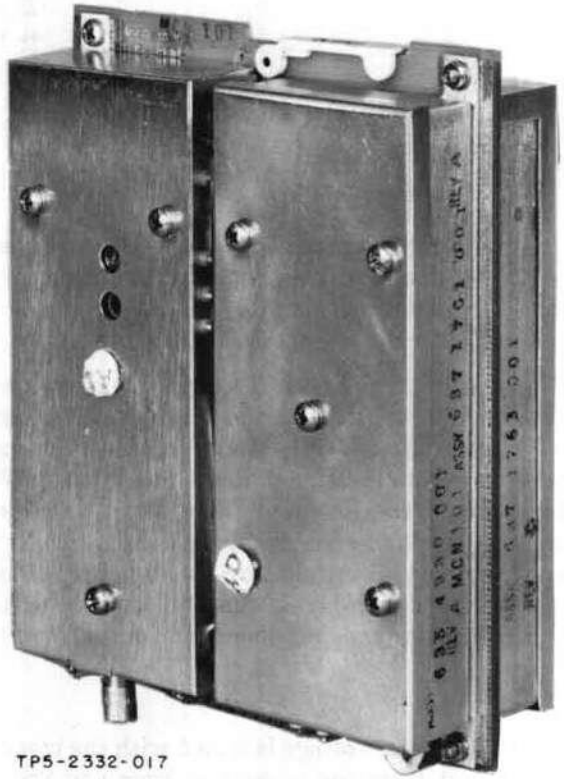
The synthesizer output module consists of translator logic, translator vco, output mixer, output logic, output vco, low-pass filter circuits, and a loss-of-lock (lol) monitor circuit.

2. PRINCIPLES OF OPERATION

2.1 General (Refer to figure 2.)

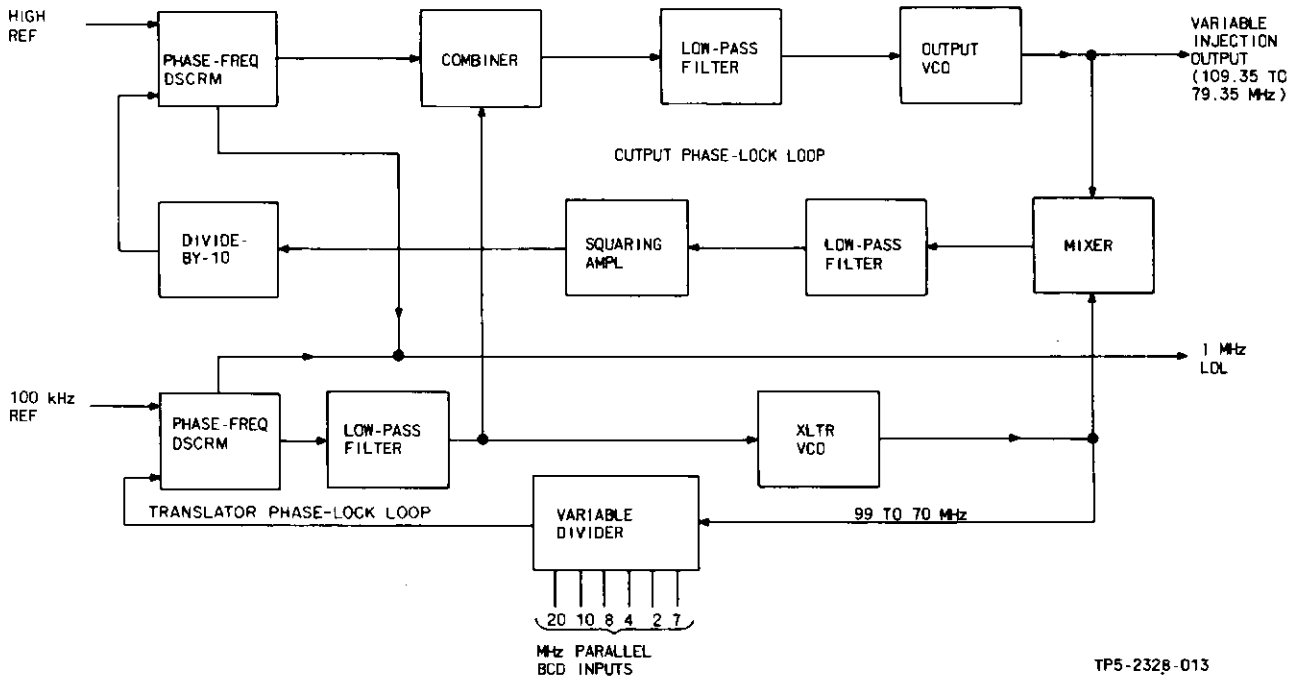
The synthesizer output module receives MHz bcd frequency control signals, a 100-kHz reference signal and a high-reference signal (1.035 to 0.935001 MHz), and generates a 109.35- to 79.35001-MHz variable injection signal output and a 1-MHz lock signal output (logic 1 for lock).

The translator logic circuits receive a 100-kHz reference input, a translator vco signal, and a bcd frequency input. The bcd frequency input is used to program a variable frequency divider (divide-by-99 to 70). The programmed variable frequency divider output (100 kHz) and the 100-kHz reference input are supplied to a phase/frequency discriminator that, with a low-pass filter, provides a control voltage proportional to the phase/frequency difference between its inputs. This control voltage is also supplied as a tracking voltage to the output phase-lock loop.



Synthesizer Output
Figure 1

The translator vco circuit receives the control voltage signal from translator logic circuits and is driven to and phase-locked at the variable frequency as programmed by variable divider bcd inputs to translator logic circuits. The translator vco output (99 to 70 MHz) is supplied to translator logic circuits for



Synthesizer Output, Block Diagram
Figure 2

clocking and lock signal generation. The translator vco output (99 to 70 MHz) is supplied to output mixer circuits for frequency mixing.

The output mixer circuit receives the translator signal input (99 to 70 MHz) and the output vco signal input (109.35 to 79.3501 MHz), mixes them and supplies a reference signal input (10.35 to 9.35001 MHz) through the low-pass filter and divide-by-10 counter to the phase/frequency discriminator. In the phase/frequency discriminator, the divide-by-10 output (1.035 to 0.935 MHz) is compared with the high reference input and produces an output control voltage.

The output control voltage is mixed with the tracking voltage input from the translator logic and vco circuits and applied to the output vco circuit. The output vco circuit receives the output control voltage signal from the output logic circuits and is driven to and locked at the variable injection frequency (109.35 to 79.3501 MHz).

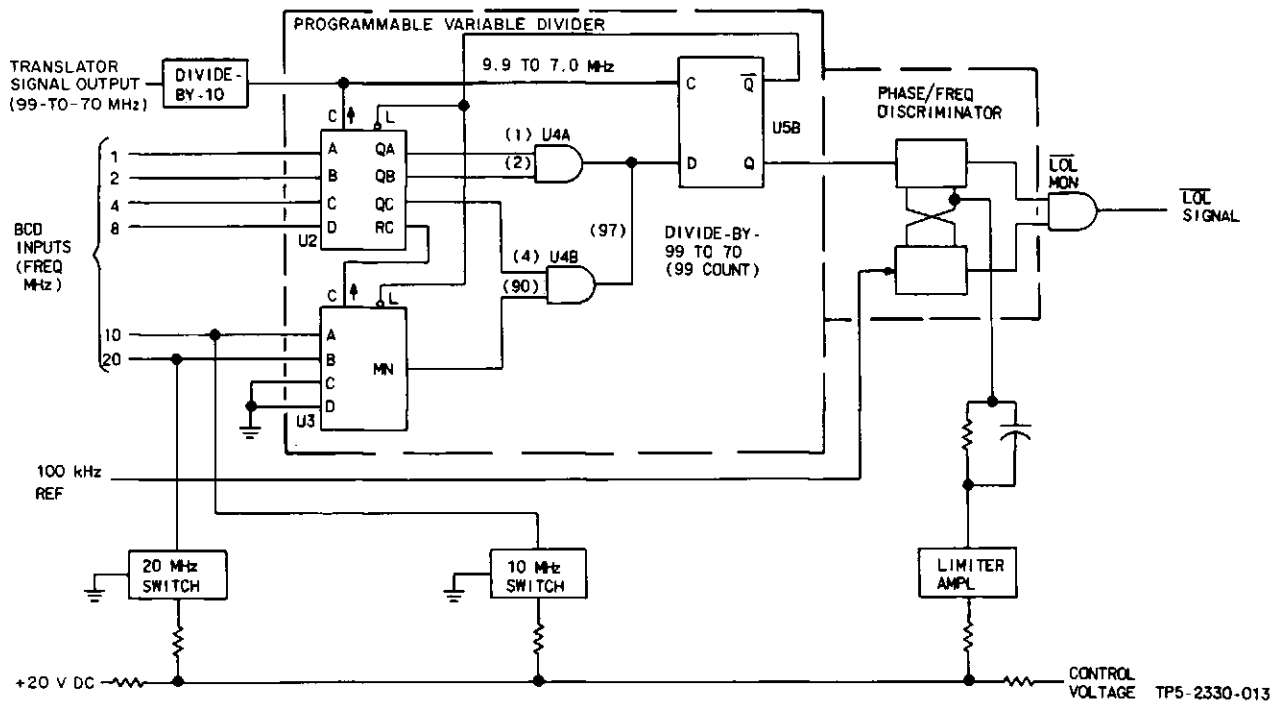
The output vco circuit is phase-locked to the high reference input and through the translator phase-lock loop to the 100-kHz reference input.

The output vco output (109.35 to 79.3501 MHz) is supplied as the variable injection to associated rf circuits.

2.2 *Translator Logic Circuits*

The translator logic circuits receive a 100-kHz reference input, a translator vco signal output, and bcd frequency inputs for 0, 1, 2, 4, 8, 10, and 20 MHz; it also supplies a control voltage output signal to the translator vco.

Refer to figure 3. The translator vco signal output (99 to 70 MHz) is supplied through a fixed divide-by-10 network (9.9 to 7.0 MHz) and applied as the clock input to a programmable variable divider. The output of the programmable variable divider (100 kHz) is supplied to a phase/frequency discriminator and is compared with a 100-kHz reference input. A phase or frequency difference in the discriminator causes a control voltage input increase or decrease to adjust the frequency of the vco. If there is no phase or frequency difference, the discriminator provides a logic 1 lock signal output indicating the vco frequency is locked. Note that a 10- or 20-MHz bcd input enables switches that change the limiter amplifier voltage divider ratio to equalize the loop gain over the frequency range.



Translator Logic Circuits
Figure 3

The programmable variable divider is programmed by bcd frequency inputs. For example, if a bcd input of 00 MHz is applied, the up/down decade counter is programmed to load the count 0 at any time a load signal (logic 0) is applied. Refer to table 1. This programs the variable divider to count from 0 (first count 1) to 99 (last count 99/0), causing the output of the variable divider to be 1/99th of the clock input, or divide-by-99 with a bcd input of 00. Note that as the bcd input goes up 1, 2, 3 etc, the division ratio goes down 98, 97, 96, etc. Also note that for the divide-by circuit to operate as a constant, the last count 99 must also be the loaded count (in the case of bcd 00, count 0). To do this, prerecognition of count 99 is required. Look-ahead circuit of U4A and U4B performs this function. At clock 97 (count 97) gates U4A and U4B are ANDed and supply a logic 1 input to U5B-D. With a logic 1 at U5B-D, clock 98 (count 98) causes U5B-$\overline{Q}$ to go to logic 0 and loads decade counter to bcd input (ANDed outputs of U4A and U4B are removed). At clock 98, U5B-Q supplies a pulse to phase/frequency discriminator. Clock 99 (count 00) causes U5B-$\overline{Q}$ to go to logic 1 and enables decade counter to count on the next clock. Next clock is one above the bcd programmed input. Note that count 98 initiates the output from the divider and count 99 appears only as the bcd programmed input. Refer to figure 4. A 15-MHz programmed input is shown; the same principles apply to any other programmed bcd input.

2.3 Translator VCO Circuits

The translator vco circuits receive a control voltage from the translator logic circuits. The control voltage drives the vco to the required translator frequency. The translator signal output is supplied through one buffer amplifier to the output mixer circuits and through a second buffer amplifier to the translator logic circuits.

2.4 Output Mixer Circuits

The output mixer circuits receive a translator signal input (99 to 70 MHz) from the translator vco. The translator vco signal is mixed with the output vco frequency (109.35 to 79.35001 MHz) and a resulting difference frequency (10.35 to 9.35001 MHz) is supplied through a low-pass filter to the output logic circuits.

2.5 Output Logic Circuits

The output logic circuits receive the output mixer difference frequency (10.35 to 9.35001 MHz), a tracking voltage from the translator vco, and a high reference input signal (1.035 to 0.935001 MHz), and supply a control voltage output signal to operate the output vco.

Table 1. Variable Divider, Logic Truth Table.

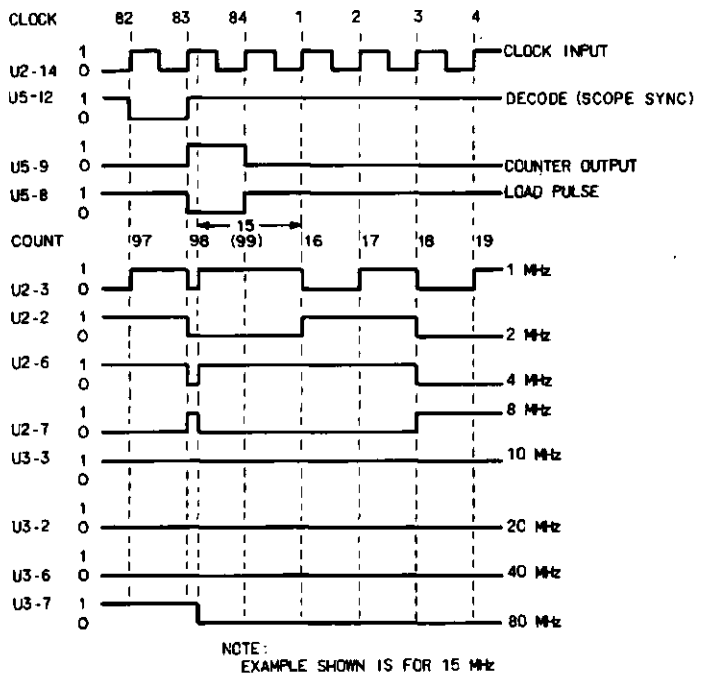
FREQUENCY CONTROL (MHz)	PROGRAMMABLE INPUTS								OUTPUT COUNT	DIVIDE-BY	LOOP FREQUENCY (MHz)
	U2				U3						
	A	B	C	D	A	B	*C	*D			
0	0	0	0	0	0	0	0	0	0	99	99
1	1	0	0	0	0	0	0	0	1	98	98
2	0	1	0	0	0	0	0	0	2	97	97
3	1	1	0	0	0	0	0	0	3	96	96
4	0	0	1	0	0	0	0	0	4	95	95
5	1	0	1	0	0	0	0	0	5	94	94
6	0	1	1	0	0	0	0	0	6	93	93
7	1	1	1	0	0	0	0	0	7	92	92
8	0	0	0	1	0	0	0	0	8	91	91
9	1	0	0	1	0	0	0	0	9	90	90
10	0	0	0	0	1	0	0	0	10	89	89
11	1	0	0	0	1	0	0	0	11	88	88
12	0	1	0	0	1	0	0	0	12	87	87
13	1	1	0	0	1	0	0	0	13	86	86
14	0	0	1	0	1	0	0	0	14	85	85
15	1	0	1	0	1	0	0	0	15	84	84
16	0	1	1	0	1	0	0	0	16	83	83
17	1	1	1	0	1	0	0	0	17	82	82
18	0	0	0	1	1	0	0	0	18	81	81
19	1	0	0	1	1	0	0	0	19	80	80
20	0	0	0	0	0	1	0	0	20	79	79
21	1	0	0	0	0	1	0	0	21	78	78
22	0	1	0	0	0	1	0	0	22	77	77
23	1	1	0	0	0	1	0	0	23	76	76
24	0	0	1	0	0	1	0	0	24	75	75
25	1	0	1	0	0	1	0	0	25	74	74
26	0	0	1	0	0	1	0	0	26	73	73
27	1	1	1	0	0	1	0	0	27	72	72
28	0	0	0	1	0	1	0	0	28	71	71
29	1	0	0	1	0	1	0	0	29	70	70

*Grounded inputs (fixed logic 0)

Refer to figure 5. The output mixer difference frequency (10.35 to 9.35001 MHz) is supplied through a squaring amplifier and a fixed divide-by-10 network (1.035 to 0.935001 MHz), to a phase/frequency discriminator. This frequency from the divide-by-10 network is compared with the high reference input signal (1.035 to 0.935001 MHz). A phase or frequency difference in the discriminator causes the control voltage to increase or decrease to adjust the frequency of the vco. If there is no phase or frequency difference, the discriminator provides a logic 1 lock signal output and the vco frequency locks. Note that the translator tracking voltage is summed with the output logic circuits' control voltage to provide control voltage for the total variable injection frequency output (109.35 to 79.35001 MHz).

2.6 Output VCO Circuits

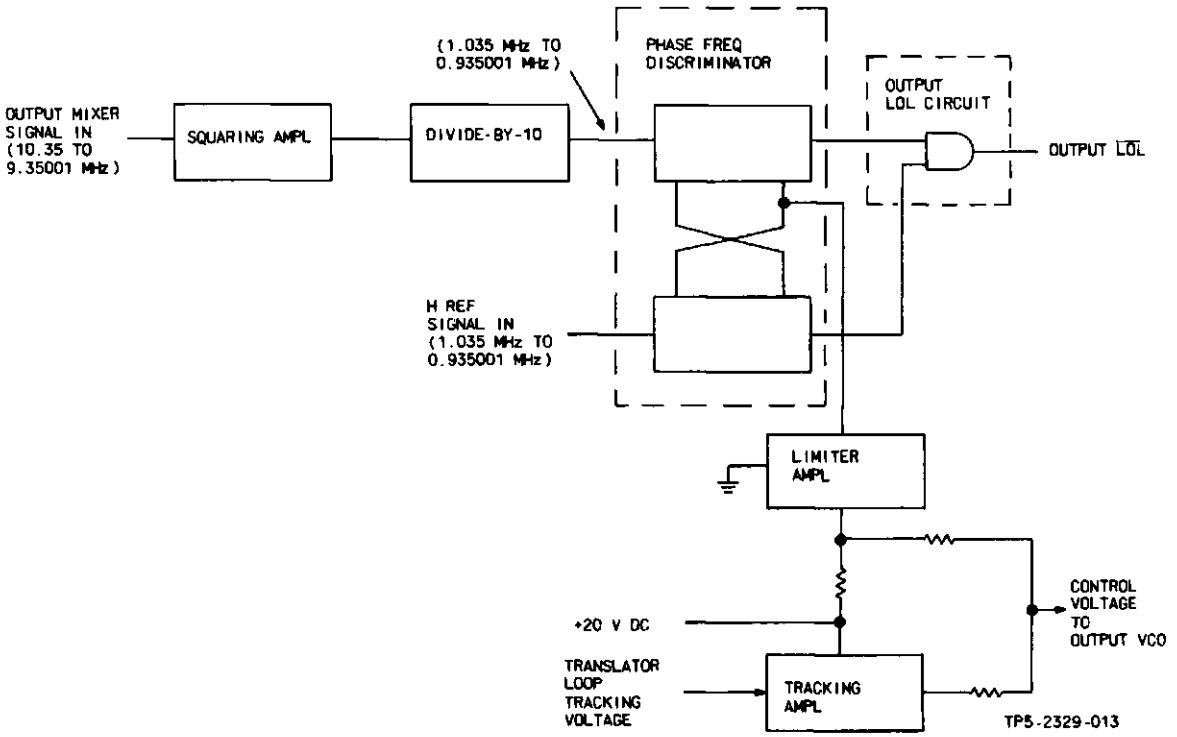
The output vco circuits receive a control voltage from the output logic circuits. The control voltage drives the vco to the required output variable injection frequency. The output variable injection frequency is supplied through one output amplifier to the unit under control and through a second output amplifier to the output mixer circuits.



	PROGRAMMED BCD INPUTS	
MHz	PIN NO.	LOGIC LEVEL
1	U2-15	1
2	U2-1	0
4	U2-10	1
8	U2-9	0
10	U3-15	1
20	U3-1	0
40	U3-10	FXD 0
80	U3-9	FXD 0

TP5-2331-013

Variable Divider, Inputs and Outputs
Figure 4



Output Logic Circuits
Figure 5

2.7 *Up/Down Decade Counter 74LS190 (Refer to table 2 and figure 6.)*

The 74LS190 up/down decade counter is a 4-bit decade counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when input conditions are met.

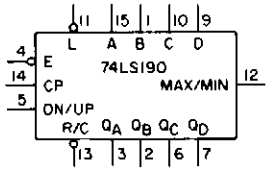
A high at the enable input inhibits counting. A low at the enable input and a low-to-high clock transition triggers the four master/slave flip-flops. The enable input should be changed only when the clock is high. The down/up input determines the direction of the count. When low, the count goes up; when high, the count goes down.

These counters are programmable. The outputs may be preset to any state by placing a low on the load input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the state of the clock input. This allows the counters to be used as modulo N dividers by modifying the count length with the preset inputs.

Two outputs are available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low level output pulse equal in width to the low level portion of the clock input when an overflow or underflow condition exists. The counters are cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

2.8 *Decade Counter 74LS90 (Refer to table 3 and figure 7.)*

The 74LS90 decade counter is a high-speed, monolithic decade counter consisting of four dual-



V_{CC} = PIN 16

GND = PIN 8

TP5-2325-013

Up/Down Decade Counter 74LS190
Figure 6

Table 2. Up/Down Decade Counter, Logic Truth Table.

PROGRAMMABLE INPUTS				COUNT	BCD OUTPUTS			
A	B	C	D		QA	QB	QC	QD
0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	0	0	0
0	1	0	0	2	0	1	0	0
1	1	0	0	3	1	1	0	0
0	0	1	0	4	0	0	1	0
1	0	1	0	5	1	0	1	0
0	1	1	0	6	0	1	1	0
1	1	1	0	7	1	1	1	0
0	0	0	1	8	0	0	0	1
1	0	0	1	9	1	0	0	1

E (enable): logic 0 enables counter; logic 1 inhibits counter.

L (load): logic 0 programs the bcd output count to be set at the bcd count of the programmable inputs; the next clock pulse counts one higher/lower (up/down).

DU (down/up): logic 0 counts up; logic 1 counts down.

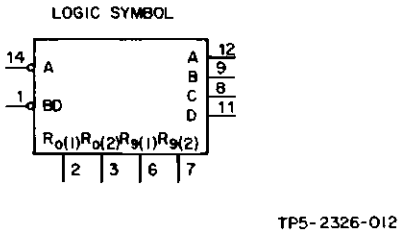
CP (clock pulse): logic 0-to-logic 1 transition advances counter.

RC (ripple clock): logic 0 pulse equal to 1/2 clock cycle when an overflow occurs.

MM (maximum/minimum count): logic 1 pulse equal to full clock cycle when an overflow or underflow occurs.

rank, master-slave flip-flops internally interconnected to provide a divide-by-2 counter and a divide-by-5 counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logic 0 or to a binary coded decimal (bcd) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated into the three following independent count modes:

a. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the bcd count sequence truth table shown above. In addition to a conventional 0 reset, inputs are provided to reset a bcd 9-count for 9's complement decimal applications.
b. If a symmetrical divide-by-10 count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of 10, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-10 square wave is obtained at output A.



Decade Counter 74LS90
Figure 7

c. For operation as a divide-by-2 counter and divide-by-5 counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-2 function. The BD input is used to obtain binary divide-by-5 operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

2.9 Dual D-Type Flip-Flop With Preset and Clear 74LS74 (Refer to table 4 and figure 8.)

The 74LS74 consists of dual high-speed, D-type flip-flops. Information on the D input is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either high or low level, the D input signal has no effect.

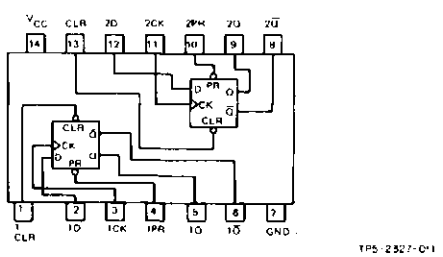
3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the synthesizer output module are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 5 check total performance of the synthesizer output module. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.



Dual D-Type Flip-Flop With Preset and Clear 74LS74
Figure 8

Table 3. Decade Counter 74LS90, Logic Truth Table.

*BCD COUNT SEQUENCE				
COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

**RESET/COUNT							
RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	Count			
0	X	0	X	Count			
0	X	X	0	Count			
X	0	0	X	Count			

*Output A connected to input BD for BCD count.
**X indicates that either a logical 1 or a logical 0 may be present.

Table 4. Dual D-Type Flip-Flop With Preset and Clear 74LS74, Logic Truth Table.

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	*H	*H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_O	$\overline{Q_O}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_O = the level of Q before the indicated input conditions were established.
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Table 5. Synthesizer Output, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of the unit containing the synthesizer output that is to be tested.		
	b. Remove cover from the synthesizer section of the unit.		
	c. Remove synthesizer output and install it on an extender card and place it in the unit.		
	d. Set unit LINE SELECTOR switch to 115 V.		
	e. Connect unit to 115-V ac power source and set power on.		
	f. Measure dc voltage from J1-19 to J1-17 (ground).	+5.2 +0.2 V dc.	Check unit synthesizer voltage regulator.
	g. Measure dc voltage from J1-7 to J1-17 (ground).	NLT +19.5 V dc. NMT +20.8 V dc.	Check unit synthesizer voltage regulator.
	h. Measure dc voltage from J1-20 to J1-17 (ground).	+8.0 ±0.5 V dc.	Check unit power supply.
	i. Set unit MODE switch to ISB.		
2. Synthesizer output	a. Set FREQUENCY KHZ control on front panel to 29555.55 (or 29555.5).		
	b. Using a frequency counter, measure the high reference input between P1-1 and P1-2 (ground).	979 ±1 kHz. Note actual frequency	Check unit decades one at a time.
	c. Measure the dc voltage at A3E110. (Refer to note and chart at end of test 2 for voltages and frequencies at different 10 and 1 MHz settings.)	4.51 ±0.1 V dc.	Adjust L2 for 4.90 ±0.1 V dc. If L2 adjustment does not correct the problem check Q4, Q5, and associated circuit.
	d. Using a frequency counter, measure the output at P2.	79.79 ±0.005 MHz. (Actual should equal 79.35 MHz plus the difference between 1035 kHz and the actual frequency in step a.)	Adjust L3 for actual frequency with required V dc at A1E100. If L3 adjustment does not correct the problem check A1A1Q1, A1A1Q2, A1A103, and associated circuits.
	e. Measure the dc voltage at A1E100.	4.80 ±0.1 V dc.	Same as step d.
	f. Note the dc voltage at A1E100 while moving the 10 and 1 MHz frequency controls from 9 down to 0.	Refer to chart at end of test 2. (Voltage goes up as frequency controls go down.)	Adjust L3 so that all settings fall into the limits shown in chart.
(Cont)			

Table 5. Synthesizer Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	g. Set FREQUENCY KHZ control on front panel to 00000.00 (or 00000.0).		
	h. Using a frequency counter, measure the high reference input between P1-1 and P1-2 (ground).	1035 ±0.5 kHz.	Check unit 100-kHz decade.
	i. Using a frequency counter, measure the output at P2.	109.350 MHz ±0.5 kHz.	Check A4A1U1 thru A4A1U5 and associated circuits.
	j. Set FREQUENCY KHZ control on front panel to 29999.99 (or 29999.9).		
	k. Using a frequency counter, measure the output at P2.	79.350 MHz ±0.5 kHz.	Same as step i.
	l. Measure the dc voltage at P1-8 to ground.	NLT +3.5 V dc. **Note** RCV FAULT, EXCTR FAULT, or R/E FAULT indicator lighting indicates that results of step m are satisfactory.	Check A4A1U4 and A4A1U6 thru A4A1U8.
	m. Ground P1-10 while noting the voltage at P1-8.	NMT 0.5 V dc.	Same as step l.
	n. Remove P1-10 ground.		
	o. Set front-panel PWR switch off.		
	p. Remove 100-kHz decade from unit under test.		
	q. Set front-panel PWR switch on.		
	r. Measure the dc voltage at P1-8 to ground.	NMT 0.5 V dc.	Check A2A1U3 thru A2A1U5.
	s. Set front-panel PWR switch off.		
(Cont)	t. Replace 100-kHz decade in unit under test.		

Table 5. Synthesizer Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL

2. (Cont)

Note

The following chart is shown with an input frequency of 1035 ±5 kHz. The actual output frequency with an input frequency can be determined using the following formula:

AF = LF - 100 kHz + 1035 kHz - IF.

AF = actual output frequency at P1-1.

LF = output frequency listed in chart for associated MHz frequency digits.

IF = actual input frequency.

10-MHz FREQ DIGIT	1-MHz FREQ DIGIT	A3E110 DC VOLTAGE	XLTR FREQ A3A1E9 (MHz)	A1E100 DC VOLTAGE	OUTPUT FREQ P2 (MHz)
2	9	4.90	70.000	4.80	80.350
	8	5.20	71.000	5.05	81.350
	7	5.50	72.000	5.30	82.350
	6	5.80	73.000	5.60	83.350
	5	6.10	74.000	5.85	84.350
	4	6.40	75.000	6.15	85.350
	3	6.70	76.000	6.40	86.350
	2	7.05	77.000	6.70	87.350
	1	7.35	78.000	7.00	88.350
	0	7.70	79.000	7.25	89.350
1	9	8.00	80.000	7.55	90.350
	8	8.35	81.000	7.85	91.350
	7	8.70	82.000	8.15	92.350
	6	9.00	83.000	8.45	93.350
	5	9.35	84.000	8.80	94.350
	4	9.70	85.000	9.10	95.350
	3	10.10	86.000	9.40	96.350
	2	10.45	87.000	9.75	97.350
	1	10.85	88.000	10.05	98.350
	0	11.20	89.000	10.40	99.350
0	9	11.60	90.000	10.75	100.350
	8	12.00	91.000	11.10	101.350
	7	12.40	92.000	11.50	102.350
	6	12.85	93.000	11.90	103.350
	5	13.30	94.000	12.30	104.350
	4	13.75	95.000	12.75	105.350
	3	14.20	96.000	13.25	106.350
	2	14.70	97.000	13.75	107.350
	1	15.25	98.000	14.30	108.350
	0	15.80	99.000	14.90	109.350

Note

Table shown with an input frequency of 1035 ±5 kHz (front-panel FREQUENCY KHZ setting of XX000.00 (or XX000.0)). Frequencies shown ±0.0005 MHz, voltages shown ±0.1 V dc.

4. ALIGNMENT/ADJUSTMENT

Note

Perform these adjustments only if repairs have been made and test procedures in table 5 cannot meet the normal indications.

4.1 Translator VCO Tracking

a. Perform setup of table 5, test 1.
b. Adjust the slug in oscillator coil A3A1L2 to approximately 1.6 mm (1/16 in) below coil form.
c. Adjust the plates in oscillator capacitor A3A1C7 two turns below the top of capacitor form.
d. Set front-panel FREQUENCY KHZ to 29000.00 (or 29000.0).
e. Connect a frequency counter between P1-1 and P1-2 (ground). Must equal 1035 ±0.5 kHz.
f. Connect a frequency counter between P1-10 and P1-9 (ground). Must equal 100 ±0.01 kHz.
g. Connect a frequency counter at A3A1E5 to A3A1E4 (ground).
h. Adjust the slug in oscillator coil A3A1L2 for 70.000 MHz ±20 kHz.
i. Set front-panel FREQUENCY KHZ to 00000.00 (or 00000.0).
j. Adjust the plates in oscillator capacitor A3A1C7 for 99.000 MHz ±20 kHz.

Note

Adjust capacitor A3A1C7 for an error opposite the error of coil A3A1L2. Example, if A3A1L2 is adjusted at 70.000 MHz minus 20 kHz, adjust A3A1C7 for 99.000 MHz plus 20 kHz.

k. Repeat steps f through j until low and high frequencies are within 10 kHz of the correct frequency.

4.2 Output VCO Tracking

a. Perform setup of table 5, test 1.
b. Adjust the slug in oscillator coil A1A1L3 to approximately 1.6 mm (1/16 in) below coil form.
c. Adjust the plates in oscillator capacitor A1A1C2 two turns below the top of capacitor form.
d. Set front-panel FREQUENCY KHZ to 29000.00 (or 29000.0).
e. Connect a frequency counter between P1-1 and P1-2 (ground). Must equal 1035 ±0.5 kHz.
f. Connect a frequency counter between P1-10 and P1-9 (ground). Must equal 100 ±0.01 kHz.
g. Connect a frequency counter with 50-Ω load at P2.
h. Adjust the slug in oscillator coil A1A1L3 for 80.350 MHz ±20 kHz.
i. Set front-panel FREQUENCY KHZ to 00000.00 (or 00000.0).
j. Adjust the plates in oscillator capacitor A1A1C2 for 109.350 MHz ±20 kHz.

Note

Adjust capacitor A1A1C2 for an error opposite the error of coil A1A1L3. Example, if A1A1L3 is adjusted at 80.350 MHz minus 20 kHz, adjust A1A1C2 for 109.350 MHz plus 20 kHz.

k. Repeat steps f through j until low and high frequencies are within 10 kHz of the correct frequency.

4.3 Output VCO Level Adjustment

a. Perform setup of table 5, test 1.
b. Connect an rf voltmeter with 50-Ω load to P2.
c. Set front-panel FREQUENCY KHZ to 16000.00 (or 16000.0).
d. Adjust A1A1R4 for +7 dB mW on rf voltmeter.

Note

A1A1R10 may be replaced with a selected resistor (50 through 720 Ω) to meet this adjustment.

4.4 Output VCO Final Tuning

a. Perform setup of table 5, test 1.
b. Connect a high-impedance scope probe to A2A1U4-6.

Note

A steady rectangular waveform should be seen. The object of this adjustment is to make the rectangular waveform as near a square wave as possible throughout the synthesizer output tuning range.

c. Set front-panel FREQUENCY KHZ controls to 29 555.55 kHz.
d. Adjust A1A1L3 for a 42-percent duty ratio (square wave, 42-percent logic 1, 58-percent logic 0).
e. Set front-panel FREQUENCY KHZ controls to 00 555.55 kHz.

f. Adjust A1A1C2 for duty ratio, opposite that indicated. For example, if a 30-percent duty ratio is indicated, adjust for a 70-percent duty ratio.
g. Repeat steps c through f until the duty ratio at both end frequencies is between 45 and 55 percent.

5. REPAIR

Repair of the synthesizer output module is accomplished using standard planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

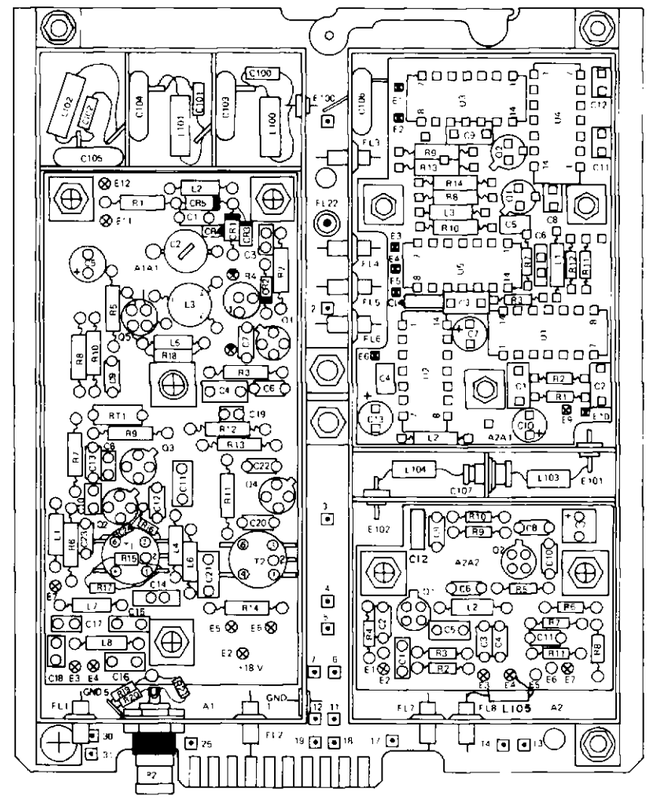
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figure 9). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

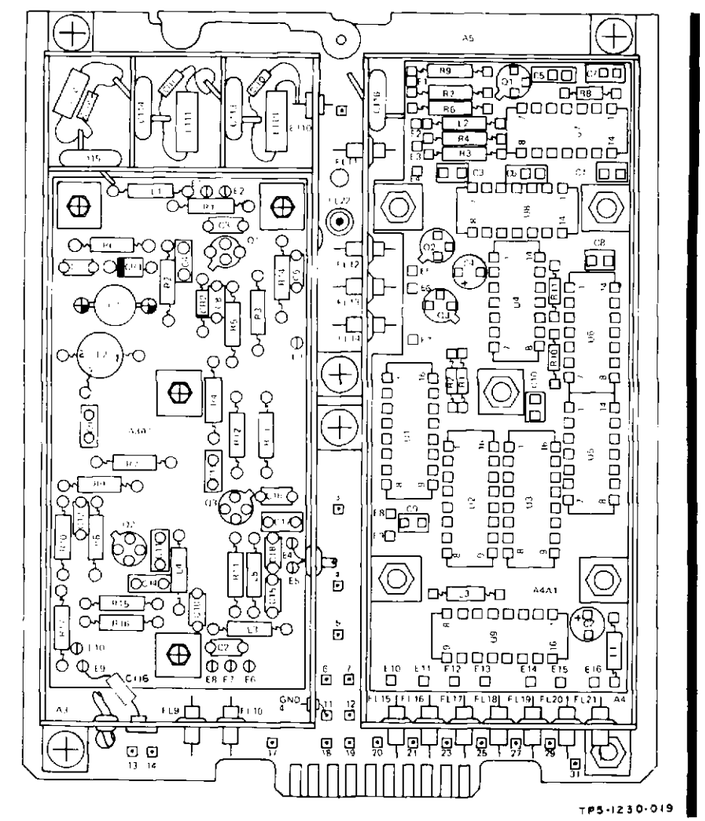
Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description is listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses, and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Synthesizer output	635-4930-001	REV E
Output vco assy A1	637-1760-001	REV E
Output vco board A1A1	635-0890-002	REV F
Output mixer-logic assy A2	637-1761-001	REV E
Output logic board A2A1	635-0836-001	REV C
Output mixer board A2A2	635-0837-001	REV B
Translator vco assy A3	637-1763-001	REV F
Translator vco board	635-0846-001	REV D
Translator logic assy A4	637-1762-001	REV D
Translator logic board	635-0646-001	REV B





Synthesizer Output, Schematic Diagram
Figure 9 (Sheet 1 of 5)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	SYNTH OUTPUT 635-4930-001		
A1	OUTPUT VCO	637-1760-001	
A2	OUTPUT MIXER/LOGIC	637-1761-001	
A3	TRANSLATOR VCO	637-1763-001	
A4	TRANSLATOR LOGIC	637-1762-001	
A5	CONNECTOR BOARD	635-0998-001	
FL1-FL21	NOT USED		
FL22	FILTER, RAD INTR 1750pF	241-5006-010	
	OUTPUT VCO A1 637-1760-001		
A1	OUTPUT VCO BOARD	635-0890-002	
C1-C99	NOT USED		
C100	CAPACITOR, FXD, CER DIEL, 18pF, 10%, 75V	913-1098-030	
C101	CAPACITOR, FXD, CER DIEL, 0.00015μF, 5%, 100V	913-3117-050	
C102	CAPACITOR, FXD, MICA DIEL, 68pF, ±0.5pF, 50V	912-4141-330	
C103, C104	CAPACITOR, FXD, MICA DIEL, 1500pF, 5%, 500V	912-4114-370	
C105	CAPACITOR, FXD, MICA DIEL, 750pF, 5%, 500V (A8)	912-4114-350	
C105	CAPACITOR, FXD, MICA DIEL, 1500pF, 5%, 500V	912-4114-370	
FL1, FL2	FILTER, RAD INTR, 1750pF	241-5006-010	
L1-L99	NOT USED		
L100-L102	COIL, RF, 15000μH	240-2715-630	
P1	NOT USED		
P2	CONNECTOR, RCPT, ELEC	357-7207-090	
R1-R18	NOT USED		
R19, R20	RESISTOR, FXD, CMPSN, 270Ω, 10%, 1/8W (A7)	745-2320-000	
R21	RESISTOR, FXD, CMPSN, 18Ω, 10%, 1/8W (A7)	745 2277-000	
	OUTPUT VCO BOARD A1A1 635-0890-002		
CR1	SEMICOND DEVICE, BB109	922-6131-010	
CR2	SEMICOND DEVICE, 1N5711	353-3691-010	
CR3-CR5	SEMICOND DEVICE, BB109 (A6)	922-6131-010	
C1	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V (A6)	913-4018-000	
C2	CAPACITOR, VAR, AIR DIEL, 1 TO 10pF, 200V	922-0583-230	
C3	CAPACITOR, FXD, CER DIEL, 18pF, 10%, 75V	913-1098-030	
C4	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C5	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-240	
C6	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V (A6)	913-4018-000	
C6	CAPACITOR, FXD, CER DIEL, 470pF, 10%, 200V	913-4014-000	
C7	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C8	CAPACITOR, FXD, CER DIEL, 15pF, 5%, 75V (A6)	913-1098-180	
C9	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V (A6)	913-4018-000	
C9	CAPACITOR, FXD, MICA DIEL, 27pF, 5%, 50V	912-4141-180	
C10	CAPACITOR, FXD, CER DIEL, 0.00047μF, 5%, 100V	913-3117-080	
C11	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C12, C13	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C14	CAPACITOR, FXD, CER DIEL, 47pF, ±0.25pF, 150V	913-1098-370	
C15	CAPACITOR, FXD, MICA DIEL, 33pF, 5%, 50V	913-4141-220	
C16	CAPACITOR, FXD, MICA DIEL, 51pF, 5%, 50V	912-4141-300	
C17	CAPACITOR, FXD, CER DIEL, 0.00068μF, 5%, 100V	913-3117-090	
C18	CAPACITOR, FXD, CER DIEL, 270pF, 5%, 100V	913-1098-470	
C19	CAPACITOR, FXD, CER DIEL, 3pF, ±0.25pF, 150V	913-1098-340	
C20	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C21	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C22	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C23	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	
C24	CAPACITOR, FXD, MICA DIEL, 8pF, ±.5pF, 300V (A6)	912-4141-110	
L1	COIL, RF, 100μH	240-2047-000	
L2	COIL, RF, 2.70μH (A6)	240-2028-000	
L2	COIL, RF, 15μH	240-2037-000	
L3	COIL, ADJUSTABLE	637-4502-001	
L4	COIL, RF, 100μH	240-2047-000	
L5	COIL, RF, 1μH (A4)	240-2023-000	
L6	COIL, RF, 100μH	240-2047-000	

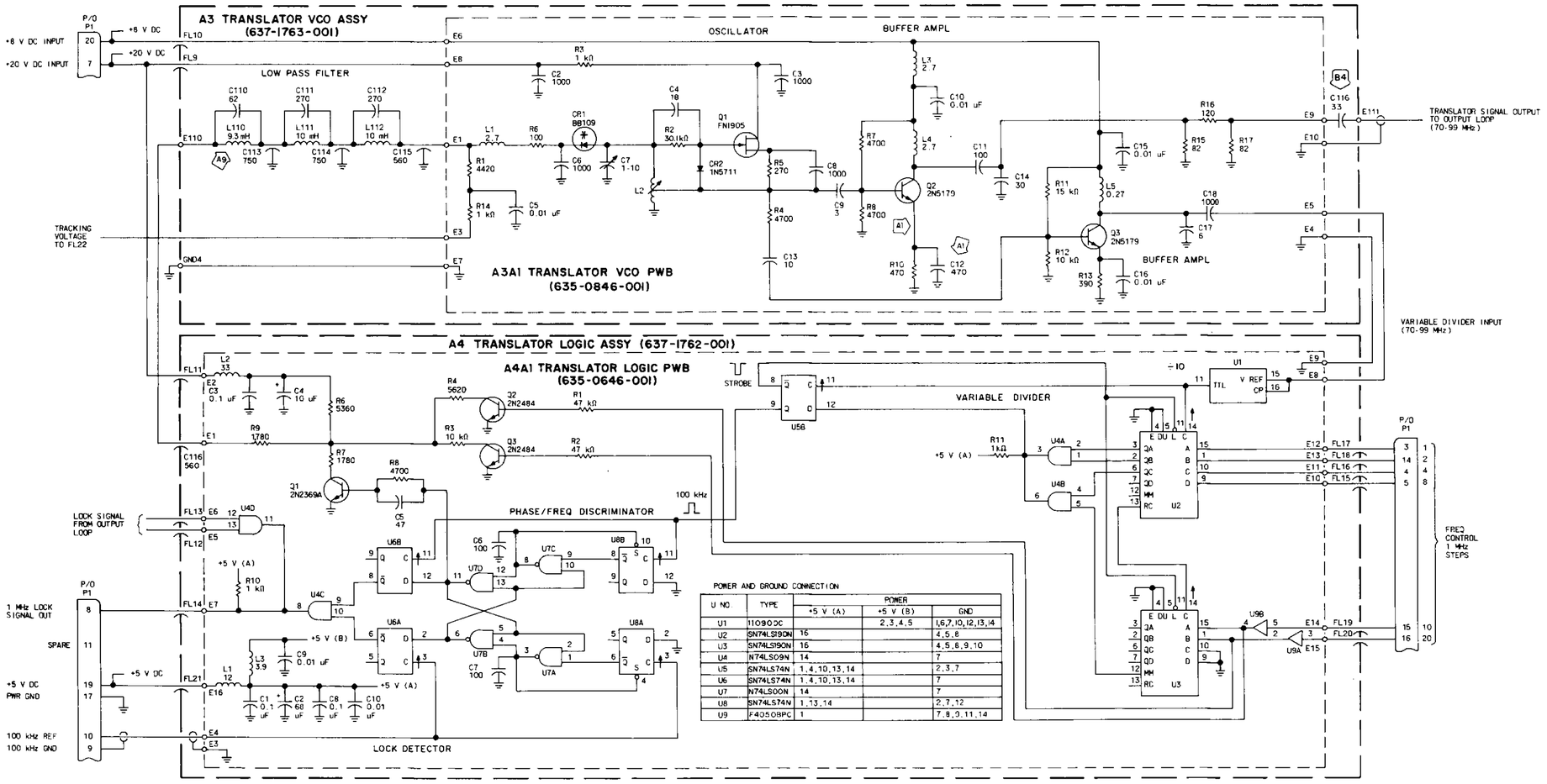
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART	USABLE ON CODE
L7, L8	COIL, RF, 0.100μH	240-2723-140	
Q1	TRANSISTOR, FN1905	352-0756-050	
Q2	TRANSISTOR, 2N918	352-0440-000	
Q3, Q4	TRANSISTOR, 2N5179	352-0792-020	
Q5	TRANSISTOR, FN1905 (A5)	352-0756-050	
R1	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R2	RESISTOR, FXD, FILM, 30.1kΩ, 1%, 1/8W (A6)	705-1067-000	
R2	RESISTOR, FXD, FILM, 68.1kΩ, 1%, 1.8W	705-1084-000	
R3	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W (A6)	745-0749-000	
R3	RESISTOR, FXD, CMPSN, 560Ω, 10%, 1/4W	745-0740-000	
R4	RESISTOR, VAR, 1kΩ, 10%, 0.5W (A11)	382-00	
R4	RESISTOR, FXD, CMPSN, 150 THRU 560Ω, 10%, 1/4W	638-6457-001	
R5	RESISTOR, FXD, CMPSN, 220Ω, 10%, 1/4W	745-0725-000	
R6	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 1/4W	745-0761-000	
R7	RESISTOR, FXD, CMPSN, 1.5kΩ, 10%, 1/4W	745-0755-000	
R8	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 1/4W	745-0761-000	
R9	RESISTOR, FXD, CMPSN, 68Ω, 10%, 1/4W (A5)	745-0707-000	
R9	RESISTOR, FXD, CMPSN, 22Ω, 10%, 1/4W	745-0689-000	
R10	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W (A2)	745-0713-000	
R10	RESISTOR, FXD, CMPSN, 100 THRU 390Ω, 10%, 1/4W (A5)	638-1088-001	
R10	RESISTOR, FXD, CMPSN, 180Ω, 10%, 1/4W	745-0722-000	
R11	RESISTOR, FXD, CMPSN, 2.7kΩ, 10%, 1/4W	745-0764-000	
R12	RESISTOR, FXD, CMPSN, 680Ω, 10%, 1/4W (A2)	745-0743-000	
R12	RESISTOR, FXD, CMPSN, 560Ω, 10%, 1/4W	745-0740-000	
R13	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R14	RESISTOR, FXD, CMPSN, 56Ω, 10%, 1/4W	745-0704-000	
R15	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/8W (A3, A4) OR	745-2304-000	
R15	RESISTOR, FXD, CMPSN, 150Ω, 10%, 1/8W (A3, A4)	745-2311-000	
R16	RESISTOR, FXD, CMPSN, 47Ω, 10%, 1/8W (A6)	745-2292-000	
R17	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/8W (A6)	745-2323-000	
R18	RESISTOR, FXD, CMPSN, 820Ω, 10%, 1/8W (A6)	745-2338-000	
RT1	RESISTOR, THRM, 220Ω, 10%, 1/2W	714-1721-000	
T1	TRANSFORMER, RF (A5)	278-0430-200	
T1	TRANSFORMER, RF	278-0430-290	
T2	TRANSFORMER, RF	278-0430-200	
	OUTPUT MIXER/LOGIC A2 637-1761-001		
A1	OUTPUT LOGIC BOARD	635-0836-001	
A2	OUTPUT MIXER BOARD	635-0837-001	
C1-C105	NOT USED		
C106	CAPACITOR, FXD, MICA DIEL, 750pF, 5%, 500V	912-4114-350	
C107	CAPACITOR, FXD, CER DIEL, 15pF, 20%, 500V	913-3111-050	
FL1, FL2	NOT USED		
FL3-FL8	FILTER, RAD INTR, 1750pF	241-5006-010	
L1-L102	NOT USED		
L103-L104	COIL, RF, 10μH	240-2715-250	
L105	COIL, RF, 100μH (B3)	240-2047-000	
	OUTPUT LOGIC BOARD A2A1 635-0836-001		
C1-C3	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C4	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C5	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C6	CAPACITOR, FXD, CER DIEL, 47pF, 10%, 75V	913-1098-020	
C7	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-680	
C8	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C9	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C10	CAPACITOR, FXD, ELCTLT, 68μF, 20%, 6V	184-9102-040	
C11, C12	CAPACITOR, FXD, CER DIEL, 100pF, 5%, 100V	913-3281-280	
C13	CAPACITOR, FXD, ELCTLT, 0.47μF, 20%, 35V	184-9102-330	
C14	CAPACITOR, FXD, MICA DIEL, 150pF, 5%, 50V (B2)	912-4141-400	
L1, L2	COIL, RF, 100μH	240-2047-000	
L3	COIL, RF, 4.70μH (B2)	240-2031-000	
L3	COIL, RF, 100μH	240-2047-000	
Q1	TRANSISTOR, 2N930	352-0517-010	
Q2	TRANSISTOR, 2N2369A	352-0596-030	
R1, R2	RESISTOR, FXD, CMPSN, 470Ω, 10%, 1/8W	745-2329-000	

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
R3	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/8W	745-2341-000	
R4-R6	NOT USED		
R7	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/8W	745-2365-000	
R8	RESISTOR, FXD, FILM, 33.2kΩ, 1%, 1/8W (A10)	705-1069-000	
R8	RESISTOR, FXD, FILM, 21kΩ, 1%, 1/8W	705-3605-630	
R9	RESISTOR, FXD, FILM, 3.48kΩ, 1%, 1/8W	705-1022-000	
R10	RESISTOR, FXD, FILM, 3.83kΩ, 1%, 1/8W	705-1024-000	
R11	RESISTOR, FXD, FILM, 10kΩ, 1%, 1/20W	705-3163-120	
R12	RESISTOR, FXD, CMPSN, 10Ω, 10%, 1/8W	745-2377-000	
R13	RESISTOR, FXD, FILM, 4.64kΩ, 1%, 1/8W	705-1028-000	
R14	RESISTOR, FXD, FILM, 464Ω, 1%, 1/8W	705-0980-000	
U1	INTEGRATED CKT, N74LS04N	351-1523-090	
U2	INTEGRATED CKT, SN74LS90N	351-1636-010	
U3	INTEGRATED CKT, SN74LS74N	351-1525-040	
U4	INTEGRATED CKT, N74LS00N	351-1523-110	
U5	INTEGRATED CKT, SN74LS74N	351-1525-040	
	OUTPUT MIXER BOARD A2A2 635-0837-001		
C1	CAPACITOR, FXD, MICA DIEL, 10pF, ±0.5pF, 50V	912-4141-020	
C2, C3	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	912-4018-000	
C4	CAPACITOR, FXD, CER DIEL, 0.1μF, 10%, 50V	913-5019-320	
C5	CAPACITOR, FXD, MICA DIEL, 5pF, ±0.5pF, 50V	912-4141-010	
C6	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C7	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-240	
C8-C10	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	
C11	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C12	CAPACITOR, FXD, MICA DIEL, 22pF ±0.5pF, 300V (B1)	912-4141-030	
L1	NOT USED		
L2	COIL, RF, 0.18μH	240-2014-000	
Q1	TRANSISTOR, 2N5179	352-0792-020	
Q2	TRANSISTOR, 3N187	352-1093-010	
R1	NOT USED		
R2	RESISTOR, FXD, CMPSN, 2.7kΩ, 10%, 1/8W	745-2356-000	
R3	RESISTOR, FXD, CMPSN, 680Ω, 10%, 1/8W	745-2335-000	
R4	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/8W	745-2304-000	
R5	RESISTOR, FXD, CMPSN, 200Ω, 10%, 1/8W	745-2317-000	
R6	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/8W	745-2304-000	
R7	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/8W	745-2377-000	
R8	RESISTOR, FXD, CMPSN, 180Ω, 10%, 1/8W	745-2314-000	
R9, R10	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/8W	745-2341-000	
R11	RESISTOR, FXD, CMPSN, 56Ω, 10%, 1/8W	745-2295-000	
	TRANSLATOR VCO A3 637-1763-001		
A1	TRANSLATOR VCO BOARD	635-0846-001	
C1-C109	NOT USED		
C110	CAPACITOR, FXD, MICA DIEL, 62pF, 5%, 50V	912-4141-320	
C111,C112	CAPACITOR, FXD, CER DIEL, 270pF, 5%, 100V	913-1098-470	
C113, C114	CAPACITOR, FXD, MICA DIEL, 750pF, 5%, 500V	912-4114-350	
C115	CAPACITOR, FXD, MICA DIEL, 560pF, 5%, 500V	912-4114-320	
C116	CAPACITOR, FXD, MICA DIEL, 33pF, 2%, 50V (B4)	912-4141-220	
FL1-FL8	NOT USED		
FL9-FL10	FILTER, RAD INTR, 1750pF	241-5006-010	
L1-L109	NOT USED		
L110	COIL, RF, 10000μH (A9)	240-2715-610	
L110	COIL, WW, 9.3MH	634-5339-001	
L111, L112	COIL, RF, 10000μH	240-2715-610	
	TRANSLATOR VCO BOARD A3A1 635-0846-001		
CR1	SEMICOND DEVICE, BB109	922-6131-010	
CR2	SEMICOND DEVICE, 1N5711	353-3691-010	
C1	NOT USED		
C2, C3	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C4	CAPACITOR, FXD, CER DIEL, 18pF, 10%, 75V	913-1098-030	
C5	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	
C6	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C7	CAPACITOR, VAR, AIR DIEL, 1 TO 10pF, 200V	922-0583-230	
C8	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	

Synthesizer Output, Schematic Diagram
Figure 9 (Sheet 2)



POWER AND GROUND CONNECTION

U NO.	TYPE	POWER		
		+5 V (A)	+5 V (B)	GND
U1	11090DC		2,3,4,5	1,6,7,10,12,13,14
U2	SN74LS190N	16		4,5,8
U3	SN74LS190N	16		4,5,6,9,10
U4	N74LS09N	14		7
U5	SN74LS74N	1,4,10,13,14		2,3,7
U6	SN74LS74N	1,4,10,13,14		7
U7	N74LS00N	14		7
U8	SN74LS74N	1,13,14		2,7,12
U9	F4050BPC	1		7,8,9,11,14

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN PICOFARADS AND INDUCTANCE VALUES ARE IN MICROHENRYS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. P1 IS ON CONNECTOR CARD 635-0998-001.
4. ALL UNMARKED SET AND RESET PINS ARE CONNECTED TO INACTIVE STATE AS SHOWN IN TABLES.
5. TEST SELECT: A1A1R4 FROM 150 Ω TO 560 Ω (A2) (A5) (A3) (A4) (A11)

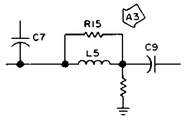
Synthesizer Output, Schematic Diagram
Figure 9 (Sheet 3)

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
C9	CAPACITOR, FXD, MICA DIEL, 3pF, ±0.5pF, 50V	912-4141-070	
C10	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	
C11	CAPACITOR, FXD, CER DIEL, 100pF, 5%, 100V	913-3281-280	
C12	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V (A1)	913-5019-200	
C12	CAPACITOR, FXD, CER DIEL, 470pF, 10%, 200V	913-4014-000	
C13	CAPACITOR, FXD, CER DIEL, 10pF, 5%, 75V	913-1098-010	
C14	CAPACITOR, FXD, MICA DIEL, 30pF, 5%, 50V	912-4141-200	
C15, C16	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	
C17	CAPACITOR, FXD, MICA DIEL, 6pF, ±0.5pF, 50V	912-4141-090	
C18	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
L1	COIL, RF, 2.70μH	240-2028-000	
L2	COIL, ADJUSTABLE	635-9660-001	
L3, L4	COIL, RF, 2.70μH	240-2028-000	
L5	COIL, RF, 0.27μH	240-2016-000	
Q1	TRANSISTOR, FN1905	352-0756-050	
Q2, Q3	TRANSISTOR, 2N5179	352-0792-020	
R1	RESISTOR, FXD, FILM, 4.42kΩ, 1%, 1/8W	705-1027-000	
R2	RESISTOR, FXD, FILM, 30.1kΩ, 1%, 1/8W	705-1067-000	
R3	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W	745-0749-000	
R4	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R5	RESISTOR, FXD, CMPSN, 270Ω, 10%, 1/4W	745-0728-000	
R6	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R7, R8	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R9	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W (A1)	745-0713-000	
R10	RESISTOR, FXD, CMPSN, 470Ω, 10%, 1/4W	745-0737-000	
R11	RESISTOR, FXD, CMPSN, 15kΩ, 10%, 1/4W	745-0791-000	
R12	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R13	RESISTOR, FXD, CMPSN, 390Ω, 10%, 1/4W	745-0734-000	
R14	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W	745-0749-000	
R15	RESISTOR, FXD, CMPSN, 82Ω, 10%, 1/4W	745-0710-000	
R16	RESISTOR, FXD, CMPSN, 120Ω, 10%, 1/4W	745-0716-000	
R17	RESISTOR, FXD, CMPSN, 82Ω, 10%, 1/4W	745-0710-000	
	TRANSLATOR LOGIC A4 637-1762-001		
A1	TRANSLATOR LOGIC BOARD	635-0646-001	
C1-C115	NOT USED		
C116	CAPACITOR, FXD, MICA DIEL, 560pF, 5%, 500V	912-4114-320	
FL1-FL10	NOT USED		
FL11-FL21	FILTER, RAD IN TR, 1750pF	241-5006-010	
	TRANSLATOR LOGIC BOARD A4A1 635-0646-001		
C1	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-180	
C2	CAPACITOR, FXD, ELCTLT, 68μF, 20%, 6V	184-9102-040	
C3	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-180	
C4	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-240	
C5	CAPACITOR, FXD, CER DIEL, 47pF, 10%, 75V	913-1098-020	
C6, C7	CAPACITOR, FXD, CER DIEL, 100pF, 5%, 100V	913-3281-280	
C8	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-180	
C9, C10	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
L1	COIL, RF, 12μH	240-2036-000	
L2	COIL, RF, 33μH	240-2041-000	
L3	COIL, RF, 3.90μH	240-2030-000	
Q1	TRANSISTOR, 2N2369A	352-0596-030	
Q2, Q3	TRANSISTOR, 2N2484	352-0549-000	
R1, R2	RESISTOR, FXD, CMPSN, 47kΩ, 10%, 1/8W	745-2401-000	
R3	RESISTOR, FXD, FILM, 10kΩ, 1%, 1/8W	705-1044-000	
R4	RESISTOR, FXD, FILM, 5.62kΩ, 1%, 1/8W	705-1032-000	
R5	NOT USED		
R6	RESISTOR, FXD, FILM, 5.36kΩ, 1%, 1/8W	705-1031-000	
R7	RESISTOR, FXD, FILM, 1.78kΩ, 1%, 1/8W	705-1008-000	
R8	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/8W	745-2365-000	
R9	RESISTOR, FXD, FILM, 1.78kΩ, 1%, 1/8W	705-1008-000	
R10, R11	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/8W	745-0749-000	
U1	INTEGRATED CKT, 11C90DC	351-1653-020	
U2, U3	INTEGRATED CKT, SN74LS190N	351-1527-040	
U4	INTEGRATED CKT, N74LS09N	351-1523-210	
U5, U6	INTEGRATED CKT, SN74LS74N	351-1525-040	
U7	INTEGRATED CKT, N74LS00N	351-1523-110	
U8	INTEGRATED CKT, SN74LS74N	351-1525-040	
U9	INTEGRATED CKT, F4050BPC	351-8159-220	

MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Removed A3A1R9, 100Ω from in series with A3A1Q2-E and junction of A3A1R10-A3A1C12. Changed A3A1 C12 from 0.01μF to 470pF.	635-0846-001, REV B and above.
A2	Changed: A1A1R12 from 680u to 560u. A1A1R10 from 100u to test select of 100u to 390u.	635-0890-002, REV A and above.
A3	Added A1A1R15, test select of 100u or 150u.	635-0890-002, REV C and above.
A4	Removed A1A1L5, 1μH and A1A1R15, test select of 100u or 150u from circuit as shown below.	635-0890-002, REV E and above.

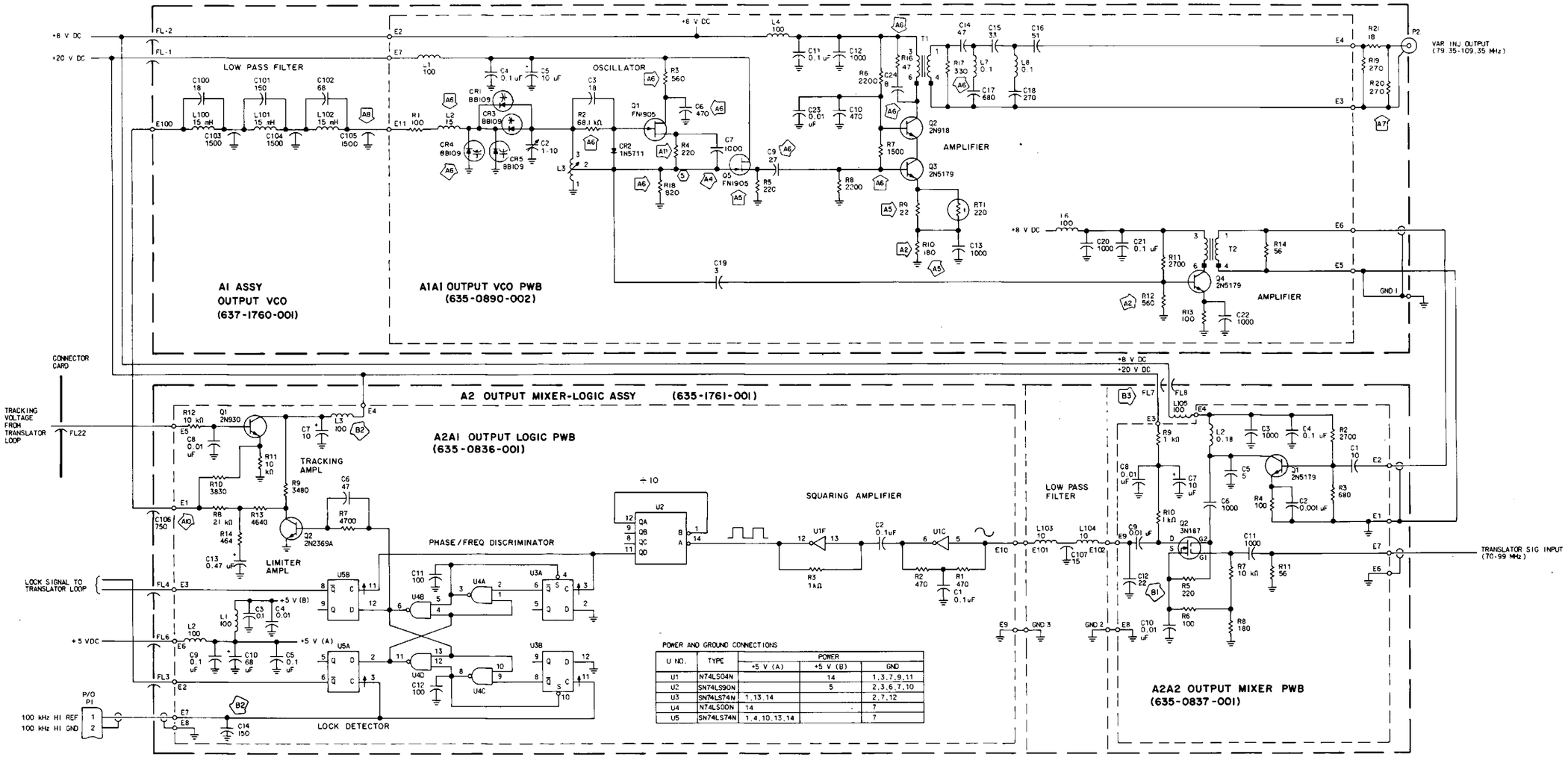


A5	Added A1A1 Q5, FN1905 Changed: A1A1R9 from 68Ω to 22Ω A1A1R10 from test select of 100Ω to 390Ω; to 180Ω fixed. A1A1T1 changed from 278-0430-200 to 278-0430-290.	635-0890-002, REV E and above.
A6	Removed A1A1C1, 1000pF from A1A1CR1 cathode to ground. Removed A1A1C8, 15pF from A1A1Q3-B to ground. Changed: A1A1C6 from 1000pF to 470pF A1A1C9 from 1000pF to 27pF A1A1L2 from 2.7μH to 15μH A1A1R2 from 30.1ku to 68.1ku A1A1R3 from 1ku to 560u. Added A1A1CR3, BB109 Added A1A1CR4, BB109 Added A1A1CR5 BB109 Added A1A1C24, 8pF Added A1A1R16, 47u Added A1A1R17, 330u Added A1A1R18, 820u	635-0890-002, REV F and above.
A7	Added A1R19, 270u Added A1R20, 270u Added A1R21, 18u	635-1760-001, REV D and above.
A8	Changed A1C105 from 750pF to 1500pF.	637-1760-001, REV E and above.
A9	Changed A3L110 from 10mH to 9.3mH	637-1763-001, REV D and above.
A10	Changed A2A1R8 from 33.2ku to 21ku.	635-0836-001, REV B and above.
A11	Changed A1A1R4 from 1ku variable to; test select of 150u to 560u.	635-0890-002 REV G and above.
B1	Added A2A2C12, 22pF.	635-0837-001 REV B and above.
B2	Added A2A1C14, 150pF. Changed A2A1L3 from 4.7uH to 100μH.	635-0836-001 REV C and above.
B3	Added A2L105, 100μH.	637-1761-001 REV E and above.

MODIFICATION HISTORY (Cont)

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
B4	Added A3C116, 33pF.	637-1763-001 REV F and above.

Synthesizer Output, Schematic Diagram
Figure 9 (Sheet 3A)



POWER AND GROUND CONNECTIONS

U NO.	TYPE	POWER		
		+5 V (A)	+5 V (B)	GND
U1	N74LS04N		14	1,3,7,9,11
U2	SN74LS90N		5	2,3,6,7,10
U3	SN74LS74N	1,13,14		2,7,12
U4	N74LS00N	14		7
U5	SN74LS74N	1,4,10,13,14		7

Synthesizer Output, Schematic Diagram
Figure 9 (Sheet 4)

TS-8010 Card Extender Kit (622-3431-001, -002)

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

523-0767968-002211
2nd Edition, 1 June 1978

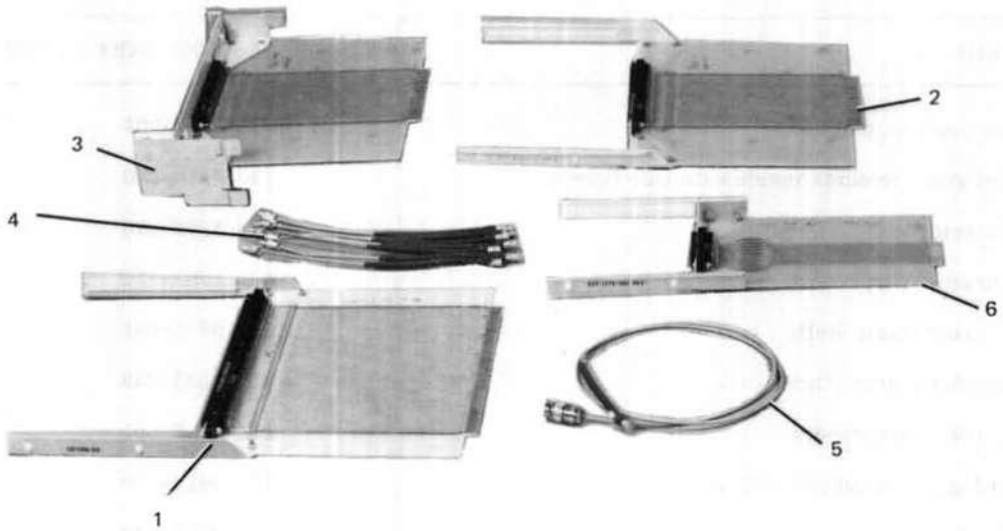
1. DESCRIPTION

The TS-8010 Card Extender Kit 622-3431-001, -002 contains all cables and extender cards necessary for extending cards and modules in the HF-80 series receivers, exciters, and controls. These extenders enable testing and troubleshooting of individual circuit cards in hot mockup or in on-line situations without the need of sophisticated test fixtures or test equipment.

The TS-8010 622-3431-001 contains all cables and extenders necessary for testing and troubleshooting the HF-8010/8010A Exciter, HF-8050/8050A Receiver, HF-8070/8070A Receiver-Exciter, and HF-8090/8091/8092 controls.

The TS-8010 622-3431-002 contains only those extenders necessary for testing and troubleshooting the HF-8090 Exciter Control, HF-8091 Receiver Control, and HF-8092 Receiver-Exciter Control.

Refer to figure 1 and table 1 for the complement of these card extender kits.



TP5-4916-017

TS-8010 Card Extender Kit
Figure 1

NOTICE: This section replaces first edition dated 1 June 1978.

Table 1. TS-8010 Card Extender Kit Complement.

ITEM NO	COLLINS PART NUMBER	DESCRIPTION	622-3431-	
			001	002
1	635-0913-001	130-pin edge-on extender	X	X
2	635-0915-001	56-pin edge-on extender	X	X
3	635-0915-002	Rf module extender	X	
4	635-9686-001	Subminiax coax extender	7	
5	635-9686-002	Subminiax coax/BNC extender	X	
6	637-2843-001	Synthesizer extender	X	

2. REPAIR

Repair of the TS-8010 Card Extender Kit is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

3. PARTS LIST/DIAGRAMS

This paragraph assists in identification, requisition, and issuance of parts, and in maintenance of the equipment. The Collins part number and description for each nonstandard replacement part are listed in table 2.

All pins and shields of the extenders are one-to-one connections; therefore a schematic diagram of the extenders is not shown.

Table 2. TS-8010 Card Extender Kit Parts List.

DESCRIPTION	COLLINS PART NUMBER
130-pin edge-on extender	635-0913-001
Card guide (mounts inside extender frames)	150-0810-040
Connector	372-2274-060
Printed wiring board	600-1993-770
Extender frame (left)	635-9683-001
Extender frame (right)	635-9683-002
56-pin edge-on extender	635-0915-001
Card guide (mounts inside extender frames)	150-0810-040
Connector	372-7515-040
Printed wiring board	600-1993-771
Extender frame (left)	635-9685-001
Extender frame (right)	635-9685-002

Table 2. TS-8010 Card Extender Kit Parts List (Cont).

DESCRIPTION	COLLINS PART NUMBER
Rf module extender	635-0915-002
Connector	372-7515-040
Printed wiring board	600-1993-771
Extender frame	635-9681-001
Subminiax coax extender	635-9686-001
Rf connector	357-7207-010
Rf connector	357-7207-020
Coaxial cable, RG-316/U	425-0146-010
Subminiax coax/BNC extender	635-9686-002
Rf connector	357-7207-010
Rf connector, BNC	357-7279-010
Coaxial cable, RG-316/U	425-0146-010
Synthesizer extender	637-2843-001
Card guide (mounts inside extender brackets)	150-0810-030
Connector	372-7515-050
Printed wiring board	600-1993-050
Extender bracket (left)	637-1775-001
Extender bracket (right)	637-1776-001

AC-8012 Oven Standard Kit (622-3460-001)

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

523-0768671-001211
1 June 1978

1. DESCRIPTION

AC-8012 Oven Standard Kit 622-3460-001 contains an rf oscillator, an external phase-lock card, and all the cables and hardware necessary to install them in the units listed in table 1. When installed, the oven standard provides a high-stability crystal oscillator mounted inside a proportionally controlled oven.

Table 1. AC-8012 Oven Standard Kit, Equipment Used On.

EQUIPMENT	COLLINS PART NUMBER
HF-8010 Exciter	622-3389-( )
HF-8010A Exciter	622-3395-( )
HF-8050 Receiver	622-3385-( )
HF-8050A Receiver	622-3393-( )
HF-8070 Receiver-Exciter	622-3387-( )
HF-8070A Receiver-Exciter	622-3394-( )
851S-1 Receiver	622-4272-( )

Note

This kit is factory installed on some configurations of these units.

The AC-8012 rf oscillator provides a 1-MHz sine-wave frequency output at a level of 0.40 volt rms into 50 ohms. Accuracy of the rf oscillator exceeds that of the tcxo built into the used-on equipments and uses a proportionally controlled oven instead of the temperature-compensating network to improve accuracy over the controlled temperature range, -20 to +70 °C (-4 to +158 °F).

The AC-8012 rf oscillator has two frequency adjustments: a coarse adjustment (FREQ ADJ - COARSE) to adjust the output frequency to $\pm 1.5 \times 10^{-6}$ of the nominal frequency with $\pm 5 \times 10^{-9}$ or better resolution, and a fine adjustment (FREQ ADJ - FINE) to adjust the output frequency to 2.0×10^{-8} minimum to 4.0×10^{-8} maximum with minimum resolution of $\pm 2 \times 10^{-10}$.

The AC-8012 rf oscillator requires +18.0 ±0.9 V dc, 8.0 watts maximum during warmup; 2.5 watts nominal after warmup; and +5.0 ±0.25 V dc, 20 mA maximum.

2. INSTALLATION (Refer to figure 1.)

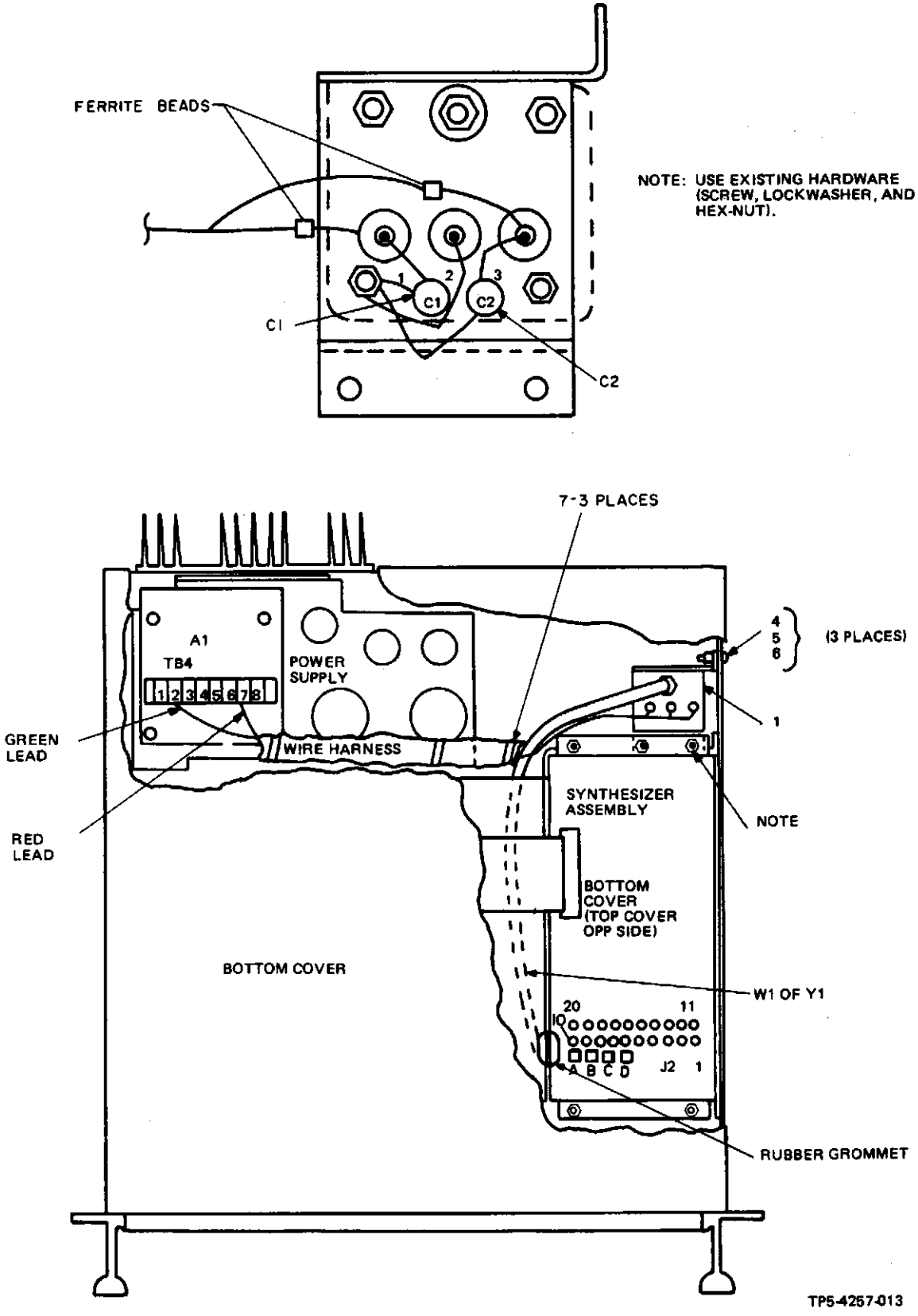
Installation of AC-8012 Oven Standard Kit (622-3460-001) consists of installation of external phase-lock on the synthesizer reference (REF STD) and installation of oscillator assembly Y1 (637-9135-001).

Note

Refer to maintenance section of this instruction book for planar card component replacement procedures.

2.1 External Phase-Lock (635-0655-001) Installation

a. Remove top cover from unit.
b. Remove top cover from synthesizer assembly.
c. Remove REF STD from synthesizer assembly.
d. Remove cover from left side rf compartment on REF STD, and move jumper clip from INT to EXT position (strap for external operation).



AC-8012 Oven Standard Kit Installation
Figure 1

e. Reinstall left side rf compartment cover on REF STD.
f. Mount external phase-lock (table 2, item 2) to REF STD with two lockscrews (table 2, item 3).
g. Set jumper clip on external phase-lock to 1-MHz position.
h. Insert REF STD in its original position in synthesizer assembly.
i. Reinstall synthesizer assembly top cover.
j. Reinstall unit top cover.

2.2 Oscillator Assembly (637-9135-001) Installation

a. Remove bottom cover from unit.
b. Remove attaching hardware referred to in note on figure 1.
c. Install oscillator assembly (table 2, item 1) to chassis using three screws (table 2, item 4), three lockwashers (table 2, item 5), three hexnuts (table 2, item 6), and attaching hardware removed in step b above.
d. Install the two wires from oscillator assembly (table 2, item 1) to power supply A1 (green wire to A1TB4-2 and red wire to A1TB4-7).
e. Using three cable ties (table 2, item 7), tie the two wires that connect the oscillator assembly to power supply A1.
f. Remove bottom cover of synthesizer assembly and install oscillator assembly cable W1 (table 2, P/O item 1) to synthesizer sideboard as follows:
   1. Thread cable W1 through rubber grommet as shown in figure 1.

Note

Some configurations of the synthesizer assembly do not contain a rubber grommet. In configurations not having a rubber grommet, place W1 in one of the cutouts for wiring, using care not to pinch wires when reinstalling synthesizer assembly bottom cover.

Note

Some configurations of the synthesizer sideboard contain posts on the J2 pad and some only contain solder holes. In the configurations containing solder holes, do not insert leads more than 0.508 cm (0.20 in) into sideboard when soldering.

   2. Solder center conductor of W1 (insulated) to J2-A post or pad of synthesizer sideboard.
   3. Solder shield top of W1 (uninsulated) to J2-B post or pad of synthesizer sideboard.
g. Reinstall synthesizer assembly bottom cover.
h. Reinstall unit bottom cover.

3. REPAIR

Repair of the AC-8012 Oven Standard Kit is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

Table 2. AC-8012 Oven Standard Kit Parts List.

ITEM	DESCRIPTION	COLLINS PART NUMBER	QUANTITY
1	Oscillator assembly	637-9135-001	1
	Radio frequency oscillator	277-0472-010	1
	Capacitor, 0.1 μF	913-3681-000	2
	Ferrite bead	288-0915-030	2
2	External phase-lock	635-0655-001	1
3	Lockscrew - 0.112 x 40 x 0.187	330-1716-130	2
4	Machined screw - 0.138 x 32 x 0.375	343-0169-000	3
5	Lockwasher - 0.138	310-0096-000	3
6	Hexnut - 0.138 x 32	313-0045-000	3
7	Cable tie	435-1169-200	3
8	Drawing envelope	520-8360-132	1
	Installation kit, oven oscillator -- AC-8012	622-3460-001	1

4. PARTS LIST/DIAGRAMS

This paragraph assists in identification, requisition, and issuance of parts, and in installation/maintenance of the equipment. The Collins part number and description of each nonstandard replacement part are listed in table 2.

Radio Frequency Oscillator 277-0472-010 is a nonrepairable assembly and should be returned to factory if defective.

External Phase-Lock 635-0655-001 is repairable and is covered in Synthesizer Reference (623-2085-001) instructions (Collins part number 523-0767970) included in this instruction book.

AC-8013 External Standard Kit (622-3461-001)

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

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1 June 1978

1. DESCRIPTION

The AC-8013 External Standard Kit 622-3461-001 contains an external phase-lock card, a cable assembly, and the hardware necessary to install them in the units listed in table 1. When installed, the external standard kit allows for an external high-stability frequency source to be connected to the synthesizer reference.

The external phase-lock card (P/O AC-8013 kit), when installed, allows an external reference frequency of 5 MHz, 1 MHz, or 100 kHz to be supplied to the units listed. The external reference signal must be 0.5 to 1.5 volts rms sine wave into 50 ohms with accuracy depending on the accuracy of the signal source.

2. INSTALLATION (Refer to figure 1.)

Installation of AC-8013 External Standard Kit (622-3461-001), consists of installation of external phase-lock on the synthesizer reference (REF STD) and installation of cable assembly W1 (637-9136-001).

Note

Refer to maintenance section of this instruction book for planar card component replacement procedures.

2.1 External Phase-Lock (635-0655-001) Installation

a. Remove top cover from unit.
b. Remove top cover from synthesizer assembly.
c. Remove REF STD from synthesizer assembly.

Table 1. AC-8013 External Standard Kit, Equipment Used On.

EQUIPMENT	COLLINS PART NUMBER
HF-8010 Exciter	622-3389-( )
HF-8010A Exciter	622-3395-( )
HF-8050 Receiver	622-3385-( )
HF-8050A Receiver	622-3393-( )
HF-8070 Receiver-Exciter	622-3387-( )
HF-8070A Receiver-Exciter	622-3394-( )
851S-1 Receiver	622-4272-( )

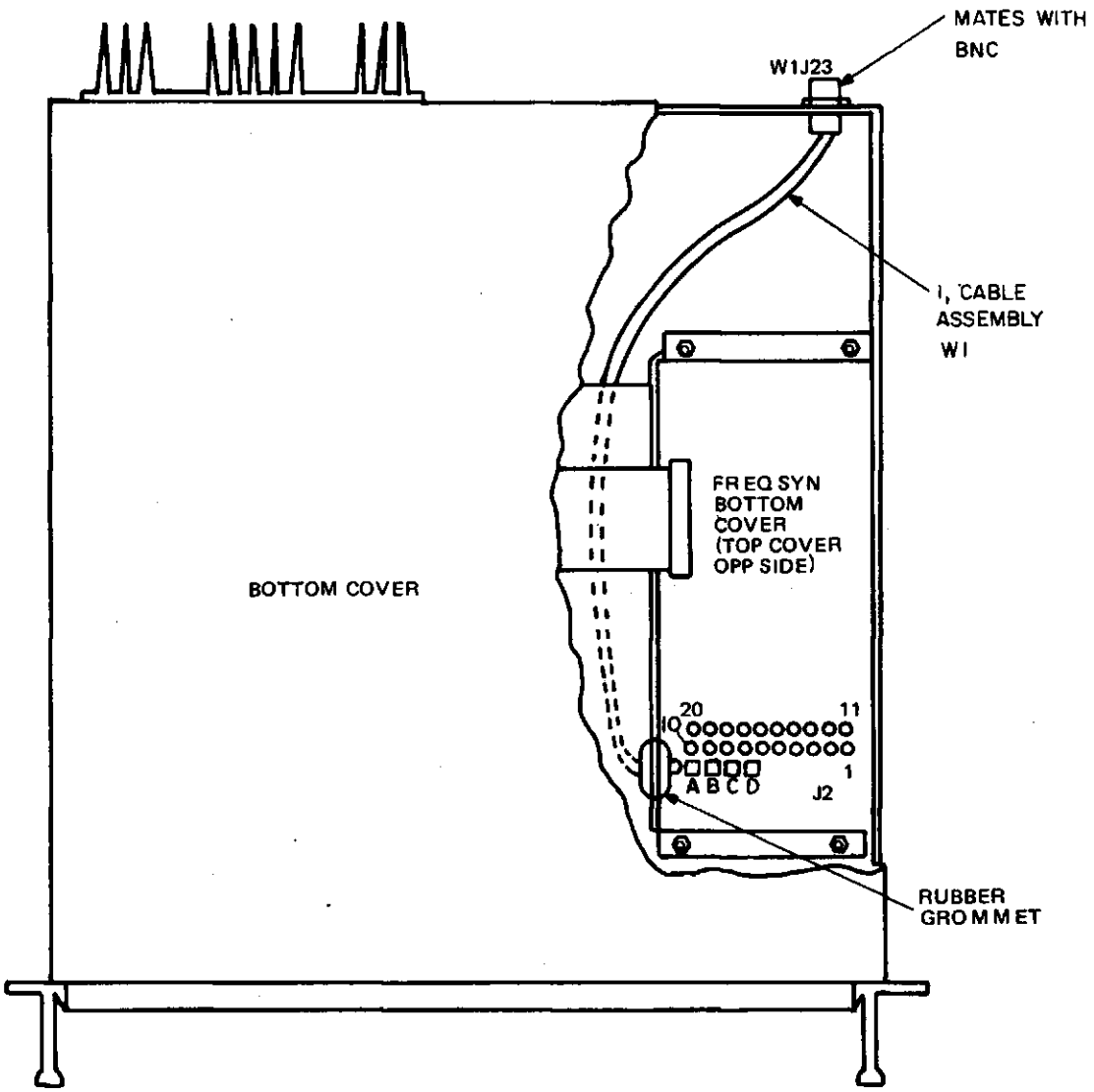
Note

If an oven standard kit is installed, the oven standard must first be removed before the external standard kit is installed.

d. Remove cover from left side rf compartment on REF STD, and move jumper clip from INT to EXT position (strap for external operation).
e. Reinstall left side rf compartment cover on REF STD.
f. Mount external phase-lock (table 2, item 2) to REF STD with two lockscrews (table 2, item 3).
g. Set jumper clip on external phase-lock to 1-MHz position.
h. Insert REF STD in its original position in synthesizer assembly.
i. Reinstall synthesizer assembly top cover.
j. Reinstall unit top cover.

2.2 Cable Assembly W1 (637-9136-001) Installation

a. Remove bottom cover from unit.
b. Remove bottom cover from synthesizer assembly.



TP5-4258-013

AC-8013 External Standard Kit Installation
Figure 1

c. Secure cable assembly W1 (table 2, item 1) to J23 position of rear panel and thread cable through rubber grommet to synthesizer assembly as shown in figure 1.

Note

Some configurations of the synthesizer assembly do not contain a rubber grommet. In configurations not having a rubber grommet, place W1 in one of the cutouts for wiring using care not to pinch wires when reinstalling synthesizer assembly bottom cover.

Some configurations of the synthesizer sideboard contain posts in the J2 pads and some only contain solder holes. In the configurations containing solder holes, do not insert leads more than 0.508 cm (0.20 in) into sideboard when soldering.

d. Solder center conductor of W1 (insulated) to J2-A post or pad of synthesizer sideboard.

e. Solder shield top of W1 (uninsulated) to J2-B post or pad of synthesizer sideboard.

f. Reinstall synthesizer assembly bottom cover.

g. Reinstall unit bottom cover.

3. REPAIR

Repair of the AC-8013 External Standard Kit is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

4. PARTS LIST/DIAGRAMS

This paragraph assists in identification, requisition, and issuance of parts, and installation/maintenance of the equipment. The Collins part number and description for each nonstandard replacement part are listed in table 2.

External Phase-Lock 635-0655-001 is covered in Synthesizer Reference (623-3085-001) instructions (Collins part number 523-0767970) included in this instruction book.

Table 2. AC-8013 External Standard Kit, Parts List.

ITEM	DESCRIPTION	COLLINS PART NUMBER	QUANTITY
1	Cable assembly W1	637-9136-001	1
2	External phase-lock	635-0655-001	1
3	Lockscrew - 0.112 x 40 x 0.187	330-1716-130	2
4	Drawing envelope	520-8360-133	1
	Installation kit-external reference standard, AC-8013	622-3461-001	1

AC-8090
Remote Control Kit
(622-3462-001)

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

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2nd Edition, 1 January 1979

1. DESCRIPTION

AC-8090 Remote Control Kit 622-3462-001 contains a parallel output, parallel input, and serial interface card. When installed, the AC-8090 Remote Control Kit makes the equipment it is used on (table 1) completely remotable using a compatible remote control.

Table 1. AC-8090 Remote Control Kit, Equipment Used On.

EQUIPMENT	COLLINS PART NUMBER
HF-8010 Exciter	622-3389-( )
HF-8050 Receiver	622-3385-( )
HF-8070 Receiver-Exciter	622-3387-( )
*851S-1 Receiver	622-4272-( )
*This kit is factory installed on some configurations of this unit.	

2. INSTALLATION

Install AC-8090 Remote Control Kit 622-3462-001 as follows:

a. Remove the unit top cover.
b. Install the cards included in the kit in the following slots:
   1. Parallel input in A11 slot.
   2. Parallel output in A12 slot.
   3. Serial interface in A13 slot.
c. Reinstall the unit top cover.

3. REPAIR

Repair of the AC-8090 Remote Control Kit is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

4. PARTS LIST/DIAGRAMS

This paragraph assists in identification, requisition, and issuance of parts, and in maintenance of the equipment. The Collins part number and description for each replacement part are listed in table 2.

These cards are covered in the following instructions which are included in this instruction book.

a. Parallel input (635-0751-001, -002) instructions (Collins part number 523-0767949).
b. Parallel output (635-0752-001, -002) instructions (Collins part number 523-0767950).
c. Serial interface (635-0742-001) instructions (Collins part number 523-0767951).

NOTICE: This section replaces first edition dated 1 June 1978.

Table 2. AC-8090 Remote Control Kit Parts List.

PART DESCRIPTION	COLLINS PART NUMBER	QUANTITY USED ON
		AC-8090 REMOTE CONTROL KIT 622-3462-001
Serial interface A13	635-0742-001	1
Parallel input A11	635-0751-001	1 REV-
Parallel input A11	635-0751-002	1 REV A and above
Parallel output A12	635-0752-001	1 REV-
Parallel output A12	635-0752-002	1 REV A and above
Drawing envelope	520-8360-215	1
Installation Kit - Remote Control AC-8090	622-3462-( )	1

AC-85100 ISB Kit (622-4606-( ))

Rockwell International

instructions

Collins Telecommunications Products Division

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1 January 1979

1. DESCRIPTION

The AC-85100 ISB Kit 622-4606-( ) contains a channel B if. When installed, the ISB Kit provides LSB and 2-channel ISB (independent sideband) operation. Refer to table 1 for equipments used on.

The AC-85100 channel B if provides a channel B if amplifier and channel B SSB product detected audio outputs. Different configurations of the AC-85100 ISB provide different LSB bandwidth filters.

To maintain a balanced ISB operation, an LSB filter with the same bandwidth as the USB filter is desired. The standard filter in USB is 2.75-kHz bandwidth, thus a 2.75-kHz bandwidth LSB filter should be used. If a filter other than the standard is used in either USB or LSB, kits are available to maintain a balanced ISB system. LSB filters are included in these instructions; USB filters are included in AC-85108 Channel A IF Kit (622-4616-( )) instructions.

Table 1. AC-85100 ISB Kit, Equipments, Used On.

EQUIPMENT	COLLINS PART NO
851S-1 Receiver	622-4272-( )
This kit is factory installed on some configurations of this unit.	

2. INSTALLATION

Installation of the AC-85100 ISB Kit 622-4606-( ) consists of installing a channel B if A8 and, if installed, removing filter A8A2FL2 from filter card A8A2.

a. Remove top cover from unit.
b. If A8A2 installed, remove A8 CHAN A IF from the unit.
c. Remove A8A2 filter card from A8 CHAN A IF.
d. If A8A2FL2 is not the only filter on the A8A2 filter card, unsolder and remove A8A2FL2 from the A8A2 filter card.
e. Replace A8A2 filter card on A8 CHAN A IF. (If A8A2FL2 is the only filter on the A8A2 filter card, save the removed card. Do not reinstall it in the unit.)
f. Reinstall A8 CHAN A IF in its original position in the unit.
g. Install A7 CHAN B IF in its allocated position in the unit.
h. Reinstall unit top cover.

3. REPAIR

Repair of the AC-85100 ISB Kit is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

4. PARTS LIST/DIAGRAMS

This paragraph assists in identification, requisition, and issuance of parts, and in maintenance of the equipment. The Collins part number and description for each replacement part are listed in table 2.

Channel B IF 637-2647-( ) is covered in Channel B IF 637-2647-( ) instructions (Collins part number 523-0767965) included in this instruction book.

Table 2. AC-85100 ISB Kit, Parts List.

PART DESCRIPTION	COLLINS PART NO	QUANTITY USED ON AC-85100 ISB KIT 622-4606-( )		
		-001	-002	
Channel B if (2.75-kHz LSB)	637-2647-001	1		
Channel B if (3.10-kHz LSB)	637-2647-003		1	
Drawing envelope	520-8360-216	1	1	
Installation Kit - ISB AC-85100	622-4606-( )	1	1	

AC-85101 DVBFO Kit (622-4607-001)

Rockwell International

instructions

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1. DESCRIPTION

The AC-85101 DVBFO Kit 622-4607-001 contains a vbfo card. When installed the DVBFO kit provides a vbfo offset frequency for SSB/CW or ISB (channel A only) operation. Refer to table 1 for equipment this kit is used on.

The AC-85101 vbfo provides an offset frequency that is summed with the 450-kHz injection frequency and provides a 440.01- to 459.99-kHz channel A if injection frequency when the bfo is enabled. This variable injection frequency provides a CW tone of 0 to 9 990 Hz (in 10-Hz steps) in either USB or LSB.

2. INSTALLATION

Installation of the AC-85101 DVBFO Kit 622-4607-001 consists of installing an A4 VBFO card and removing optical blanker from VBFO display.

2.1 VBFO 638-6067-001 Installation

Note

Retain hardware removed during disassembly for use in reassembly. Refer to unit parts list as an aid in disassembly and assembly.

a. Remove top cover from unit.
b. Remove jumper card 637-3796-001 from A4 slot.
c. Install VBFO 638-6067-001 in A4 slot.
d. Remove front panel from unit by removing four hexhead screws and attaching hardware.

Table 1. AC-85101 DVBFO Kit, Equipment Used On.

EQUIPMENT	COLLINS PART NO
851S-1 Receiver	622-4272-( )
This kit is factory installaed on some configurations of this unit.	

Caution

Upper overlay panel (plexiglass) is brittle; exercise care during removal of upper overlay panel.

e. Remove upper overlay panel from front panel as follows:
   1. Remove four Phillips-head screws and lockwashers that secure back of front panel to upper edge bar.
   2. Remove four Phillips-head screws and lockwashers that secure back of front panel to panel support (middle bar on front panel).
   3. Lift upper edge bar from front panel.
   4. Carefully remove upper overlay panel.
f. Carefully remove optical blanker from vbfo frequency display.

Caution

Upper overlay panel (plexiglass) is brittle; exercise care during replacement of upper overlay panel.

g. Insert upper overlay panel into slot on panel support (middle bar on front panel).
h. Replace edge bar on top of front panel ensuring upper overlay panel fits properly.
i. Secure upper overlay panel to front panel with eight Phillips-head screws and lockwashers.
j. Secure front panel to unit with four hexhead screws and attaching hardware.
k. Reinstall unit top cover.

3. REPAIR

Repair of AC-85101 DVBFO Kit is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

4. PARTS LIST/DIAGRAMS

This paragraph assists in the identification, requisition, and issuance of parts, and in maintenance of the equipment. The Collins part number and description for each nonstandard replacement part are listed in table 2. These cards are covered in the following instructions which are included in this instruction book.

Table 2. AC-85101 DVBFO Kit, Parts List.

PART DESCRIPTION	COLLINS PART NO	QUANTITY USED ON AC-85101 DVBFO KIT 622-4607-001
VBFO A4	638-6067-001	1
Drawing envelope	520-8360-211	1
Installation Kit - DVBFO AC-85101	622-4607-( )	1

AC-85102
Decade Expansion Kit
(622-4608-001)

Rockwell International

instructions

Collins Telecommunications Products Division

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523-0769224-001211
1 January 1979

1. DESCRIPTION

The AC-85102 Decade Expansion Kit 622-4608-001 contains a synthesizer 100/10 Hz decade card. When installed, the AC-85102 Decade Expansion Kit provides 10-Hz tuning on all units listed in table 1.

Table 1. AC-85102 Decade Expansion Kit, Equipment Used On.

EQUIPMENT	COLLINS PART NO
851S-1 Receiver	622-4272-001

2. INSTALLATION

Installation of the AC-85102 Decade Expansion Kit 622-4608-001 consists of configuring the synthesizer assembly for 10-Hz operation using the 100/10-Hz decade supplied with the kit.

Note

Retain hardware removed during disassembly for use in reassembly. Refer to unit parts list as an aid in disassembly and assembly.

a. Remove unit top cover.
b. Remove synthesizer assembly top cover.
c. Remove END DECADE from A18 slot and install it in A17 slot.
d. Install decade card 623-2080-004 in the A18 slot.
e. Remove front panel from unit by removing four hexhead screws and attaching hardware.

Caution

Upper overlay panel (plexiglass) is brittle; exercise care during removal of upper overlay panel.

f. Remove upper overlay panel from front panel as follows:
   1. Remove four Phillips-head screws and lockwashers that secure back of front panel to upper edge bar.
   2. Remove four Phillips-head screws and lockwashers that secure back of front panel to panel support (middle bar on front panel).
   3. Lift upper edge bar from front panel.
   4. Carefully remove upper overlay panel.
g. Carefully remove optical blanker from 10-Hz frequency digit of frequency display.

Caution

Upper overlay panel (plexiglass) is brittle; exercise care during replacement of upper overlay panel.

h. Insert upper overlay panel into slot on panel support (middle bar on front panel).
i. Replace edge bar on top of front panel ensuring upper overlay panel fits properly.
j. Secure upper overlay panel to front panel with eight Phillips-head screws and lockwashers.
k. Secure front panel to unit with four hexhead screws and attaching hardware.

l. Reinstall synthesizer assembly top cover.
m. Reinstall unit top cover.

3. REPAIR

Repair of AC-85102 Decade Expansion Kit is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

4. PARTS LIST/ DIAGRAMS

This paragraph assists in identification, requisition, and issuance of parts, and in maintenance of the equipment. The Collins part number and description for each replacement part are listed in table 2.

Synthesizer Decade 623-2080-004 is covered in Synthesizer Decade 623-2080-001, -002, -003, -004 instructions (Collins part number 523-0767972) included in this instruction book.

Table 2. AC-85102 Decade Expansion Kit, Parts List.

PART DESCRIPTION	COLLINS PART NO	QUANTITY USED ON AC-85102 DECADE EXPANSION KIT 622-4608-001
Synthesizer decade	623-2080-004	1
Drawing envelope	520-8360-212	1
Installation Kit-Decade Expansion AC-85102	622-4608-( )	1

AC-85105
Optional Filters Kit
(622-4611-( ))

Rockwell International

instructions

Collins Telecommunications Products Division

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523-0769226-001211
1 January 1979

1. DESCRIPTION

AC-85105 Optional Filters Kit 622-4611-( ) contains an if filter card and two sets of decals to mark the front-panel BANDWIDTH switch. When installed, the AC-85105 Optional Filters Kit allows selection of filters using the front-panel MODE switch and BANDWIDTH switch. Normally selection of specific filters is made in SSB/CW or AM modes. The if filter card is installed in the local unit and one set of decals is used to appropriately mark the front-panel BANDWIDTH switch of the local unit. The second set of decals is used to mark the front-panel BANDWIDTH switch on the associated control unit (if applicable). Refer to table 1 for equipment this kit is used on.

2. INSTALLATION

Installation of AC-85105 Optional Filters Kit 622-4611-( ) consists of installing an if filter card and front-panel decals.

Table 1. AC-85105 Optional Filters Kit, Equipment Used On.

EQUIPMENT	COLLINS PART NUMBER
*851S-1 Receiver **HF-8095 Receiver Control	622-4272-( ) 622-3489-( )

*This kit is factory installed on some configurations of this unit.
**Control, associated only with 851S-1 Receiver with remote control or 851S-1 Receiver with AC-8090 Remote Control Kit installed.

2.1 Filter 637-2515-( ) Installation

a. Remove top cover from unit.
b. Remove A8 CHAN A IF from the unit.
c. Plug filter into A8 CHAN A IF.
d. Secure filter in place using screw and washers supplied in this kit.
e. Insert A8 CHAN A IF in its original position in unit.
f. Reinstall unit top cover.

2.2 Decal Installation

Note

Extra decals in kit to be installed on associated control unit (if applicable).

Install adhesive-backed decals in front-panel recess at BANDWIDTH switch positions as shown in table 2.

Table 2. Decal Installation.

BANDWIDTH SWITCH POSITION	DECALS INSTALLED			
	KIT 622-4611-( )			
	-001	-002	-003	-004
A	-	6	6	6
B	-	3	3	3
C	-	1	1	1
D	-	0.5	0.5	0.5
E	-	0.2	0.2	0.1

3. REPAIR

Repair of the AC-85105 Optional Filters Kit is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

4. PARTS LIST/DIAGRAMS

This paragraph assists in identification, requisition, and issuance of parts, and in maintenance of the equipment. The Collins part number and description for each nonstandard replacement part are listed in table 3.

Filter 637-2515-( ) is covered in Filter 637-2515-( ) instructions (Collins part number 523-0767967) included in this instruction book.

Table 3. AC-85105 Optional Filters Kit Parts List.

PART DESCRIPTION	COLLINS PART NUMBER	QUANTITY USED ON AC-85105 OPTIONAL FILTERS KIT 622-4611-( )			
		-001	-002	-003	-004
Filter	637-2515-001		1		
Filter	637-2515-004	1			
Filter	637-2515-005			1	
Filter	637-2515-006				1
Decal, 0.1	635-9700-001				2
Decal, 0.2	635-9700-002		2	2	
Decal, 0.5	635-9700-003		2	2	2
Decal, 1	635-9700-004		2	2	2
Decal, 3	635-9700-005		2	2	2
Decal, 6	635-9700-006		2	2	2
Drawing envelope	520-8360-134	1	1	1	1
Installation Kit-Optional Filters, AC-85105	622-4611-( )	1	1	1	1

AC-85106 RF Translator Kit (622-4612-( ))

Rockwell International

instructions

Collins Telecommunications Products Division

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1. DESCRIPTION

The AC-85106 RF Translator Kit 622-4612-( ) contains a replacement rf module.

When installed, the 622-4612-001 provides 10 1/2-octave bandpass filters for receive filtering and a narrowband 109.35-MHz if filter (±7.50 kHz at 3-dB points).

When installed, the 622-4612-002 provides three broadband rf filters and a broadband 109.35-MHz if filter (±6.10 kHz at 0.5-dB points).

Refer to table 1 for equipment this kit is used on.

Table 1. AC-85106 RF Translator Kit, Equipment Used On.

EQUIPMENT	COLLINS PART NUMBER
HF-8050 Receiver	622-3385-( )
HF-8050A Receiver	622-3393-( )
*851S-1 Receiver	622-4272-( )

*This kit factory installed on some configurations of this unit.

AC-85106 RF Translator Kit (622-4612-001) is not used on (or adaptable to) HF-8050 or HF-8050A Receivers.

2. INSTALLATION

Installation of the AC-85106 RF Translator Kit 622-4612-( ) consists of installing an rf translator A9 and checking that the correct strapping is in place on the control card A10.

a. Remove top cover from unit.
b. Remove A10 CONTROL from unit.
c. Check filter strapping on A10 CONTROL.

Note

If AC-85106 RF Translator Kit 622-4612-001 is being installed (RF Translator 637-3757-001), set strapping for 1/2-Octave filtering. Set four filter straps (from SF) to OF.

Note

If AC-85106 RF Translator Kit 622-4612-002 is being installed (RF Translator 637-1767-002), set strapping for standard filtering. Set four filter straps (from OF) to SF.

d. Reinstall A10 CONTROL in its original position in unit.
e. Remove rf translator A9 from unit.
f. Install new rf translator (637-3757-001 or 637-1767-002) in its allocated position in unit.
g. Reinstall unit top cover.

3. REPAIR

Repair of the AC-85106 1/2-Octave Filter Kit is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

4. PARTS LIST/DIAGRAMS

This paragraph assists in identification, requisition, and issuance of parts, and in installation of the equipment. The Collins part number and description of each nonstandard replacement part are listed in table 2.

The cards in this kit are covered in the following instructions which are included in this instruction book.

a. RF Translator (637-3757-001) instructions (Collins part number 523-0769220).
b. RF Translator (637-1767-001, -002) instructions (Collins part number 523-0767959).

Table 2. AC-85106 RF Translator Kit, Parts List.

PART NUMBER	COLLINS PART NO	QUANTITY USED ON AC-85106 RF TRANSLATOR KIT 622-4612-( )		
		-001	-002	
Rf translator (1/2-octave rf filtering)	637-3757-001	1		
Rf translator (broadband if filtering)	637-1767-002		1	
Drawing envelope	520-8360-214	1	1	
Installation Kit--RF Translator AC-85106	622-4612-( )	1	1	

AC-85108
Channel A IF Kit
(622-4614-( ))

Rockwell International

instructions

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1. DESCRIPTION

The AC-85108 Channel A IF Kit 622-4614-( ) contains a replacement channel A if card.

When installed, the 637-4614-001 provides a 3.10-kHz bandwidth filter for USB 450-kHz receive if filtering.

Refer to table 1 for equipment this kit is used on.

Table 1. AC-85108 Channel A IF Kit, Equipment Used On.

EQUIPMENT	COLLINS PART NUMBER
HF-8050 Receiver	622-3385-( )
HF-8050A Receiver	622-3393-( )
*851S-1 Receiver	622-4272-( )
*This kit factory installed on some configurations of this unit.	

2. INSTALLATION

Installation of the AC-85108 Channel A IF Kit 622-4614-( ) consists of installing a channel A if A8.

a. Remove top cover from unit.
b. Remove A8 CHAN A IF from unit.
c. If filter A8A2 is mounted on A8 CHAN A IF, remove it and mount it to new channel A if.
d. Install new channel A if in its allocated position in unit.
e. Reinstall unit top cover.

3. REPAIR

Repair of the AC-85108 Channel A IF Kit is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

4. PARTS LIST/DIAGRAMS

This paragraph assists in identification, requisition, and issuance of parts, and in installation of the equipment. The Collins part number and description of each nonstandard replacement part are listed in table 2.

Channel A IF 637-2650-( ) is covered in Channel A IF (637-2650-( )) instructions (Collins part number 523-0767962) included in this instruction book.

Table 2. AC-85108 Channel A IF Kit, Parts List.

PART DESCRIPTION	COLLINS PART NO	QUANTITY USED ON AC-85108 CHANNEL A IF KIT 622-4624-( )
		-001
Channel A IF (3.10-kHz filter)	637-2650-003	1
Drawing envelope	520-8360-210	1
Installation Kit-RF Translator AC-85106	622-4624-( )	1