851S-1 Receiver

Rockwell International

theory

Collins Defense Communications

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NOTICE: This section replaces first edition dated 1 January 1979.

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Record of Changes

CHG NO	CHANGE DATE	CHG NO	CHANGE DATE	CHG NO	CHANGE DATE	CHG NO	CHANGE DATE
1st Ed	1 Jan 79						
2nd Ed	1 Mar 81						

1. GENERAL

This section provides functional theory of the 851S-1 Receiver to the circuit card/module level. Theory for individual circuit cards/modules is presented in the applicable circuit card/module section of this instruction book.

The 851S-1 controls and monitors are located on the front panel (refer to figure 1). The local control only 851S-1 does not have a parallel input A11, parallel output A12, serial interface A13. Note also that in the local control only 851S-1 the CONT switch must be kept in the LCL position. The remote controlled 851S-1 is locally or remotely controlled depending on the setting of the CONT switch. When the CONT switch is in the REM position, the 851S-1 is controlled by the HF-8095 Receiver Control, a processor, or other compatible control through REMOTE connector J14 on the rear panel of the 851S-1.

2. FUNCTIONAL THEORY

The 851S-1 frequency is controlled using the DIAL switch and the TUNING knob on the front panel. Rotation of the TUNING knob generates two square-wave pulse trains, clock A (count) and clock B (up/down), whose frequency is proportional to the rotational velocity and whose phase relationship is dependent upon rotational direction (clockwise or counterclockwise) of the TUNING knob. These pulse trains are applied to count/store assembly A2A4 where the pulse frequency (TUNING knob rate) is converted to a 5-bit binary count value representative of the tuning rate, and the phase relationship between the two pulse trains is decoded to provide a logic level signal (up/down) representative of the direction of rotation of the TUNING knob. The 5-bit binary count value and up/down signals are then applied to control A10, where the count value is converted to a clock frequency by a rate decoding PROM and used to clock a bcd up/down counter, whose outputs are applied to the frequency synthesizer (A15 thru A22) and are used to establish the frequency of the vfo output (109.35 to 79.35001 MHz) from the synthesizer. The outputs of the bcd up/down counter on control A10 are also decoded to provide bandswitching output signals for rf translator A9.

The 851S-1 is operating mode controlled directly from the front panel. Mode signals from the front panel are applied directly to receive audio A6, channel A if A8, and in the case of ISB mode to channel B if A7. This controls all mode switching. Placing the MODE switch in SSB/CW or AM position enables the BANDWIDTH switch and allows for an if filter to be selected. The filters selected are 16 kHz in the 16 position, USB in the USB position, LSB in the LSB position; and optional filters are selected in positions A, B, C, D, and E. When the MODE switch is in the ISB position, the USB and LSB filters are selected and the BANDWIDTH switch is disabled.

The 851S-1 receives rf signals at the RCV ANT jack. These signals are supplied to rf translator A9 where they are mixed with the vfo injection signal and a fixed 118.8-MHz injection signal to supply a 9.45-MHz receive if signal to channel A if A8. In the if cards, the signal is mixed with a fixed 9.9-MHz injection signal to produce a final if of 450 kHz. This signal is filtered and detected and the resulting audio signal is supplied to receive audio A6. The receive audio is amplified and supplied to the speaker, phones, and receive audio line outputs. In the ISB mode the LSB signal is supplied to the channel B if A7, which provides separate filtering, amplification, and detection of the LSB signal. The detected LSB audio signal is supplied to the channel B audio amplifier on receive audio A6 and provides separate phones, receive audio line outputs, and a separate audio input to the speaker amplifier.

2.1 Receive Function (Refer to figure 2.)

The receive signals, 250 kHz to 29.999999 MHz, are supplied from an antenna to the rear panel RCV ANT jack. These rf signals are supplied to rf translator A9, through the receive overload circuit, input filter, and peak limiter to the receive rf broadband bandpass filters or receive rf half-octave bandpass filters. The bands and associated selected frequencies are listed below.

Broadband bandpass filters

Band	1	0 to 539 kHz
	2	540 kHz to 1.599 MHz
	3	1.600 to 29.999 MHz

Half-octave bandpass filters

Band 1	0 to 559 kHz
2	560 kHz to 1.599 MHz
3	1.600 to 1.999 MHz
4	2.000 to 2.999 MHz
5	3.000 to 3.999 MHz
6	4.000 to 5.999 MHz
7	6.000 to 7.999 MHz
8	8.000 to 11.999 MHz
9	12.000 to 15.999 MHz
10	16.000 to 23.999 MHz
11	24.000 to 29.999 MHz

From the selected bandpass filter, the received rf signal is mixed with a 109.35000- to 79.35001-MHz variable injection signal to produce a 109.35-MHz if signal. This if is filtered by a crystal filter and mixed with a 118.8-MHz fixed injection signal to produce a 9.45-MHz receive if output from rf translator A9.

The 9.45-MHz receive if is supplied to channel A if A8 where it is mixed with a 9.9-MHz fixed injection frequency to supply a 450-kHz if through the selected if filter to the audio detectors and AGC output amplifiers. The 16- kHz and USB if filters are on channel A if A8. The LSB (ISB) if filter and ISB switching are located on channel B if A7. An optional filter A8A2 is used to provide additional selection of if filters. Spaces for optional bandwidth filters (called A, B, C, D, and E) are available on filter A8A2. If filters A, B, C, D, and E are determined by the requirements of the user.

The channel A 450-kHz if output is supplied to the AM envelope detector and the channel A SSB product detector. The AM af output at J6-8 is supplied to receive audio A6 at J4-35. The channel A SSB af output at J6-34 is supplied to receive audio A6 at J4-34. This channel A (AM or SSB) receive audio is supplied through audio amplifiers as channel A line audio at J4-30, -31, and -32, to TB1-1, -2, and -3; as phones audio at J4-12, to J12-40, to P3-40 and PHONES jack J2; and as speaker audio at J4-9, to J12-13, to P3-13, through SPKR switch and AF GAIN control to P3-30, to J12-30, to J4-45, through speaker amplifier to J4-19, and P12-1 to speaker LS1.

The channel B 450-kHz if output is supplied to the channel B SSB product detector (ISB mode only). The channel B SSB af output at J5-34 is supplied to receive audio A6 at J4-50. This channel B receive audio is supplied through audio amplifiers as channel B line audio at J4-26, -54, and -55 to TB1-4, -5, and -6; as phones audio at J4-12, to J12-40, to P3-40 and PHONES jack J2; and as speaker audio at J4-21, to J12-15, to P3-15 through SPKR switch and AF GAIN control to P3-30, to J12-30, to J4-45, through speaker amplifier to J4-19, and P12-1 to speaker LS1.

2.2 Mode and Operating Controls

The mode and operating controls consist of the front panel switches and an external remote control device, if used. The 851S-1 has a frequency control, speaker control, squelch control, AGC control, local/remote control, af gain control, phones with level adjust, rf gain control, bandwidth control, mode control, and a power switch. The remote controlled 851S-1 can use an external remote control device such as the HF-8095 Receiver Control.

2.2.1 Mode and Bandwidth (Refer to figure 3.)

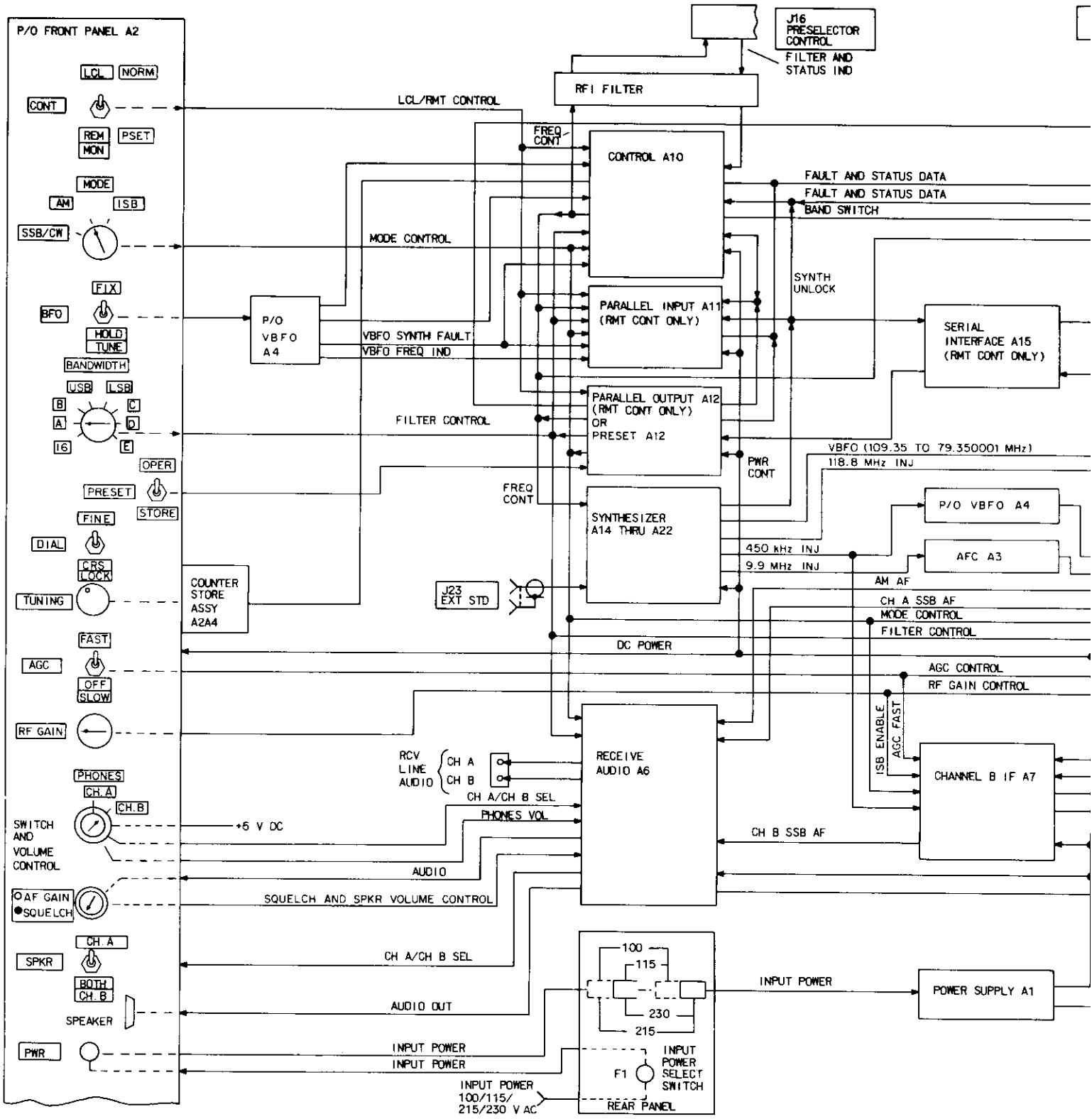
Note that figure 3 covers any optional configuration of the 851S-1 Receiver. However, this discussion is based on the following configured receiver:

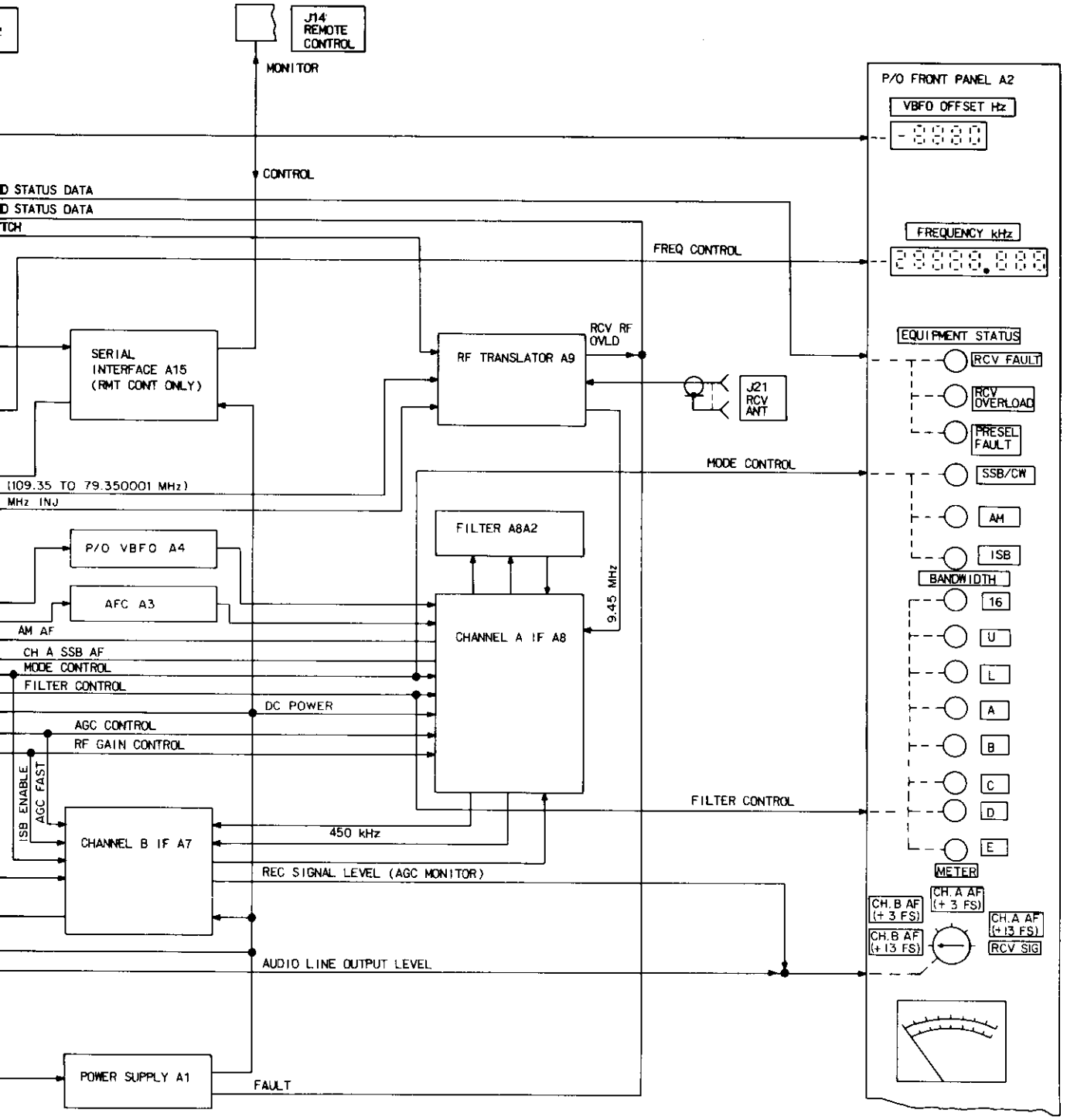
a. A 3-position MODE switch: SSB/CW, AM, and ISB.
b. No automatic USB/LSB bandwidth selection (no strapping diodes.).
c. An 8-position BANDWIDTH switch.
d. Filter A8A2 installed with filters A, B, C, D, and E.
e. Channel B if A7 installed.
f. Strapped at A8P1-46 for FL8.
g. Not strapped at A8P1-15.
h. Not strapped for AM at A8P1-35 between NAND and NOR gate.

When the MODE switch is set to the SSB/CW (USB) mode, an SSB enable signal (+5 V dc) is supplied at P4-6, to P6-14, to J4-36, and enables the SSB audio switch in receive audio A6. The SSB enable signal is also supplied to the BANDWIDTH switch, and the appropriate bandwidth for the desired operation must be selected.

With the BANDWIDTH switch in the 16 position, a 16 (FL8) signal (+5 V dc) is supplied at P3-17, to J12-17, to J6-46, and enables the 16-kHz pad in channel A if A8.

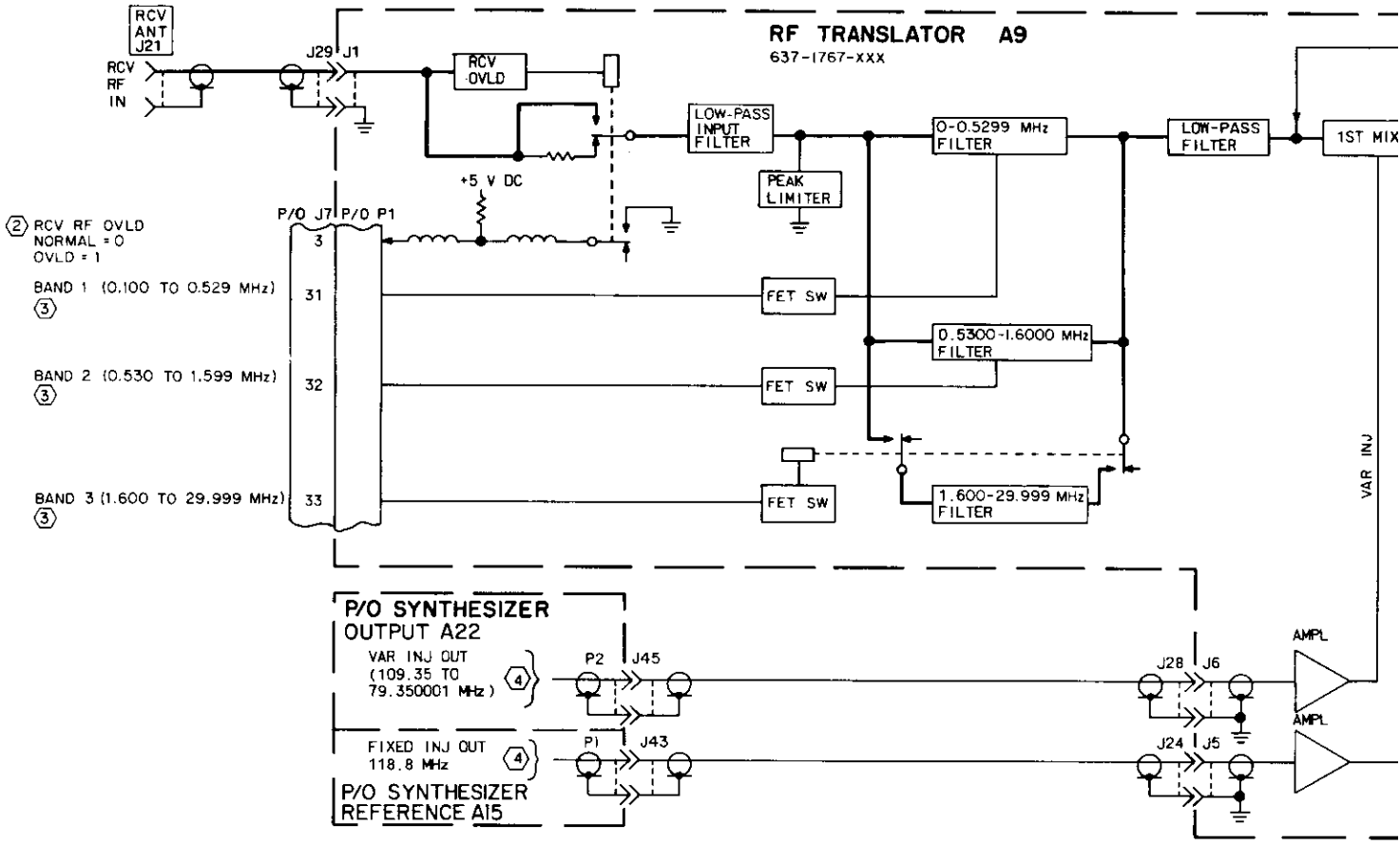
With the BANDWIDTH switch in the A position, an A (FL3) signal (+5 V dc) is supplied at P3-19, to J12-19, to J6-15, to A8A2P10-4, and enables the A filter (optional bandwidth) on filter A8A2.


P/O FRONT PANEL A2
LCL
NORM
CONT
REM
MON
PSET
MODE
AM
ISB
SSB/CW
FIX
BFO
HOLD
TUNE
BANDWIDTH
USB
LSB
B
A
C
D
16
E
OPER
PRESET
STORE
FINE
DIAL
CRS
LOCK
TUNING
FAST
AGC
OFF
SLOW
RF GAIN
PHONES
CH.A
CH.B
SWITCH AND VOLUME CONTROL
AF GAIN
SQUELCH
CH.A
SPKR
BOTH
CH.B
SPEAKER
PWR
LCL/RMT CONTROL
MODE CONTROL
FILTER CONTROL
FREQ CONT
PWR CONT
DC POWER
+6 V DC
AUDIO
SQUELCH AND SPKR VOLUME CONTROL
CH A/CH B SEL
AUDIO OUT
INPUT POWER
INPUT POWER
P/O VBFO A4
VBFO SYNTH FAULT
VBFO FREQ IND
COUNTER STORE ASSY A2A4
J23 EXT STD
J16 PRESELECTOR CONTROL
FILTER AND STATUS IND
RFI FILTER
CONTROL A10
FAULT AND STATUS DATA
FAULT AND STATUS DATA
BAND SWITCH
SYNTH UNLOCK
PARALLEL INPUT A11 (RMT CONT ONLY)
PARALLEL OUTPUT A12 (RMT CONT ONLY) OR PRESET A12
SYNTHESIZER A14 THRU A22
VBFO (109.35 TO 79.350001 MHz)
118.8 MHz INJ
450 kHz INJ
9.9 MHz INJ
AM AF
CH A SSB AF
MODE CONTROL
FILTER CONTROL
AGC CONTROL
RF GAIN CONTROL
ISB ENABLE
AGC FAST
SERIAL INTERFACE A15 (RMT CONT ONLY)
P/O VBFO A4
AFC A3
CHANNEL B IF A7
CH B SSB AF
RCV LINE AUDIO
CH A
CH B
RECEIVE AUDIO A6
100
115
230
215
INPUT POWER SELECT SWITCH
F1
REAR PANEL
INPUT POWER 100/115/ 215/230 V AC
POWER SUPPLY A1

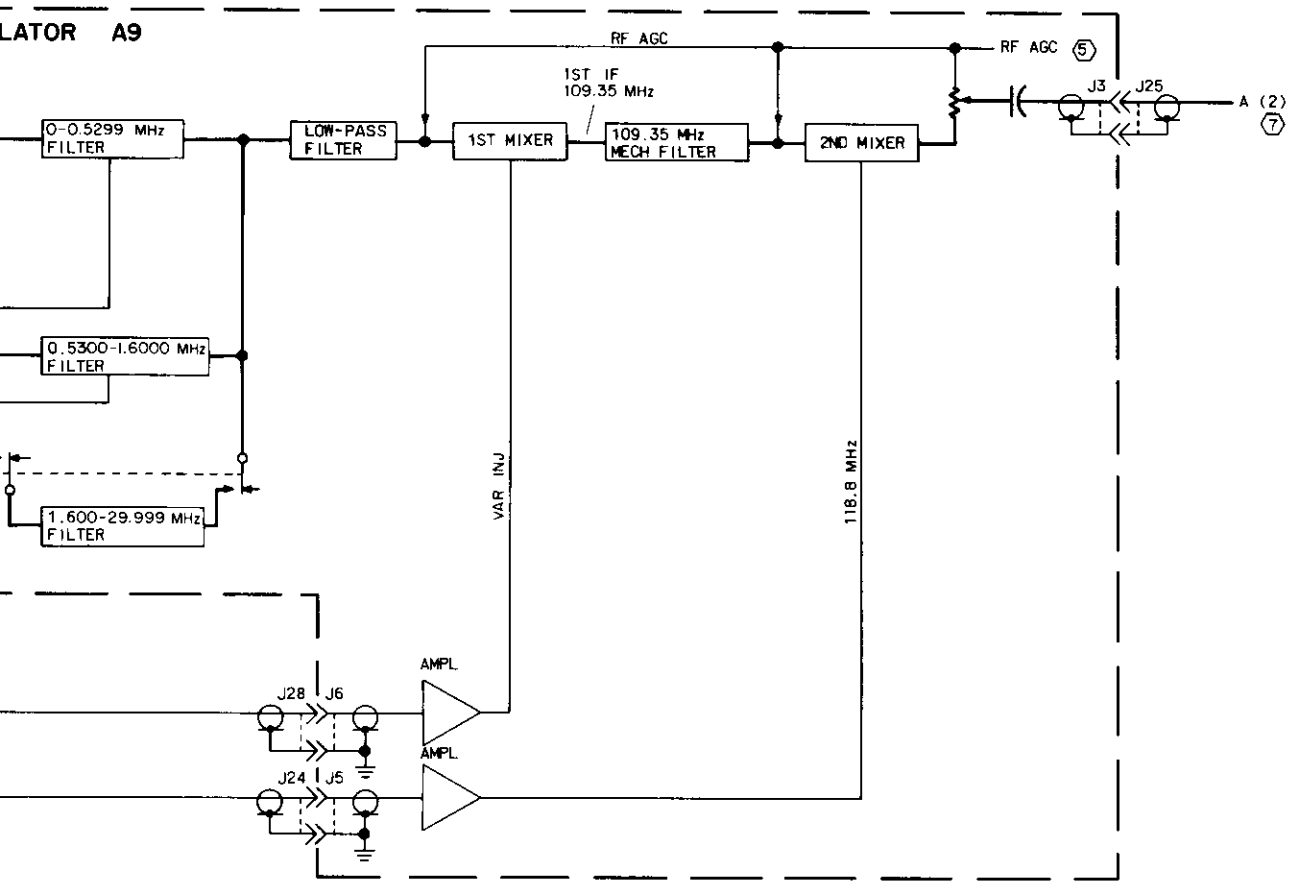


TPA-0683-014

851S-1 Receiver, Block Diagram
Figure 1



STANDARD BANDPASS FILTERING:
637-1767-001 - NARROW BAND 109.35 MHz FILTER (±7.50 kHz AT 3 dB POI
637-1767-002 - BROADBAND 109.35 MHz FILTER (±6.10 kHz AT 0.5 dB POINT



6 FILTERING:
- NARROW BAND 109.35 MHz FILTER (±7.50 kHz AT 3 dB POINTS).
- BROADBAND 109.35 MHz FILTER (±6.10 kHz AT 0.5 dB POINTS).

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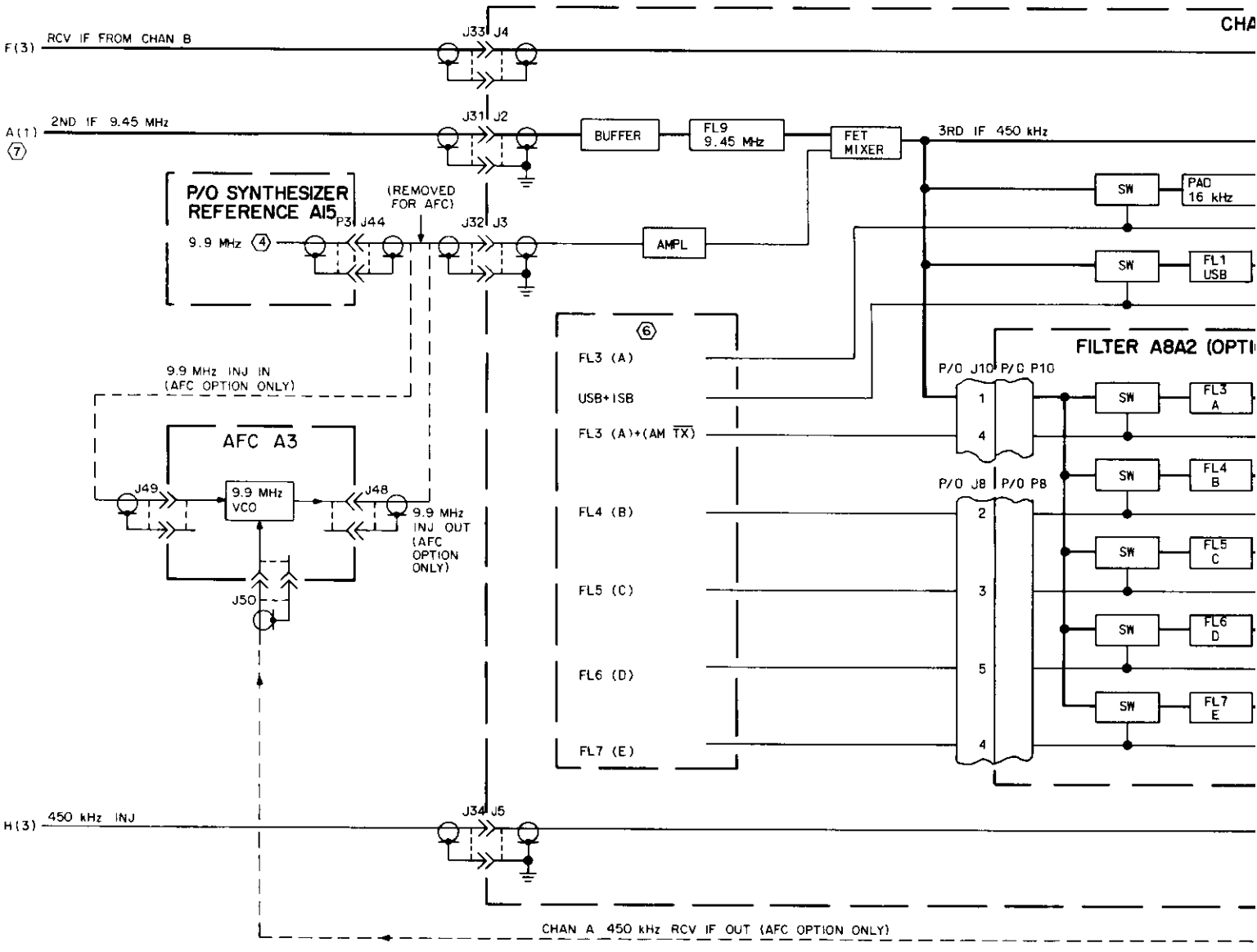
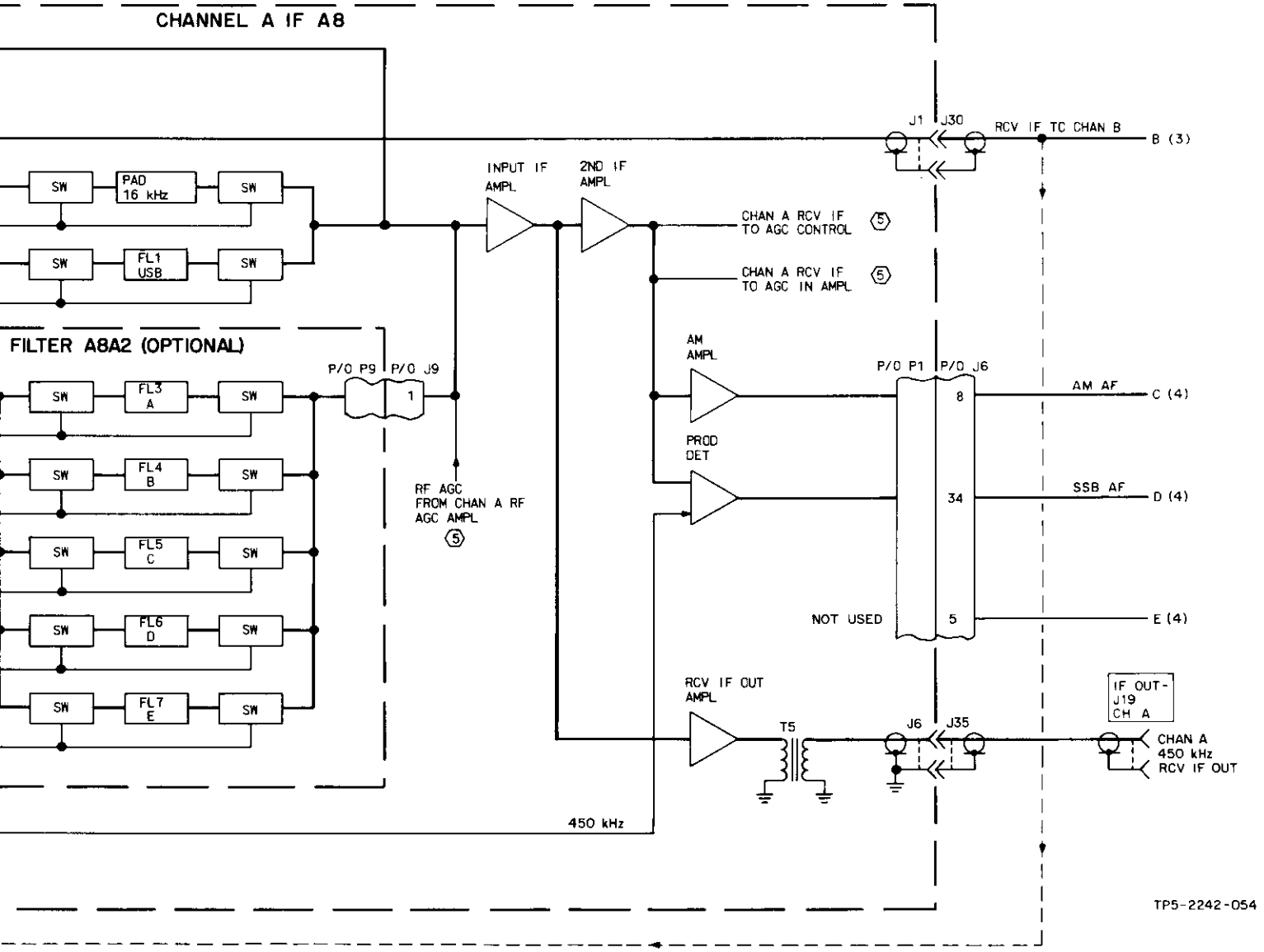
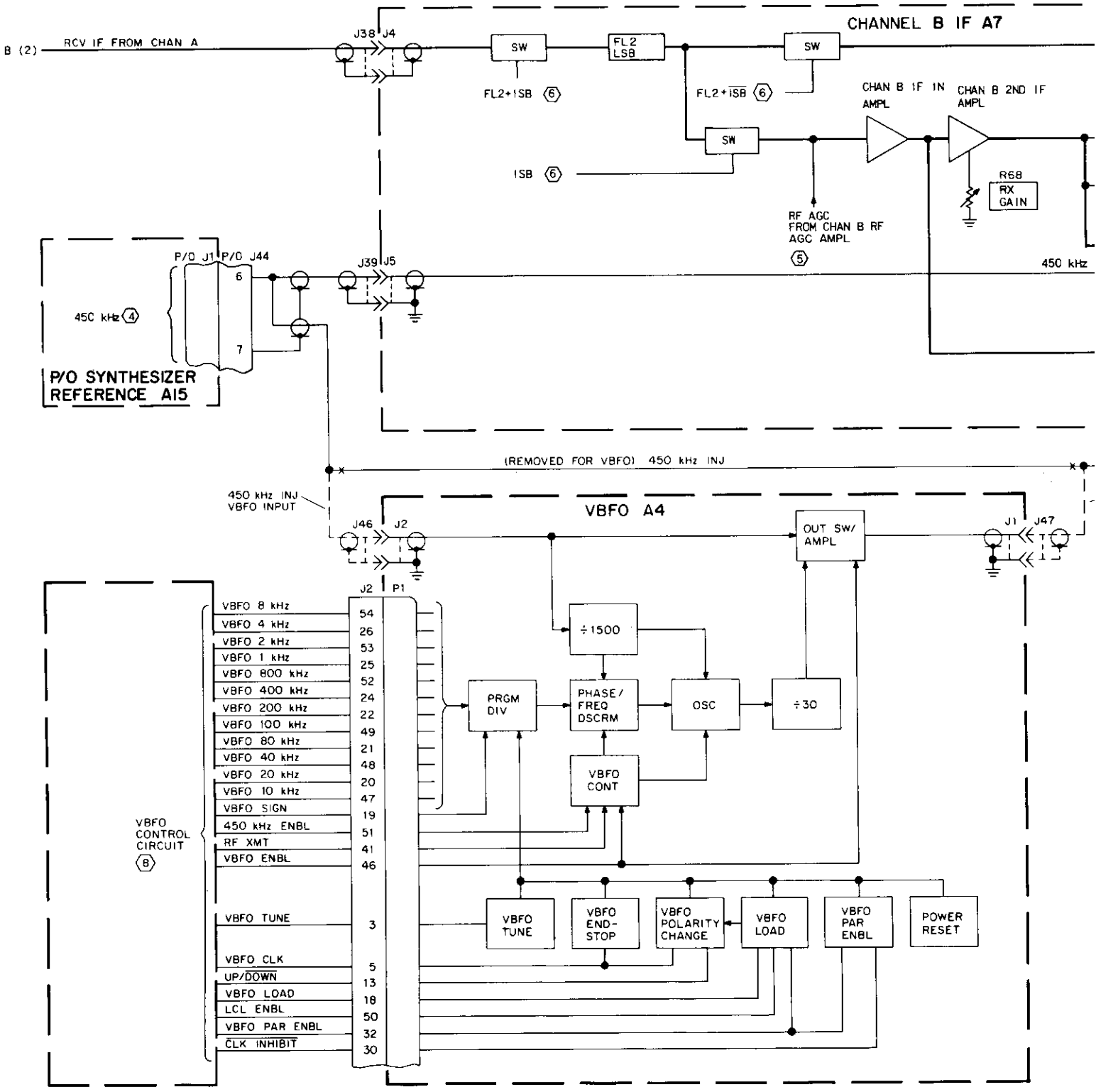
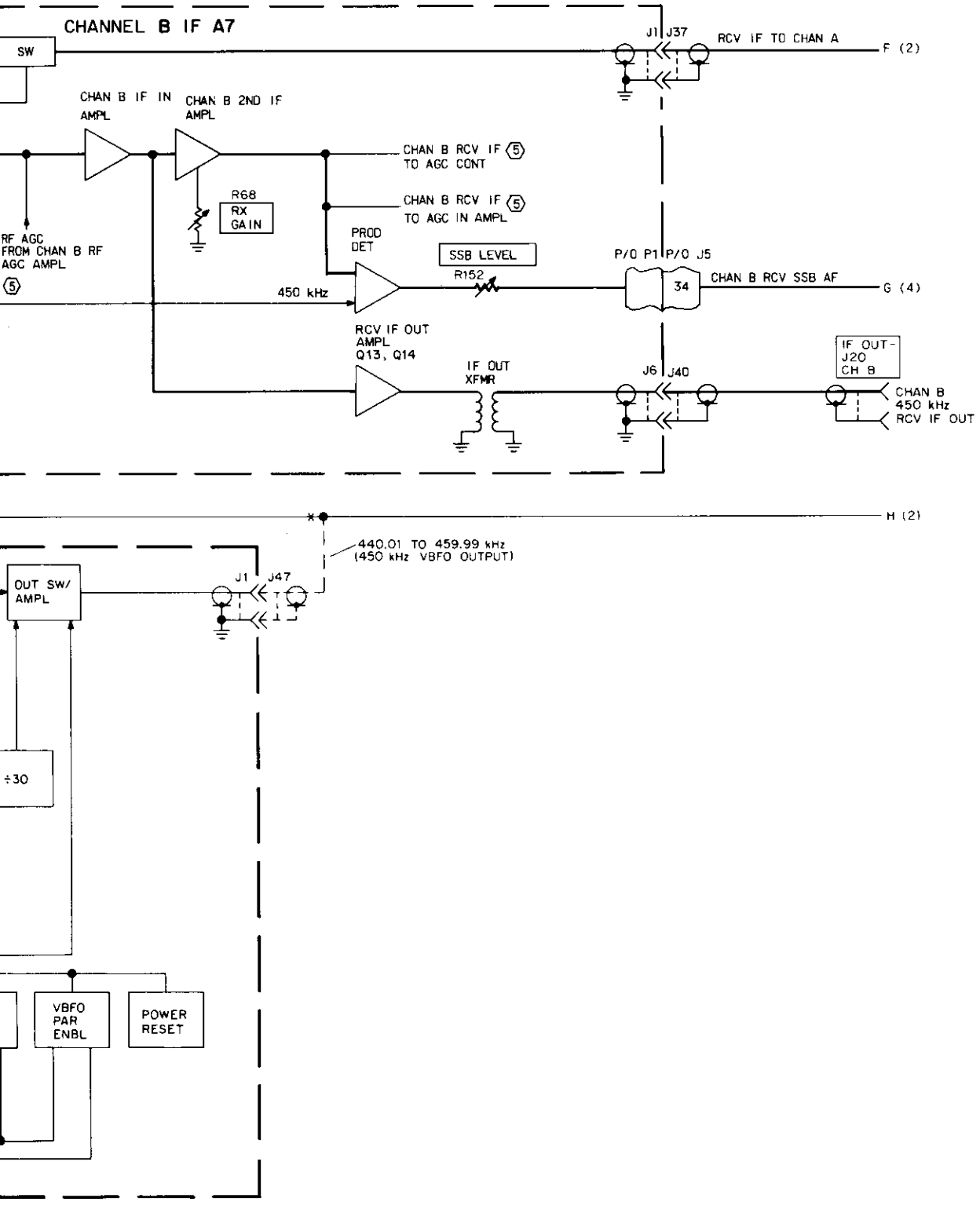
Receive Function, Block Diagram
Figure 2 (Sheet 1 of 5)


CHA
F(3)
RCV IF FROM CHAN B
J33
J4
A(1)
7
2ND IF 9.45 MHz
J31
J2
BUFFER
FL9
9.45 MHz
FET
MIXER
3RD IF 450 kHz
P/O SYNTHESIZER
REFERENCE A15
(REMOVED
FOR AFC)
P3
J44
J32
J3
9.9 MHz
4
AMPL
SW
PAD
16 kHz
SW
FL1
USB
6
FL3 (A)
USB+ISB
FL3 (A)+(AM TX)
FL4 (B)
FL5 (C)
FL6 (D)
FL7 (E)
FILTER A8A2 (OPTI
P/O J10
P/O P10
1
4
SW
FL3
A
P/O J8
P/O P8
2
3
5
4
SW
FL4
B
SW
FL5
C
SW
FL6
D
SW
FL7
E
9.9 MHz INJ IN
(AFC OPTION ONLY)
AFC A3
J49
9.9 MHz
VCO
J48
9.9 MHz
INJ OUT
(AFC
OPTION
ONLY)
J50
H(3)
450 kHz INJ
J34
J5
CHAN A 450 kHz RCV IF OUT (AFC OPTION ONLY)



Receive Function, Block Diagram
Figure 2 (Sheet 2)


CHANNEL B IF A7
B (2)
RCV IF FROM CHAN A
J38
J4
SW
FL2 LSB
SW
FL2+ISB (6)
FL2+ISB (6)
CHAN B 1F IN AMPL
CHAN B 2ND IF AMPL
SW
ISB (6)
R68
RX GAIN
RF AGC FROM CHAN B RF AGC AMPL
(5)
450 kHz
P/O J1
P/O J44
6
7
J39
J5
450 kHz (4)
P/O SYNTHESIZER REFERENCE A15
(REMOVED FOR VBFO) 450 kHz INJ
450 kHz INJ VBFO INPUT
VBFO A4
J46
J2
OUT SW/ AMPL
J1
J47
J2
P1
VBFO 8 kHz
VBFO 4 kHz
VBFO 2 kHz
VBFO 1 kHz
VBFO 800 kHz
VBFO 400 kHz
VBFO 200 kHz
VBFO 100 kHz
VBFO 80 kHz
VBFO 40 kHz
VBFO 20 kHz
VBFO 10 kHz
VBFO SIGN
450 kHz ENBL
RF XMT
VBFO ENBL
VBFO TUNE
VBFO CLK
UP/DOWN
VBFO LOAD
LCL ENBL
VBFO PAR ENBL
CLK INHIBIT
54
26
53
25
52
24
22
49
21
48
20
47
19
51
41
46
3
5
13
18
50
32
30
VBFO CONTROL CIRCUIT (8)
÷1500
PRGM DIV
PHASE/ FREQ DSCRM
OSC
÷30
VBFO CONT
VBFO TUNE
VBFO END-STOP
VBFO POLARITY CHANGE
VBFO LOAD
VBFO PAR ENBL
POWER RESET



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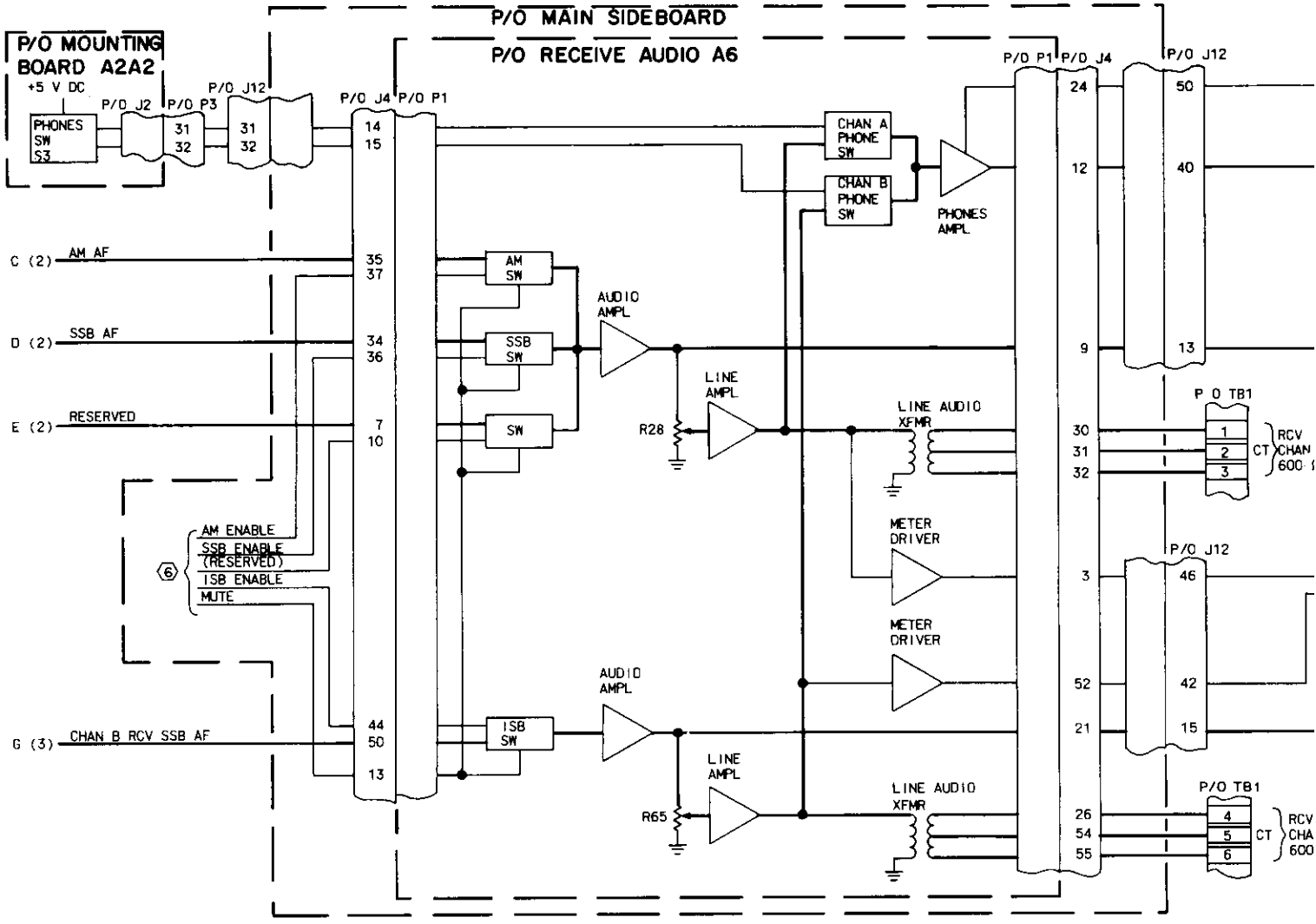
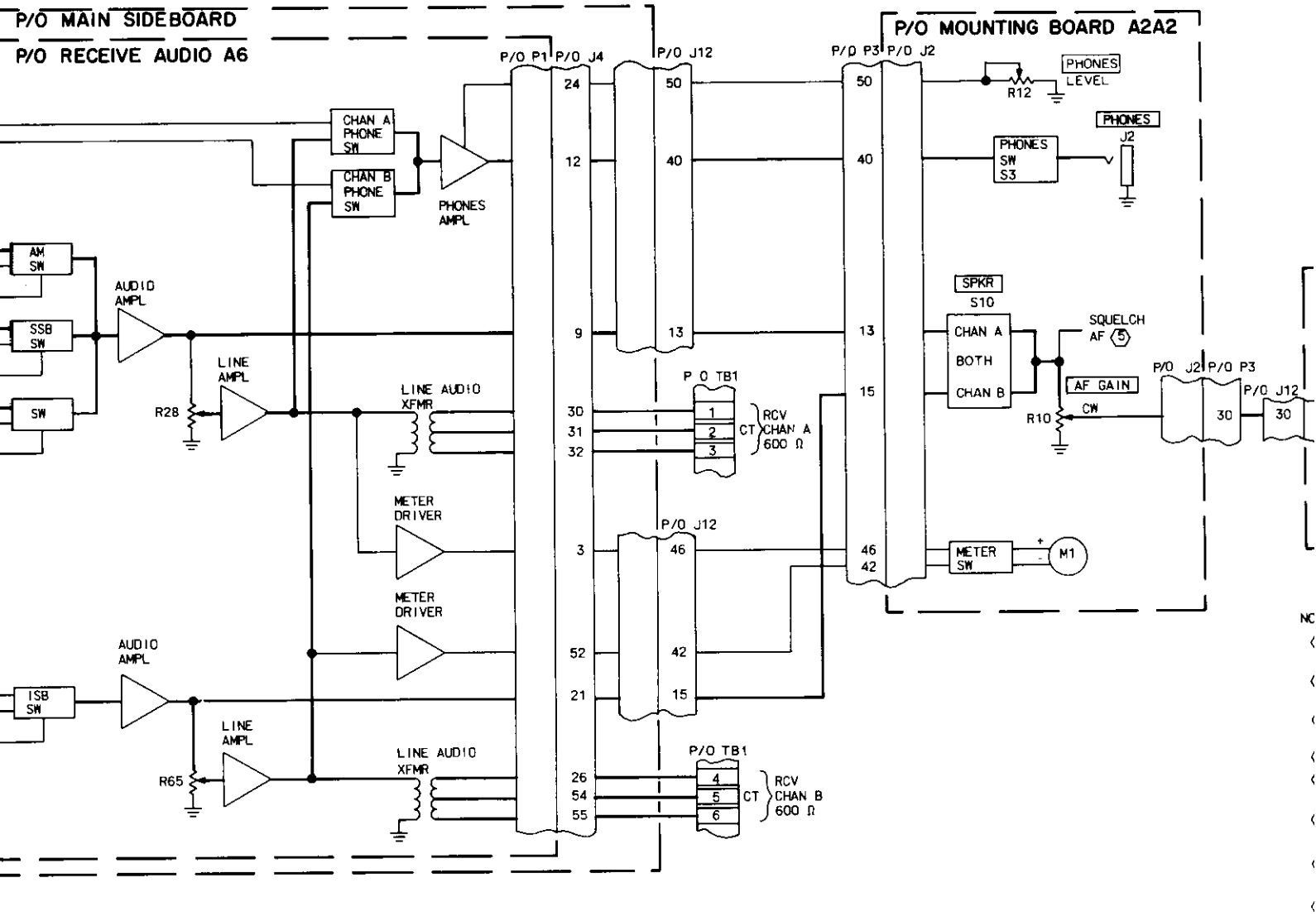
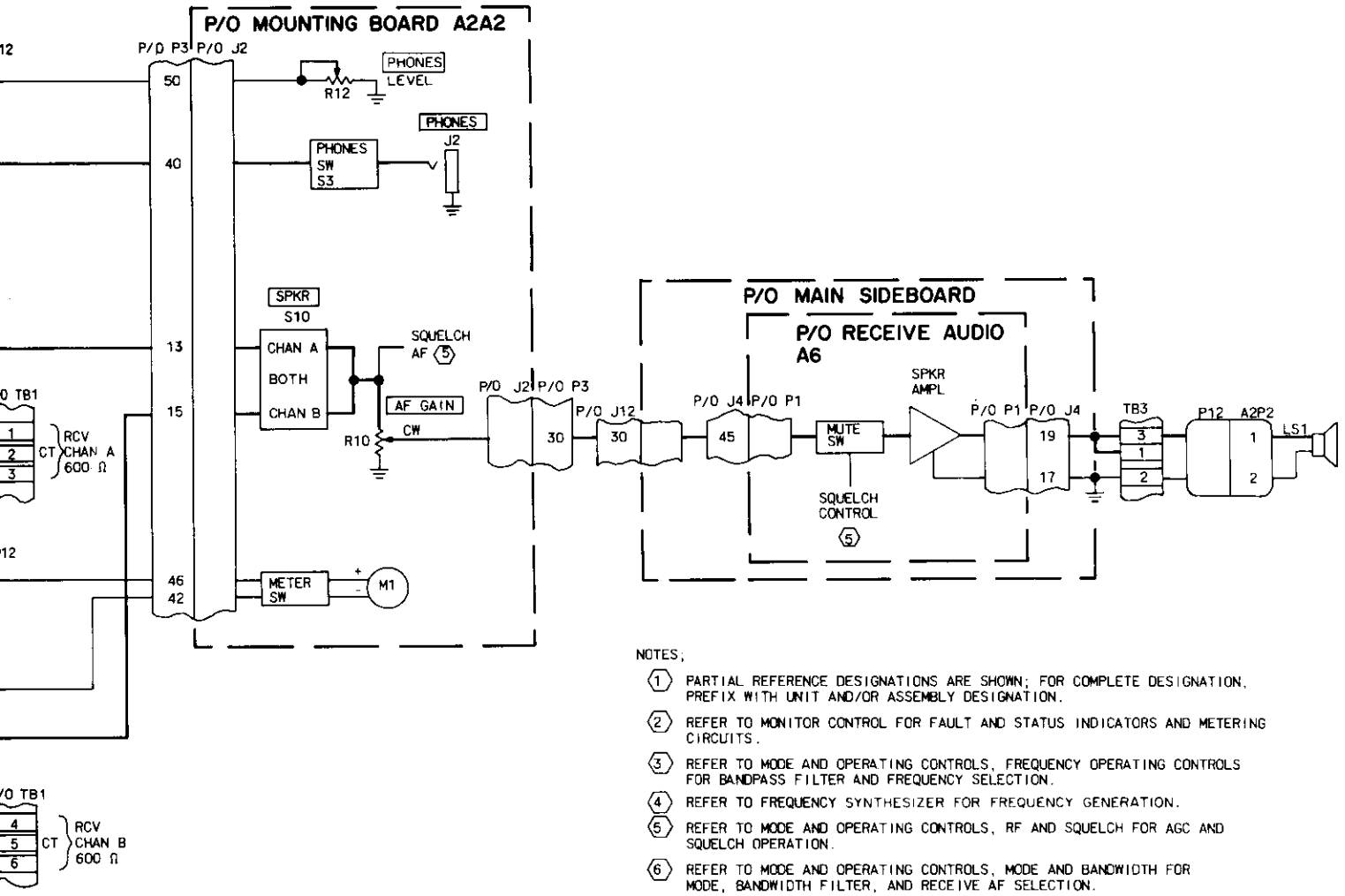
Receive Function, Block Diagram
Figure 2 (Sheet 3)


P/O MAIN SIDEBOARD
P/O RECEIVE AUDIO A6
P/O MOUNTING BOARD A2A2
+5 V DC
PHONES SW S3
P/O J2
P/O P3
P/O J12
31
32
P/O J4
P/O P1
14
15
C (2) AM AF
35
37
D (2) SSB AF
34
36
E (2) RESERVED
7
10
AM SW
SSB SW
SW
AUDIO AMPL
R28
LINE AMPL
CHAN A PHONE SW
CHAN B PHONE SW
PHONES AMPL
P/O P1
P/O J4
P/O J12
24
12
9
50
40
13
LINE AUDIO XFMR
P O TB1
30
31
32
1
2
3
CT
RCV CHAN
600
METER DRIVER
METER DRIVER
P/O J12
3
46
52
42
21
15
AM ENABLE
SSB ENABLE
(RESERVED)
ISB ENABLE
MUTE
6
G (3) CHAN B RCV SSB AF
44
50
13
ISB SW
AUDIO AMPL
R65
LINE AMPL
LINE AUDIO XFMR
P/O TB1
26
54
55
4
5
6
CT
RCV
CHA
600


P/O MAIN SIDEBOARD
P/O RECEIVE AUDIO A6
P/O MOUNTING BOARD A2A2
P/O P1
P/O J4
P/O J12
P/O P3
P/O J2
CHAN A PHONE SW
CHAN B PHONE SW
PHONES AMPL
PHONES LEVEL
R12
PHONES
J2
PHONES SW S3
AM SW
SSB SW
SW
AUDIO AMPL
LINE AMPL
R28
LINE AUDIO XFMR
P O TB1
RCV CHAN A 600 Ω
CT
SPKR
S10
CHAN A
BOTH
CHAN B
SQUELCH AF
AF GAIN
CW
R10
P/O J2
P/O P3
P/O J12
METER DRIVER
METER SW
M1
ISB SW
R65
RCV CHAN B 600 Ω
24
12
9
3
52
21
26
54
55
50
40
13
46
42
15
30
31
32
1
2
3
4
5
6

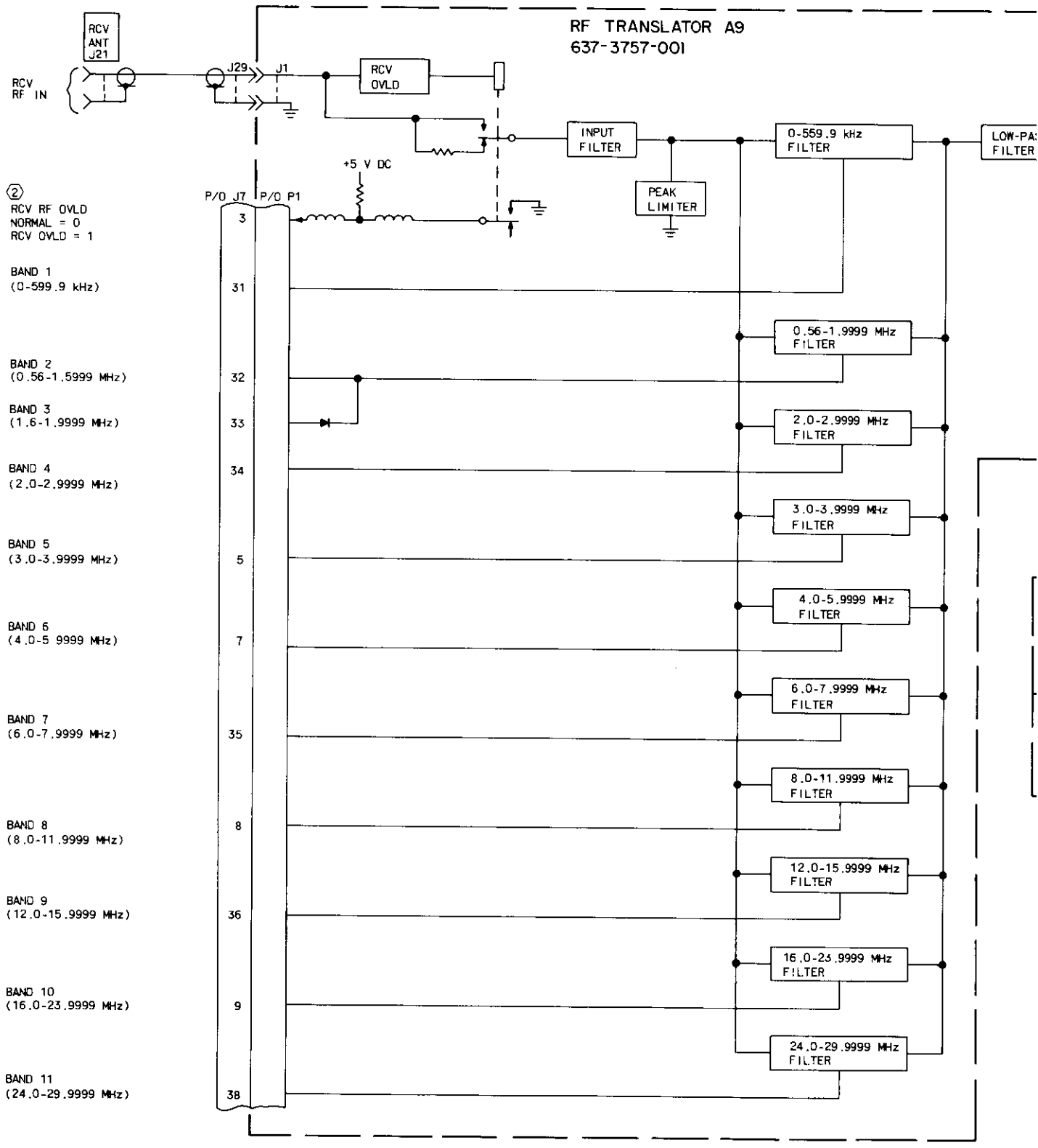


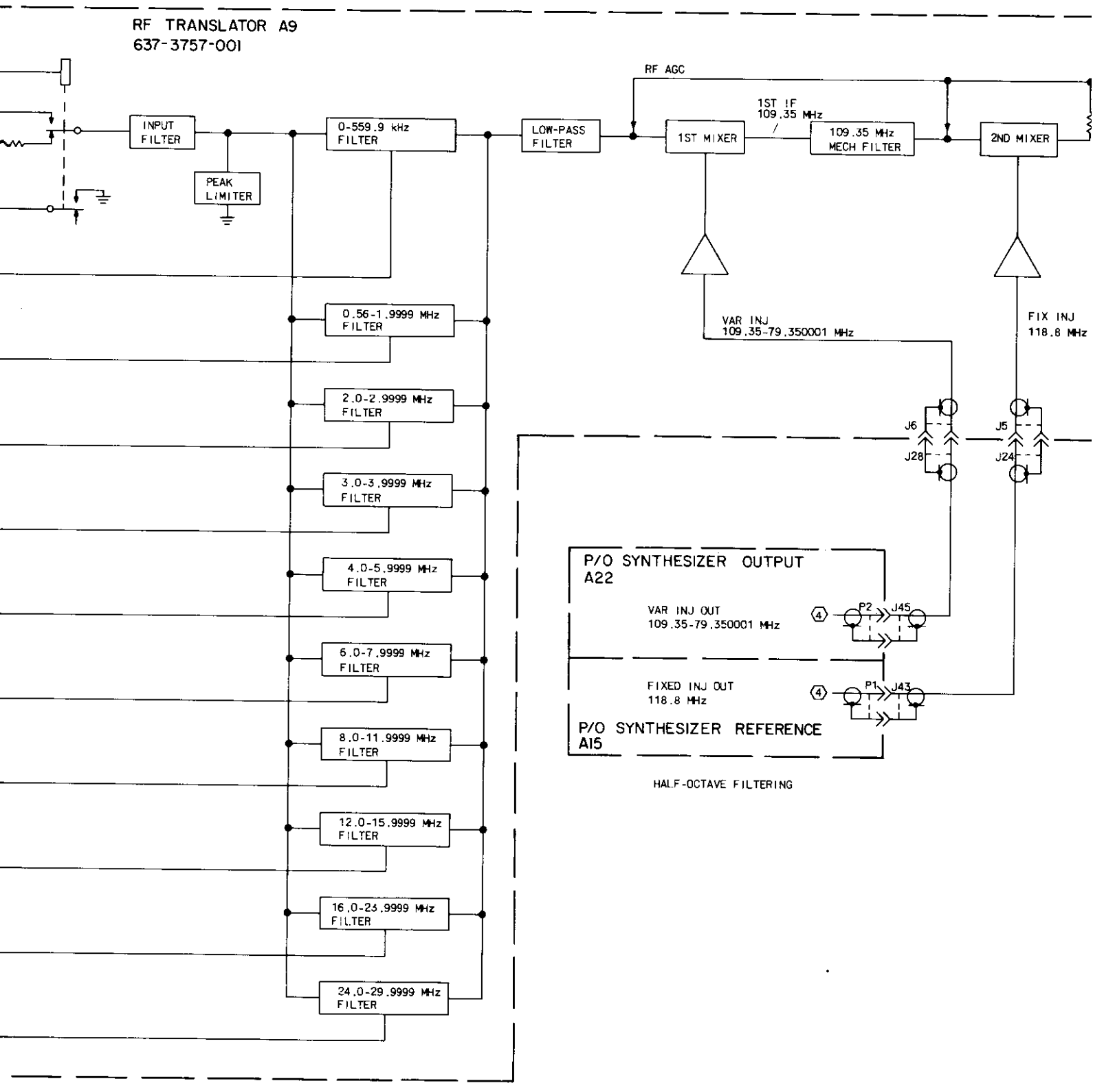
NOTES;

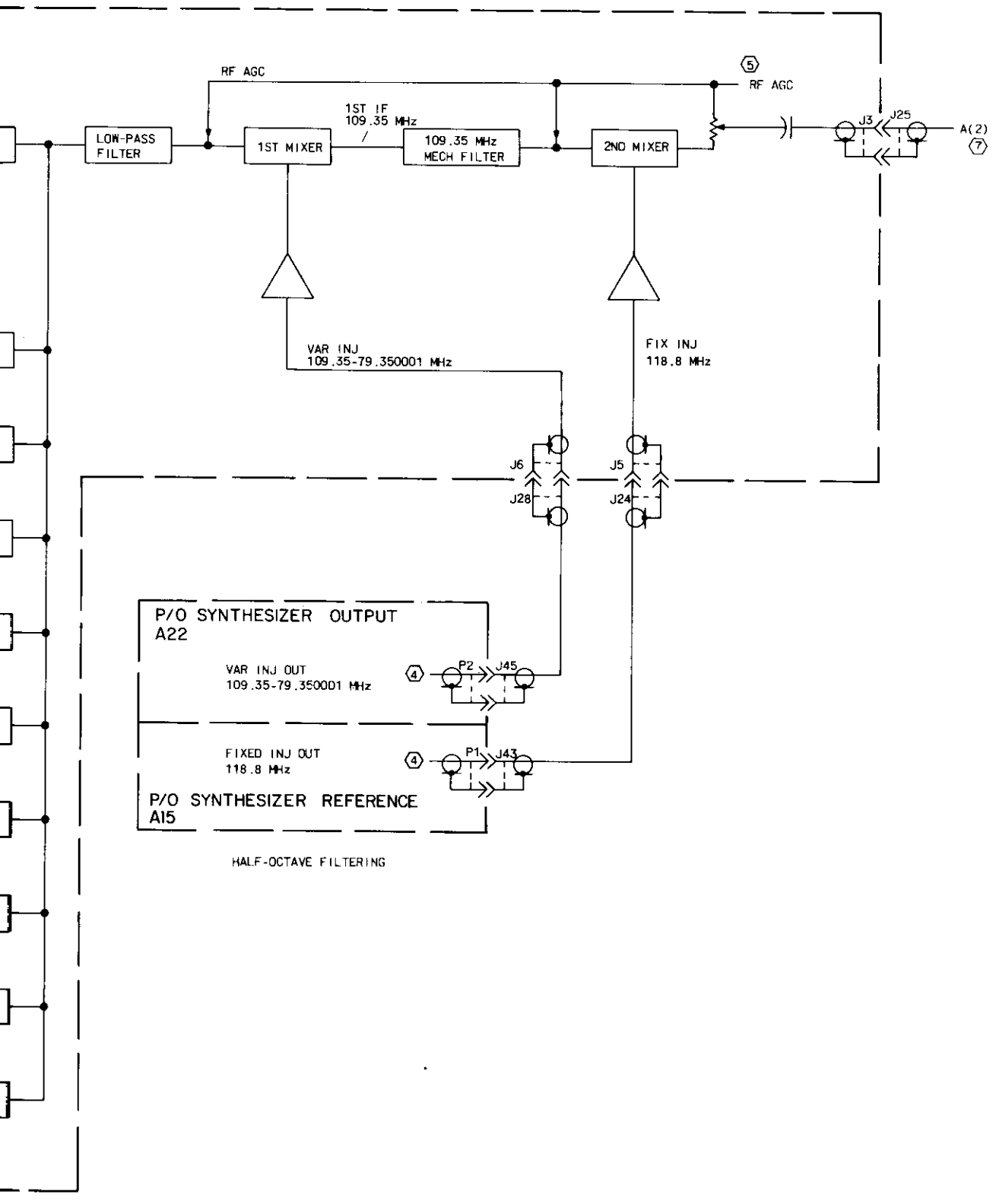
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
2. REFER TO MONITOR CONTROL FOR FAULT AND STATUS INDICATORS AND METERING CIRCUITS.
3. REFER TO MODE AND OPERATING CONTROLS, FREQUENCY OPERATING CONTROLS FOR BANDPASS FILTER AND FREQUENCY SELECTION.
4. REFER TO FREQUENCY SYNTHESIZER FOR FREQUENCY GENERATION.
5. REFER TO MODE AND OPERATING CONTROLS, RF AND SQUELCH FOR AGC AND SQUELCH OPERATION.
6. REFER TO MODE AND OPERATING CONTROLS, MODE AND BANDWIDTH FOR MODE, BANDWIDTH FILTER, AND RECEIVE AF SELECTION.
7. IF STANDARD BANDPASS FILTERING IS USED, SIGNAL COMES FROM SHEET 1. IF HALF-OCTAVE FILTERING IS USED, SIGNAL COMES FROM SHEET 5.
8. REFER TO FREQUENCY CONTROL FOR CONTROL OF VBFO.

TP5-2242-054

Receive Function, Block Diagram
Figure 2 (Sheet 4)

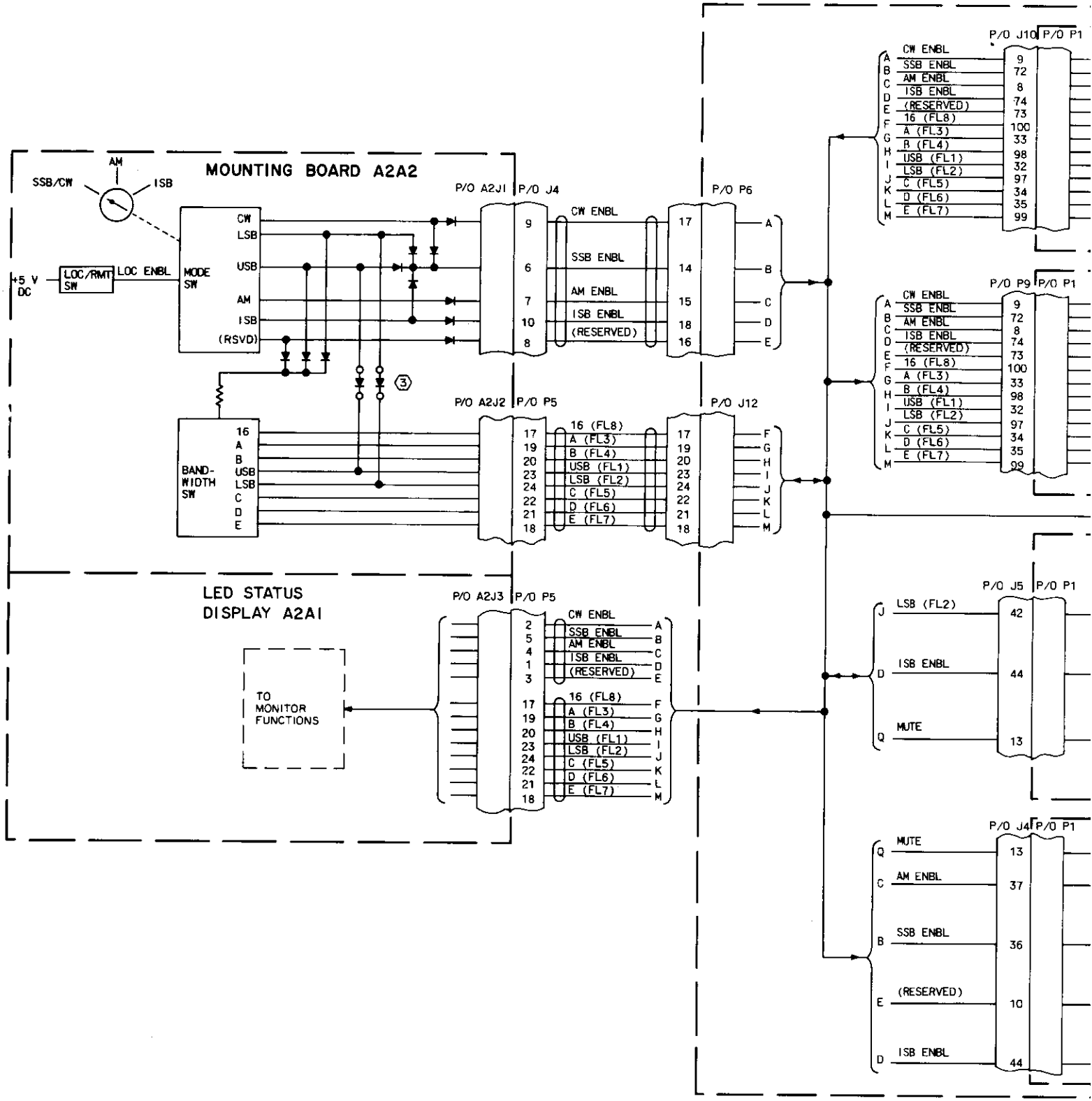

RF TRANSLATOR A9
637-3757-001
RCV ANT J21
RCV RF IN
J29
J1
RCV OVLD
INPUT FILTER
PEAK LIMITER
0-559.9 kHz FILTER
LOW-PAS FILTER
+5 V DC
P/O J7
P/O P1
② RCV RF OVLD NORMAL = 0 RCV OVLD = 1
BAND 1 (0-599.9 kHz)
BAND 2 (0.56-1.5999 MHz)
BAND 3 (1.6-1.9999 MHz)
BAND 4 (2.0-2.9999 MHz)
BAND 5 (3.0-3.9999 MHz)
BAND 6 (4.0-5.9999 MHz)
BAND 7 (6.0-7.9999 MHz)
BAND 8 (8.0-11.9999 MHz)
BAND 9 (12.0-15.9999 MHz)
BAND 10 (16.0-23.9999 MHz)
BAND 11 (24.0-29.9999 MHz)
3
31
32
33
34
5
7
35
8
36
9
38
0.56-1.9999 MHz FILTER
2.0-2.9999 MHz FILTER
3.0-3.9999 MHz FILTER
4.0-5.9999 MHz FILTER
6.0-7.9999 MHz FILTER
8.0-11.9999 MHz FILTER
12.0-15.9999 MHz FILTER
16.0-23.9999 MHz FILTER
24.0-29.9999 MHz FILTER

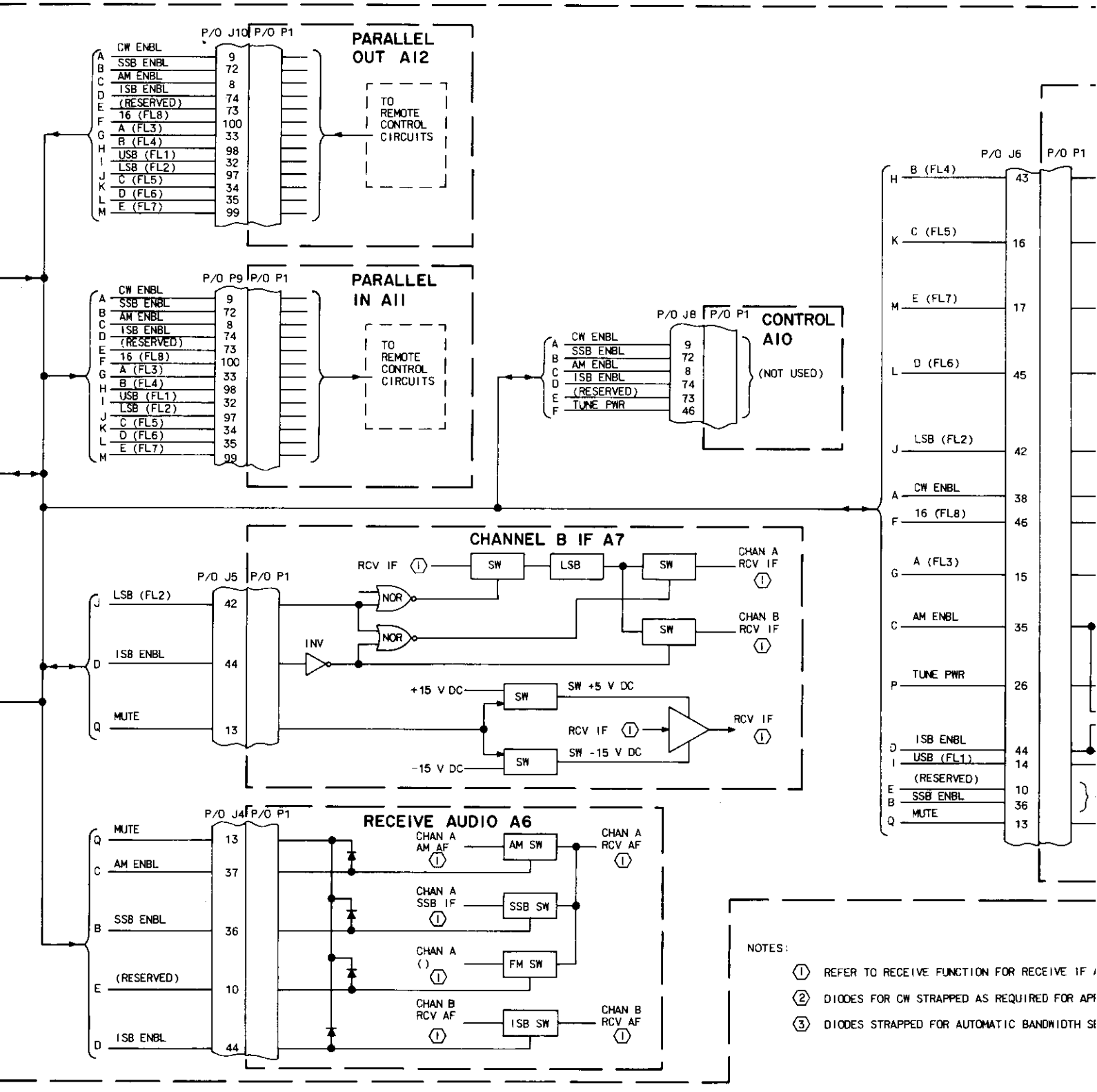

RF TRANSLATOR A9
637-3757-001
INPUT FILTER
PEAK LIMITER
0-559.9 kHz FILTER
0.56-1.9999 MHz FILTER
2.0-2.9999 MHz FILTER
3.0-3.9999 MHz FILTER
4.0-5.9999 MHz FILTER
6.0-7.9999 MHz FILTER
8.0-11.9999 MHz FILTER
12.0-15.9999 MHz FILTER
16.0-23.9999 MHz FILTER
24.0-29.9999 MHz FILTER
LOW-PASS FILTER
RF AGC
1ST MIXER
1ST IF 109.35 MHz
109.35 MHz MECH FILTER
2ND MIXER
VAR INJ 109.35-79.350001 MHz
FIX INJ 118.8 MHz
J6
J28
J5
J24
P/O SYNTHESIZER OUTPUT A22
VAR INJ OUT 109.35-79.350001 MHz
FIXED INJ OUT 118.8 MHz
P2
J45
P1
J43
P/O SYNTHESIZER REFERENCE A15
HALF-OCTAVE FILTERING

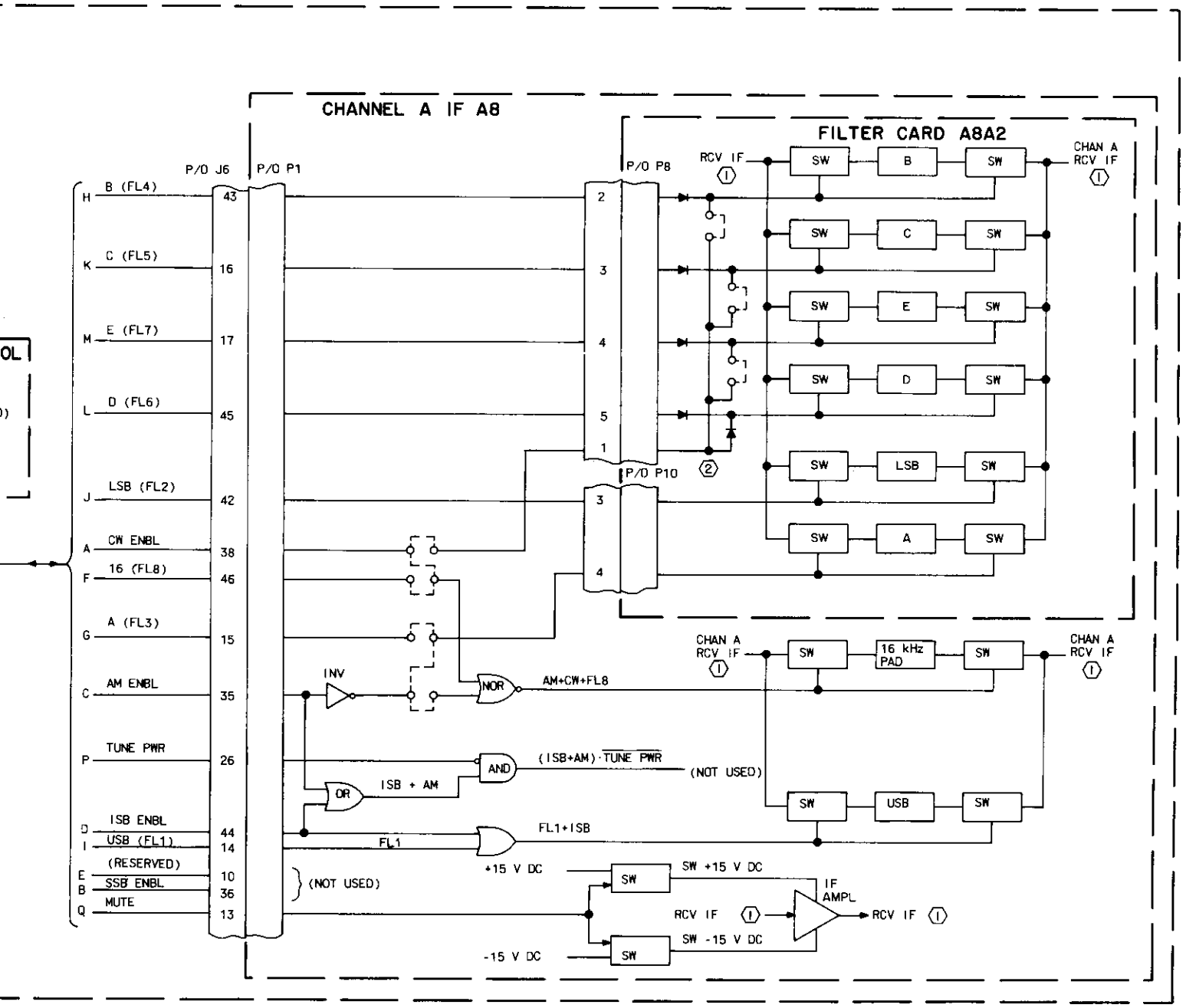


TP5-2242-054

Receiver Function, Block Diagram
Figure 2 (Sheet 5)


MOUNTING BOARD A2A2
SSB/CW
AM
ISB
+5 V DC
LOC/RMT SW
LOC ENBL
MODE SW
CW
LSB
USB
AM
ISB
(RSVD)
BAND-WIDTH SW
16
A
B
USB
LSB
C
D
E
P/O A2J1
P/O J4
P/O P6
P/O A2J2
P/O P5
P/O J12
CW ENBL
SSB ENBL
AM ENBL
ISB ENBL
(RESERVED)
16 (FL8)
A (FL3)
B (FL4)
USB (FL1)
LSB (FL2)
C (FL5)
D (FL6)
E (FL7)
LED STATUS DISPLAY A2A1
TO MONITOR FUNCTIONS
P/O A2J3
P/O P5
P/O J10
P/O P1
P/O P9
P/O P1
P/O J5
P/O P1
P/O J4
P/O P1
MUTE


PARALLEL OUT A12
P/O J10
P/O P1
CW ENBL
SSB ENBL
AM ENBL
ISB ENBL
(RESERVED)
16 (FL8)
A (FL3)
B (FL4)
USB (FL1)
LSB (FL2)
C (FL5)
D (FL6)
E (FL7)
9
72
8
74
73
100
33
98
32
97
34
35
99
TO REMOTE CONTROL CIRCUITS
PARALLEL IN A11
P/O P9
P/O P1
CONTROL A10
P/O J8
P/O P1
TUNE PWR
46
(NOT USED)
P/O J6
P/O P1
43
16
17
45
42
38
46
15
35
26
44
14
10
36
13
CHANNEL B IF A7
P/O J5
P/O P1
RCV IF
SW
LSB
CHAN A RCV IF
CHAN B RCV IF
NOR
INV
+15 V DC
SW +5 V DC
-15 V DC
SW -15 V DC
RECEIVE AUDIO A6
P/O J4
P/O P1
CHAN A AM AF
CHAN A SSB IF
CHAN A ( )
CHAN B RCV AF
AM SW
SSB SW
FM SW
ISB SW
CHAN A RCV AF
CHAN B RCV AF
NOTES:
1 REFER TO RECEIVE FUNCTION FOR RECEIVE IF
2 DIODES FOR CW STRAPPED AS REQUIRED FOR AP
3 DIODES STRAPPED FOR AUTOMATIC BANDWIDTH S



REFER TO RECEIVE FUNCTION FOR RECEIVE IF AND RECEIVE AF LINES.

DIODES FOR CW STRAPPED AS REQUIRED FOR APPROPRIATE CW OPERATION.

DIODES STRAPPED FOR AUTOMATIC BANDWIDTH SELECTION IN LSB/USB MODES IF DESIRED.

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Mode and Bandwidth, Block Diagram
Figure 3

With the BANDWIDTH switch in the B position, a B (FL4) signal (+5 V dc) is supplied at P3-20, to J12-20, to J6-43, to A8A2P8-2, and enables B filter (optional bandwidth) on filter A8A2.

With the BANDWIDTH switch in the USB position, a USB (FL1) signal (+5 V dc) is supplied at P3-23, to J12-33, to J6-14, and enables USB filter in channel A if A8.

With the BANDWIDTH switch in the LSB position, an LSB (FL2) signal (+5 V dc) is supplied at P3-24, to J12-24, to J5-42, and enables LSB filter and channel A receive if switch in channel B if A7.

With the BANDWIDTH switch in the C position, a C (FL5) signal (+5 V dc) is supplied at P3-22, to J12-23, to J6-16, to A8A2P8-3, and enables the C filter (optional bandwidth) on filter A8A2.

With the BANDWIDTH switch in the D position, a D (FL6) signal (+5 V dc) is supplied at P3-21, to J12-21, to J6-45, to A8A2P8-5, and enables the D filter (optional bandwidth) on filter A8A2.

With the BANDWIDTH switch in the E position, an E (FL7) signal (+5 V dc) is supplied at P3-18, to J12-18, to J6-17, to A8A2P8-4, and enables the E filter (optional bandwidth) on filter A8A2.

When the MODE switch is set to the AM mode, an AM enable signal (+5 V dc) is supplied at P4-7, to P6-15, to J6-35, to J4-27, and enables the AM audio switch in receive audio A6.

When the MODE switch is set to the ISB mode, an ISB enable signal (+5 V dc) and an SSB enable signal (+5 V dc) are supplied. The ISB enable signal is supplied at P4-10, to P6-18, to J4-44, and enables the ISB audio switch (channel B receive af) in receive audio A6. The SSB enable signal is supplied at P4-6, to P6-14, to J4-36, and enables the SSB audio switch (channel A receive af) in receive audio A6. The ISB enable signal is also supplied to J6-44 and enables the USB filter in channel A if A8 and is supplied to J5-44 and enables the LSB filter and channel B if switch in channel B is A7.

Figure 4 shows a simplified diagram of the mode and bandwidth selection described in the foregoing paragraphs.

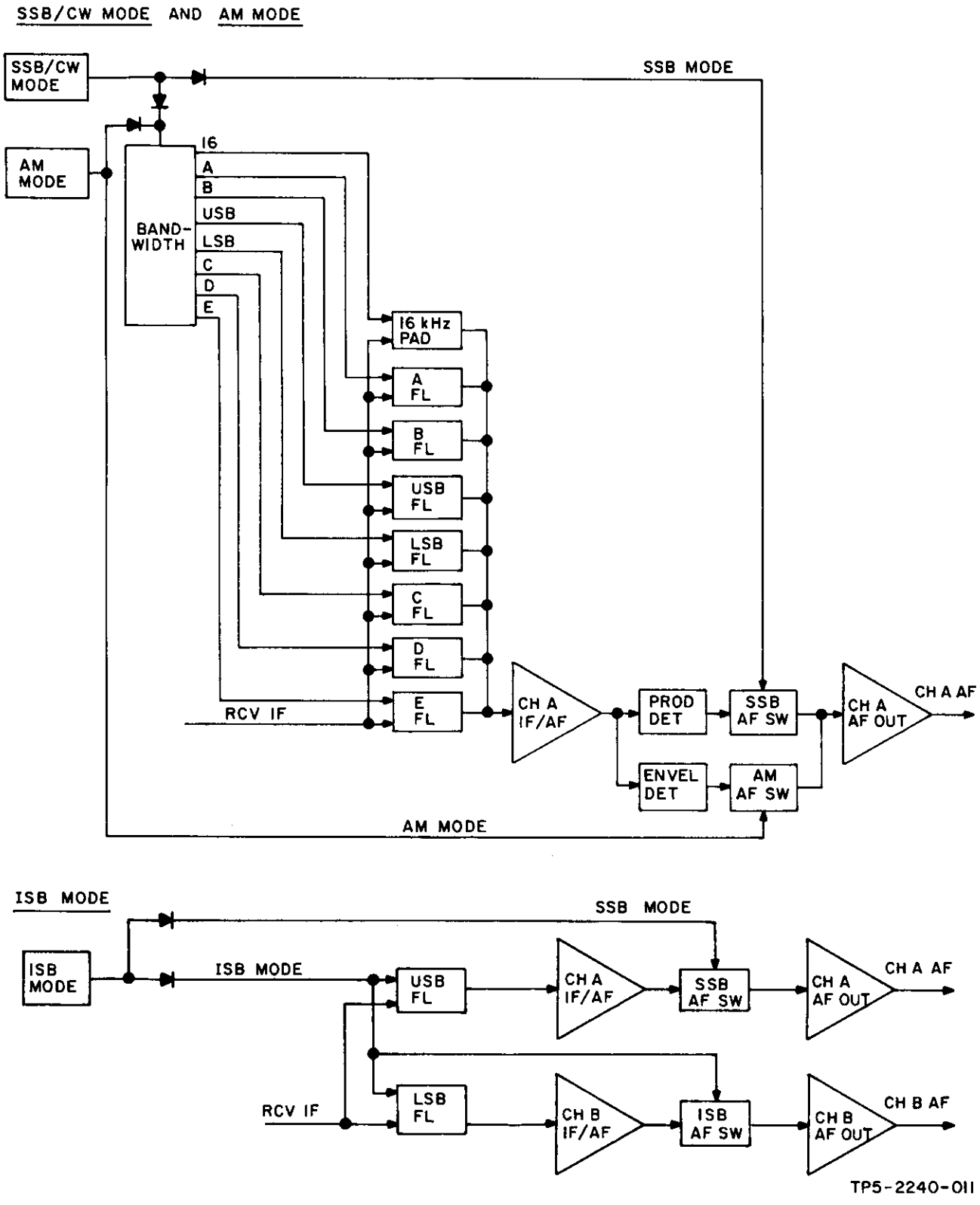
When an external controlling device is used, the same mode and bandwidth operations apply, except the control signals are supplied as serial data to serial interface A13 and converted from serial data to parallel data in parallel output A12. The outputs of parallel output A12 are supplied to the internal control circuits of the receiver.

2.2.2 Audio (Refer to figure 5.)

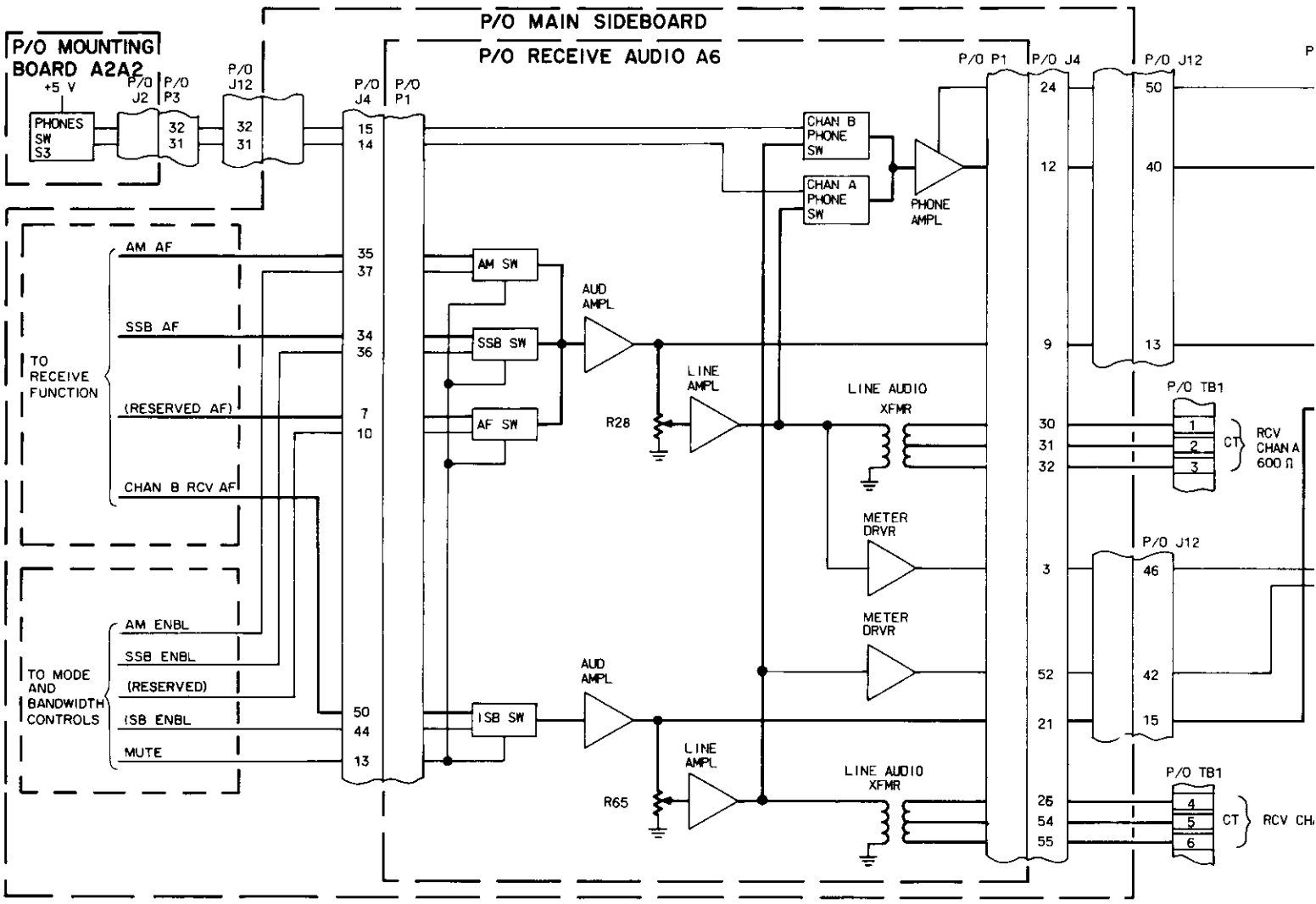
The 851S-1 audio can be monitored at the PHONES jack, at the internal speaker, at an external speaker, or through an external line audio circuit from TB1.

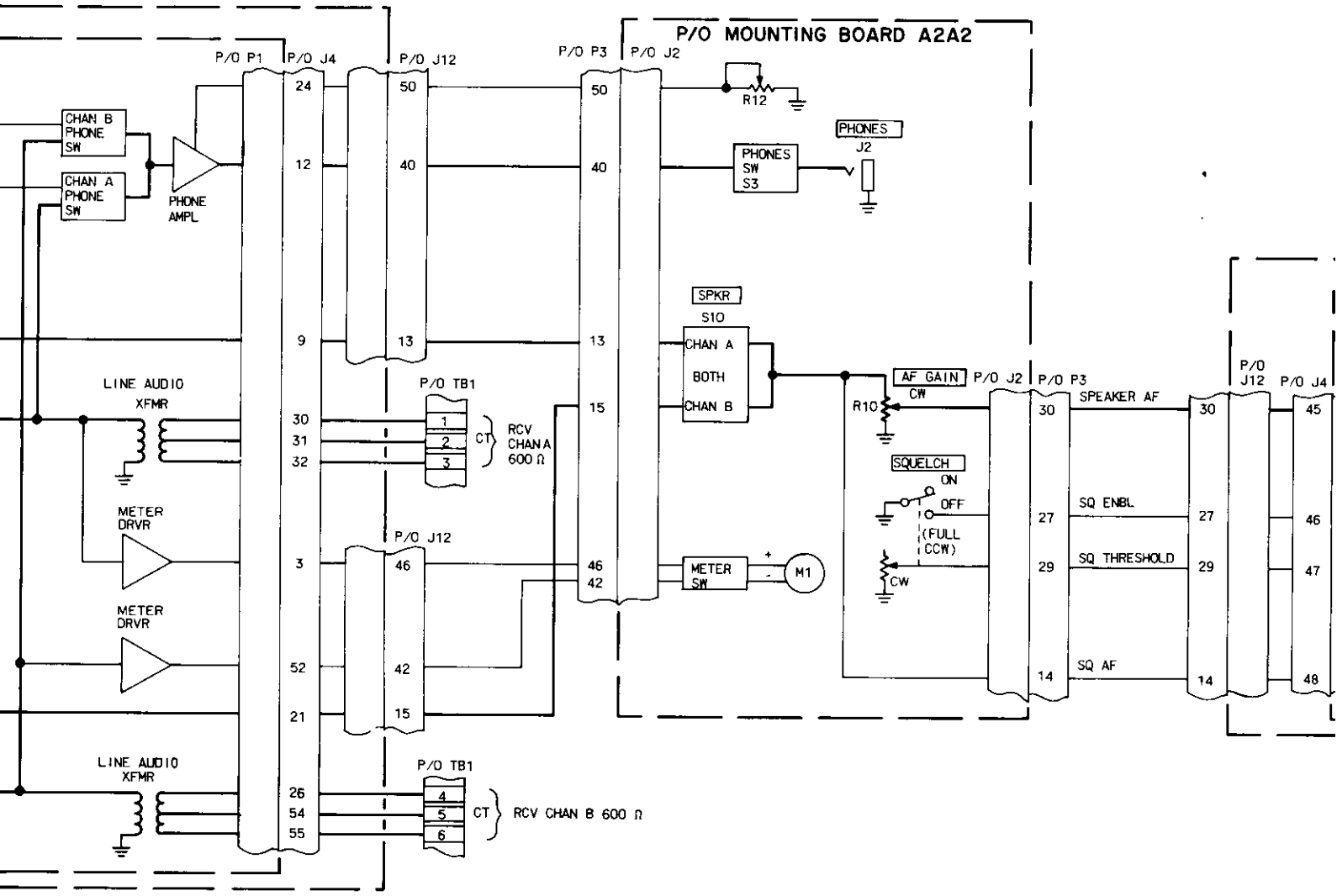
Phones audio is supplied by the headphone audio amplifier in receive audio A6. PHONES switch A2A2S3 selects channel A or channel B audio. If channel A is selected (PHONES switch in CH A position), a logic 1 signal is supplied through P3-31, J12-31, and J4-14 to the channel A phones switch in receive audio A6. Receive audio is supplied through the channel A phones switch, the phones audio amplifier, J4-12, J12-40, P3-40, and PHONES switch A2A2S3 to PHONES jack J2. If channel B is selected (PHONES switch in CH B position), a logic 1 signal is supplied through P3-32, J12-32, and J4-15 to the channel B phones switch in receive audio A6. Receive audio is supplied through the channel B phones switch, the phones audio amplifier, J4-12, J12-40, P3-40, and PHONES switch A2A2S3 to PHONES jack J2. Phones audio level is adjusted using the phones level adjust located in the center of the PHONES switch.

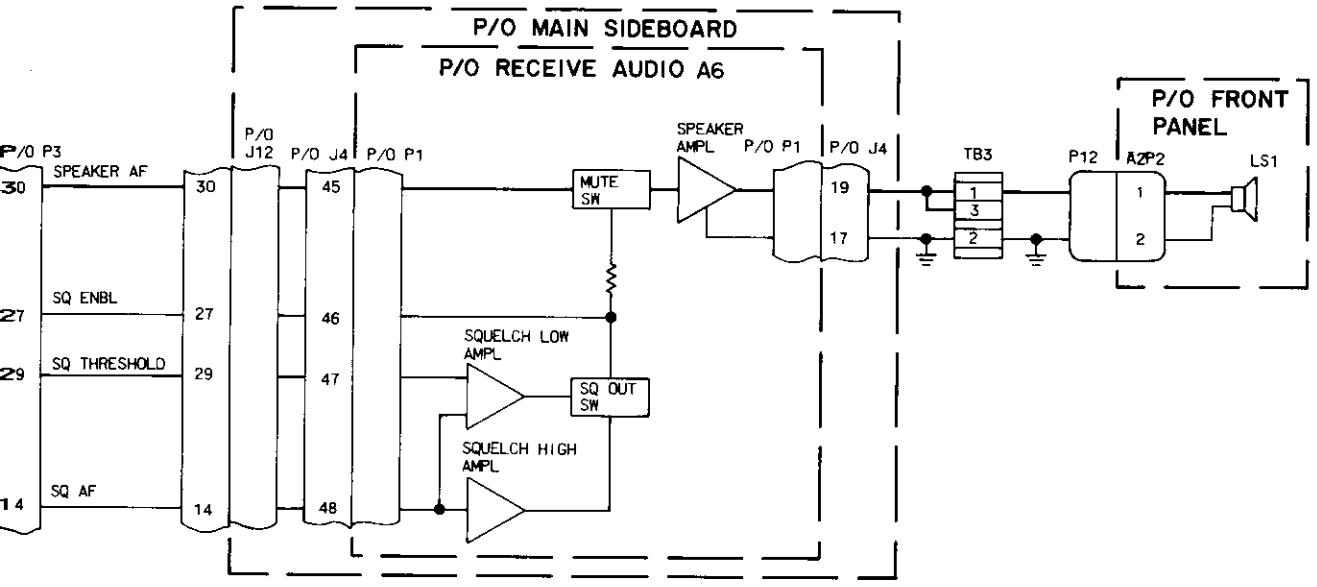
Speaker audio is supplied by the line audio amplifiers in receive audio A6. SPKR switch A2A2S10 selects channel A, channel B, or both channel A and channel B audio. If channel A is selected (SPKR switch in CH A position), channel A receive audio is supplied through J4-9, J12-13, P3-13, A2A2S10, A2A2R10, P3-30, J12-30, J4-45, through mute switch and speaker amplifier in receive audio A6. The speaker amplifier output is supplied through J4-19 to TB3-1, and speaker amplifier common is supplied through J4-17 to TB3-2. If channel B is selected (SPKR switch in CH B position), channel B receive audio is supplied through J4-21, J12-15, P3-15, A2A2S10, A2A2R10, P3-30, J12-30, J4-45, through mute switch and speaker amplifier in receive audio A6. The speaker amplifier output is supplied through J4-19 to TB3-1, and speaker amplifier common is supplied through J4-17 to TB3-2. If channel A and channel B are selected (SPKR switch in BOTH position), channel A and channel B receive audio are supplied, as described above. For internal speaker, TB3-1 is jumpered to TB3-3 and speaker audio is supplied from TB3-3 through P12-1 to loudspeaker LS1, common from TB3-2 through P12-2 to loudspeaker LS1. For external speaker, TB3-1 is connected directly to external speaker (jumper between TB3-1 and TB3-3 is removed) and speaker audio is supplied from TB3-1 to external loudspeaker, common from TB3-2 is connected directly to external loudspeaker common from TB3-2 is connected directly to external loudspeaker common. Speaker audio is volume controlled by AF GAIN control A2A2R10A.



Mode and Bandwidth Selection, Simplified Diagram
Figure 4


P/O MAIN SIDEBOARD
P/O RECEIVE AUDIO A6
P/O MOUNTING BOARD A2A2
+5 V
PHONES SW S3
P/O J2
P/O P3
P/O J12
P/O J4
P/O P1
32
31
15
14
CHAN B PHONE SW
CHAN A PHONE SW
PHONE AMPL
P/O P1
P/O J4
P/O J12
24
12
9
50
40
13
AM AF
SSB AF
(RESERVED AF)
CHAN B RCV AF
TO RECEIVE FUNCTION
35
37
34
36
7
10
AM SW
SSB SW
AF SW
AUD AMPL
R28
LINE AMPL
LINE AUDIO XFMR
P/O TB1
30
31
32
1
2
3
CT
RCV CHAN A 600 Ω
METER DRVR
P/O J12
3
46
AM ENBL
SSB ENBL
(RESERVED)
ISB ENBL
MUTE
TO MODE AND BANDWIDTH CONTROLS
50
44
13
ISB SW
AUD AMPL
52
42
21
15
R65
LINE AMPL
LINE AUDIO XFMR
P/O TB1
26
54
55
4
5
6
CT
RCV CH


P/O MOUNTING BOARD A2A2
P/O P1
P/O J4
P/O J12
P/O P3
P/O J2
CHAN B PHONE SW
CHAN A PHONE SW
PHONE AMPL
R12
PHONES
J2
PHONES SW S3
SPKR
S10
CHAN A
BOTH
CHAN B
AF GAIN
CW
R10
P/O J2
P/O P3
SPEAKER AF
P/O J12
P/O J4
SQUELCH
ON
OFF
(FULL CCW)
CW
SQ ENBL
SQ THRESHOLD
SQ AF
LINE AUDIO XFMR
P/O TB1
RCV CHAN A 600 Ω
CT
METER DRVR
METER DRVR
METER SW
M1
LINE AUDIO XFMR
P/O TB1
RCV CHAN B 600 Ω
CT



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Audio Circuits, Block Diagram
Figure 5

SQUELCH control A2A2R10B-A2A2R10C enables/disables squelch and controls the squelch threshold level. In the full counterclockwise position, a ground squelch disables (squelch enable) signal is supplied through P2-27, J12-27, and J4-36 to the squelch output switch in receive audio A6, disabling squelch control. In any other position of the SQUELCH control, squelch switch A2A2R10C (switch) is open (squelch enable signal applied) and a squelch threshold signal is applied with maximum squelch threshold applied at full clockwise position. Squelch threshold level is controlled by A2A2R10B and supplied through P3-29, J12-29, and J4-47 to the squelch circuits in receive audio A6. Neither remote squelch nor phones squelch is available in the 851S-1.

Line audio is supplied by the line audio amplifiers in receive audio A6. Channel A line audio is supplied through a line audio transformer and J4-30, -31, -32 to TB1-1, -2, -3, respectively, for external use. TB1-1 to TB1-3 is a 600-Ω balanced output; TB1-2 is the transformer center tap. The channel A line audio output level can be set by adjusting A6R28.

Channel B line audio is supplied through a line audio transformer and J4-26, -54, -55 to TB1-4, -5, -6, respectively, for external use. TB1-4 to TB1-6 is a 600-Ω balanced output; TB1-5 is the transformer center tap. The channel B line audio output level can be set by adjusting A6R65.

2.2.3 IF/RF Gain Control (Refer to figure 6.)

If/rf gain of the 851S-1 Receiver is controlled by pin diode attenuators located along the signal path in the rf and if amplifiers. The attenuators are controlled by three gain control inputs:

a. AGC detector
b. Local (front panel) rf gain control
c. Remote rf gain control

The if/rf gain control circuits provide an output signal that is proportional to the gain reduction imposed by the gain control circuit. This signal is available on the rear panel of the receiver. This AGC signal line can be used to feed in an external gain control signal, such as when two receivers are cross-coupled for diversity operation.

Each of the channel A and channel B if amplifiers has an independent if AGC circuit so that, in ISB operation, the audio and if output signal levels of each if are independent of the signal levels in the opposite sideband. When the signal level in either if reaches a level approximately 20 dB above AGC threshold, an rf AGC voltage is fed to rf translator A9 through gating diodes.

The AGC circuit attack time is typically 2 to 5 ms, depending on the change in signal level. Decay times are selectable as 0.1 second (FAST), or 1.0 second (SLOW). A crowbar decay time is available and is 7 to 10 ms, for use when fast frequency hopping is used and the normal AGC decay time is too slow. The crowbar decay time is implemented only while using remote control. When enabled, the crowbar decay circuit is switched on for a period of 10 to 20 ms when a frequency control word is received. During this period of time, the receiver tunes to a new frequency and the AGC control voltage decays to the level of the signal at the new frequency, if it is lower. After the 10- to 20-ms period, the decay time reverts to the normal FAST or SLOW time selected.

When the receiver is using remote control with AGC disabled, if/rf gain is controlled by the remote rf gain input. This control voltage has the same sensitivity as the AGC output voltage (50 mV/dB) and originates in a d/a converter circuit in parallel output A12. The digital input to the d/a converter is a 5-bit binary signal (see remote control word format, table 1) that provides a total gain control range of 93 dB in 3-dB steps.

RF GAIN control A2A2R9 controls attenuation of pin diode attenuators in the if amplifiers and rf translator. The local rf gain output is from the wiper of A2A2R9 and applied through P3-26, J12-26, J6-39, and J5-39 to the channel A and channel B AGC amplifiers on channel A if A8 and channel B if A7. The remote rf gain output is supplied through J10-76, J6-39, and J5-39, and applied to the channel A and channel B AGC amplifiers (in remote controlled 851S-1 only).

AGC switch A2A2S12 controls the AGC decay time in the receiver. In the FAST position, a logic 1 signal is supplied from AGC switch A2A2S12 for channel A through P3-9, J12-9, and J6-32 to the AGC time constant switch in channel A if A8 and for channel B through P3-12, J12-12, and J5-32 to the AGC time constant switch in channel B if A7. In the FAST position, the AGC off signal is open-circuited and appears as a logic 0 signal. In the OFF position, a logic 1 signal is supplied from AGC switch A2A2S12 for channel A through P3-7, J12-7, and J6-4 to the AGC on/off switch in channel A if card A8 and for channel B if A7. In the OFF position, the AGC fast signal is open-circuited and appears as a logic 0 signal. In the SLOW

position, the AGC fast signal and AGC off signal are open-circuited and appear as logic 0 signals. The remote AGC fast signal for channel A is supplied through J10-85 and J6-32 to the AGC time constant switch in the channel A if (in remote controlled 851S-1 only) and for channel B is supplied through J10-20 and J5-32 to the AGC time constant switch in the channel B if (in remote controlled 851S-1 only).

*2.2.4 Frequency Control (Refer to figure 7.)**

The 851S-1 frequency is controlled by parallel bcd frequency inputs to the frequency synthesizer. These parallel bcd inputs are supplied by outputs from control A10 or from A12 (parallel output or preset). During local control from the front panel TUNING knob, during preset control (see paragraph 2.2A for a description of preset control operation) from preset A12, or during remote incremental tuning (see paragraph 2.3 for a description of remote control operation) from a control unit such as the HF-8095, the bcd inputs are supplied by control A10. During preset control the bcd inputs supplied by control A10 are stored in 16 (0-15) selectable channels in the preset A12 card. When selected these presets are then supplied as bcd inputs to the synthesizer. During remote control operation, when a discrete absolute frequency (remote control command word 1) is received from the controlling device (typically a processor), the remote frequency is stored in parallel output A12 which then supplies the bcd inputs to the synthesizer.

An optical tuning switch coupled to the front panel TUNING knob is used to encode TUNING knob direction and angular velocity. The tuning mechanism generates two square-wave pulse trains displaced in phase by 90°, with one train lagging or leading the other, depending upon direction of knob rotation. The pulse trains are generated from the interruption of two light beams by opaque lines screened around the periphery of a plastic disc, thru which the light beams pass. TUNING knob rotational direction is decoded by count/store assembly A2A4 from the phase relationship between clock A and clock B pulse trains, and the pulse frequency (TUNING knob rate) is converted to a 5-bit binary count value representative of the tuning rate. The 5-bit binary count value and the direction (up/down) signals are applied to control A10, where the count value is decoded by a programmable read-only memory (PROM), programmed to provided the desired tuning characteristics. The outputs of the PROM control a variable frequency clock generated by a programmable frequency divider and applied to a bcd up/down counter, whose outputs control the receiver synthesizer and receiver frequency display. With this frequency control scheme, any desired characteristic of receiver tuning response versus TUNING knob rotational velocity can be obtained by appropriately programming the PROM. Tuning response in the 851S-1 is approximately linear for slow knob rotation and becomes somewhat exponential as TUNING knob rotation speed is increased.

Incremental remote control tuning of the 851S-1 (such as effected by an HF-8095 control unit) is accomplished in a similar fashion, except that the 5-bit binary count value and up/down direction signals are received in serial form in remote command word 4 (see paragraph 2.3) by serial interface A13, stored in parallel output A12, and applied to control A10 to control the receiver frequency as described above (in remote operation, outputs from the local count/store assembly A2A4 are disabled and outputs from parallel output A12 are enabled).

The receiver DIAL switch is used in conjunction with the TUNING knob to select between COARSE and FINE tuning modes, or to lock to the present frequency by disabling the tuning mechanism in the LOCK position. In the COARSE tuning mode, the bcd up/down frequency counter is clocked from the 10 kHz digit (with the lower order frequency digits remaining unchanged) to permit fast changes over large frequency ranges. In the FINE tune mode, the bcd counter is clocked from the lowest order digit to provide slower tuning across narrower frequency ranges.

Parallel 1-kHz to 20-MHz bcd frequency control lines are also supplied through buffer/drivers in control A10, through J8 and P7 to J46, through rfi filters to preselector connector J16. The parallel bcd inputs supplied at J8 are also band decoded, and band signals are supplied from J8 to J7 and rf translator A9.

Parallel bcd frequency inputs supplied to P11 are supplied through P11 to the appropriate decade on the synthesizer sideboard. 1-Hz bcd inputs are supplied through A23J3 to end decade A16 (1-Hz tuning only). 10-Hz bcd inputs are supplied through A23J4 to 10-Hz decade A17(1-Hz tuning only) or end decade A17 (10-Hz tuning only). 100-Hz bcd inputs are supplied through A23J5 to 100-Hz decade A18 (1-Hz and 10-Hz tuning) or end decade A18 (100-Hz tuning only). 1-kHz bcd inputs are supplied through A23J6 to 1-kHz decade A19. 10-kHz bcd inputs are supplied through

*A US patent has been applied for covering the circuits and methods used to control the receiver frequency locally or remotely, as described here.

A23J7 to 10-kHz decade A20. 100-kHz bcd inputs are supplied through A23J8 to 100-kHz decade A21. 1-MHz and 10-MHz bcd inputs are supplied through A23J9 to synthesizer output A22.

Refer to paragraph 2.4 for frequency synthesizer operation.

*2.2.5 VBFO Control (Refer to figure 7.)**

The vbfo offset frequency is controlled in a manner similar to that described for the receiver frequency control in paragraph 2.2.4. The vbfo offset frequency is controlled by a 3-digit bcd up/down counter and associated sign bit on vbfo A4. During local control from the front panel TUNING knob, or during remote incremental tuning of the vbfo offset frequency from a remote control unit such as the HF-8095, the 3-digit bcd up/down counter on vbfo A4 supplies the bcd control of the vbfo synthesizer on A4. During remote control operation, when a discrete absolute vbfo offset frequency (remote control command word 3) is received from the controlling device (typically a processor), the remote bcd offset frequency and sign bit are stored in parallel output A12, which then supplies the sign and bcd digits to vbfo A4 to control the vbfo synthesizer.

Many of the same circuits used to control the receiver rf tuning as described in paragraph 2.2.4 are also used to control the tuning of the vbfo offset frequency. When the front panel bfo switch is placed in the TUNE position, the TUNING knob may be used to control the vbfo offset frequency. Output pulses from the optical tuning switch are again applied to count/store assembly A2A4 where knob direction is decoded and tuning rate is encoded into a 5-bit binary count value. The tuning direction (up/down) and tuning rate (5-bit count) outputs from A2A4 are applied to control A10 where the 5-bit count value is again converted to clock frequency by the tuning rate decoder PROM and programmable frequency divider on A10. At this point, however, the clock pulses are not applied to the bcd up/down counter on A10 but are routed and applied to the bcd up/down counter located on vbfo A4. Here the pulses are used to clock the vbfo bcd up/down counter whose outputs control the vbfo synthesizer on A4.

Remote incremental tuning of the vbfo (such as effected by an HF-8095 control unit) is accomplished in a similar fashion, except that the 5-bit binary count value and up/down direction signals are received in serial form in remote command word 4 (see paragraph 2.3) by serial interface A13, stored in parallel output A12, and applied to control A10 to control the vbfo offset frequency as described above for local tuning. In remote operation, outputs from the local count/store assembly A2A4 are disabled and outputs from parallel output A12 are enabled.

When tuning the vbfo, the FINE and COARSE positions of the DIAL switch have no effect on vbfo tuning. The LOCK position of the switch may be used, however, to disable the tuning mechanism.

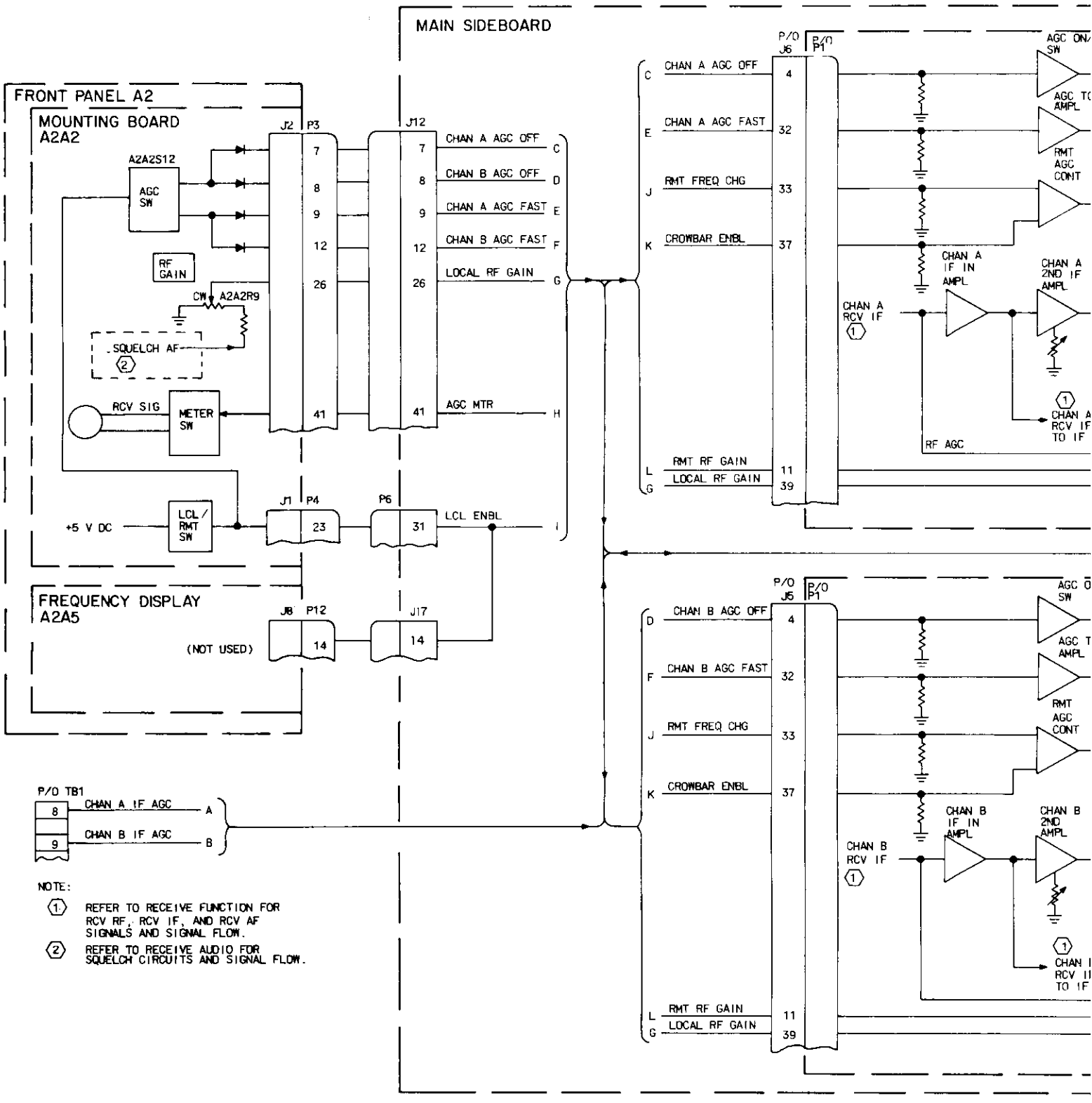
The vbfo offset frequency is controlled by the BFO switch, DIAL switch, and TUNING knob on the front panel. The vbfo offset is summed with the 450-kHz base if frequency in the channel A if line. When the DIAL switch is in COARSE or FINE position and the BFO switch is in the TUNE position, varying the TUNING knob will vary the VBFO OFFSET HZ. The direction the TUNING knob is turned determines the direction of the offset frequency (that is, ccw = negative, cw = positive). If the sign is + (plus), the vbfo offset is added to the 450-kHz if; for example: +9990-Hz vbfo offset equals (450 kHz plus 9990 Hz or) 459.990-kHz if frequency. Likewise, if the sign is - (minus), the vbfo offset is subtracted from the 450-kHz if; for example: -9990-Hz vbfo offset equals (450 kHz minus 9990 Hz or) 440.010-kHz if frequency. When the desired bfo offset is reached, setting the BFO switch to HOLD will hold the bfo frequency at the indicated offset.

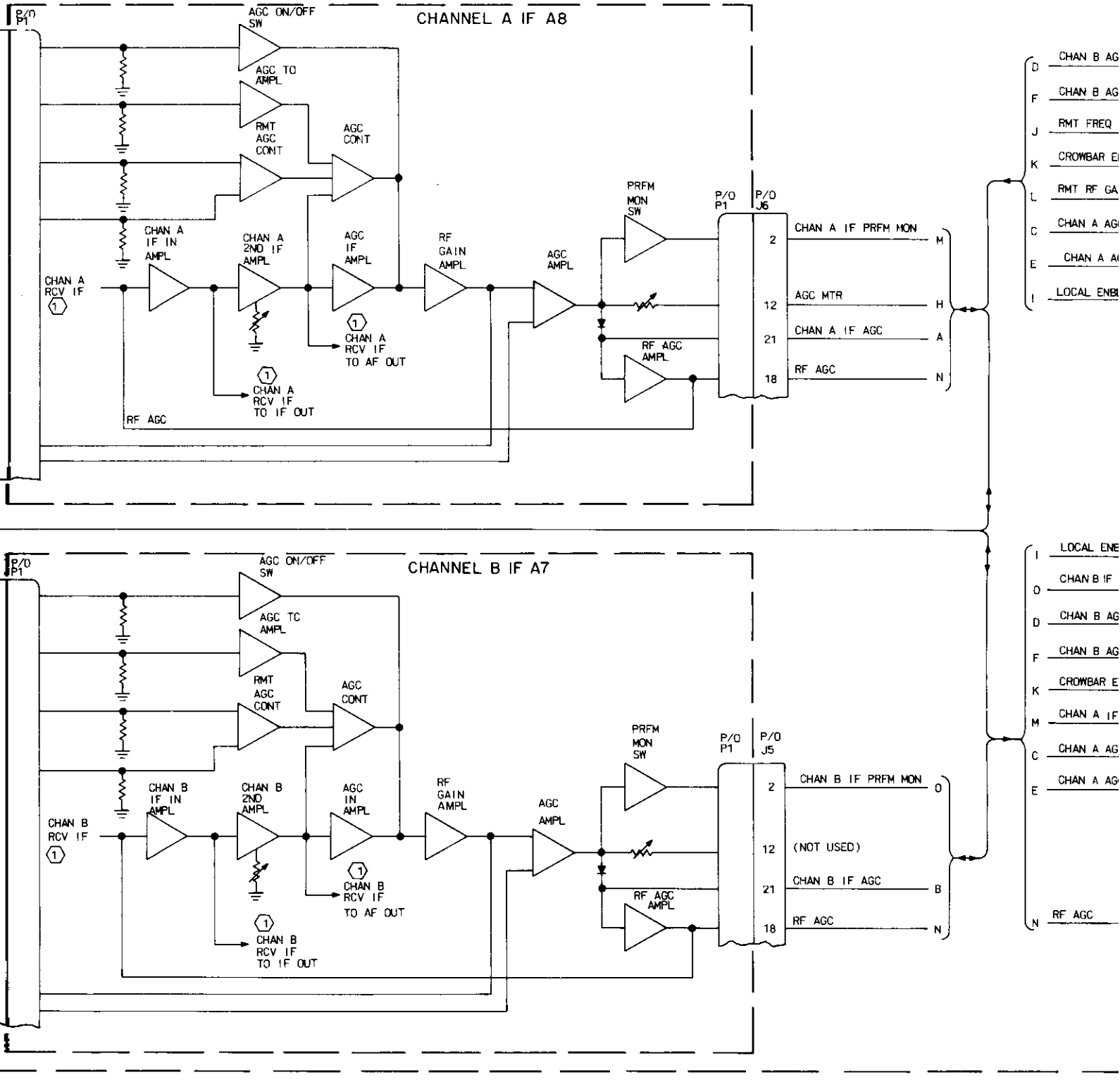
2.2.4 Preset Control (Refer to figure 7A.)

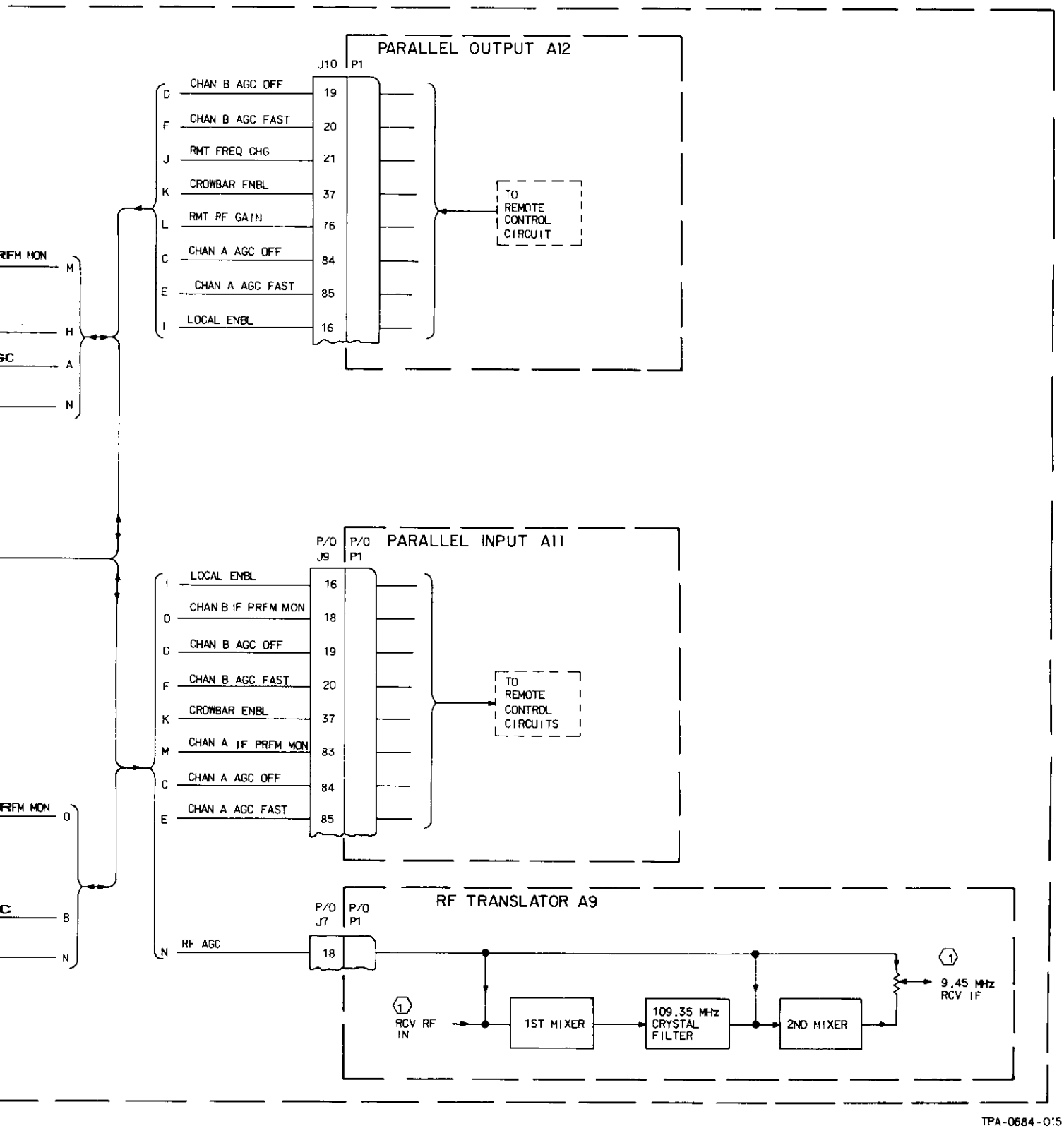
The 851S-1 Receiver is adaptable to preset control using a preset A12 card. Note that when an 851S-1 Receiver is adapted for preset operation it cannot be adapted for remote control. If a remote control receiver is used, the preset function can be implemented in the remote control.

When preset control is enabled, up to 16 channels of preset information can be stored and/or used. With front panel CONT switch in PSET position preset operation is enabled, a logic 1 is applied to preset enable input through A2A2J1-22, A2A4J1-22, P4-22, P6-30, and J10-80 to preset A12. With the PRESET switch in the OPER position (and preset enabled), the information stored in the channel selected by the PRESET-CHANNEL selector is used to set frequency, mode, and filter enable. After a channel is selected, the receiver front panel controls have direct control until the PRESET-CHANNEL selector is changed. If a frequency, mode, or filter selection other than what is selected by the preset channel, that

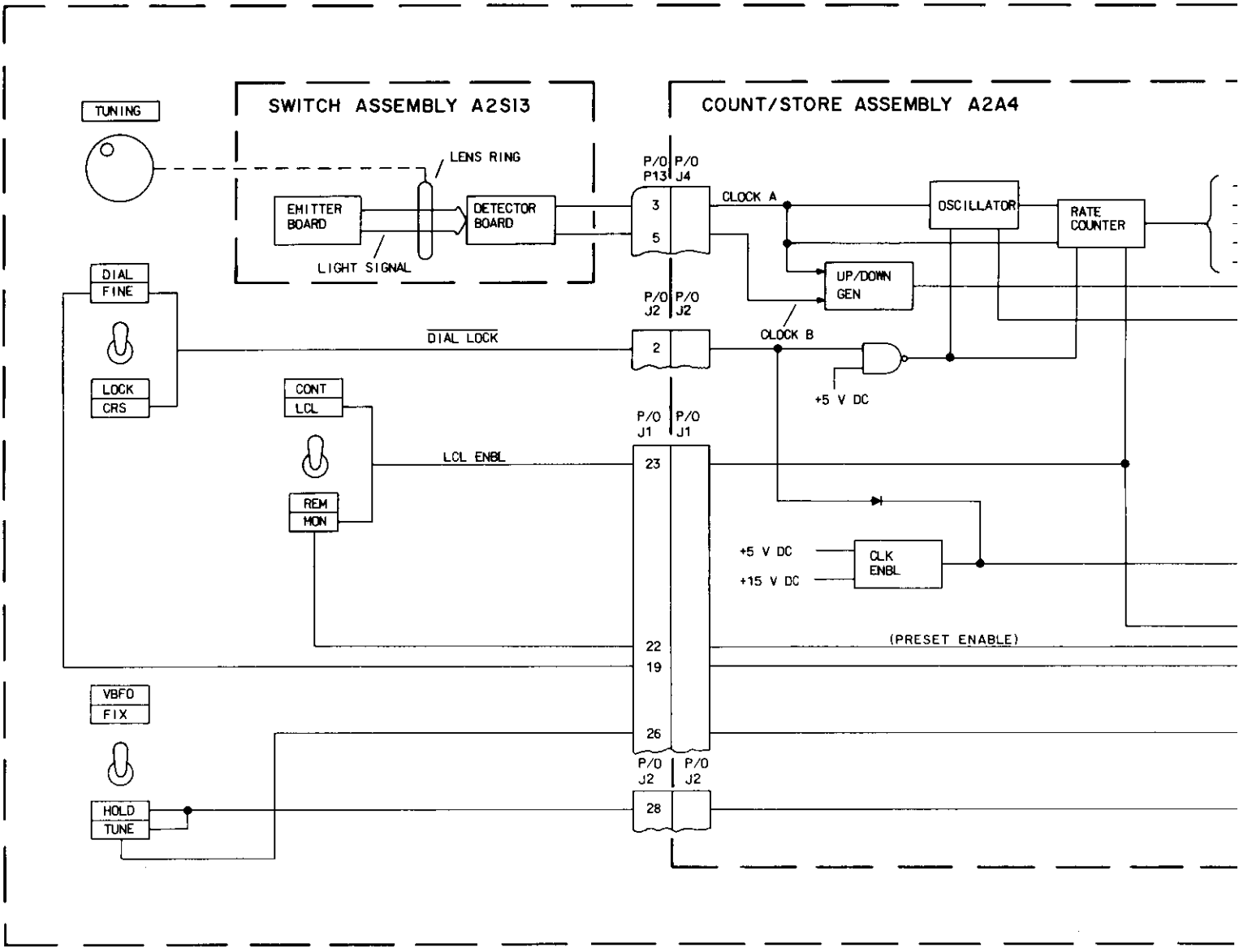
*A US patent has been applied for covering the circuits and methods used to control the receiver frequency locally or remotely, as described here.


MAIN SIDEBOARD
FRONT PANEL A2
MOUNTING BOARD A2A2
A2A2S12
AGC SW
RF GAIN
CW
A2A2R9
SQUELCH AF
2
RCV SIG
METER SW
+5 V DC
LCL / RMT SW
J2
P3
J12
J1
P4
P6
J8
P12
J17
FREQUENCY DISPLAY A2A5
(NOT USED)
CHAN A AGC OFF
CHAN B AGC OFF
CHAN A AGC FAST
CHAN B AGC FAST
LOCAL RF GAIN
AGC MTR
LCL ENBL
P/O J6
P/O P1
RMT FREQ CHG
CROWBAR ENBL
RMT RF GAIN
CHAN A IF IN AMPL
CHAN A 2ND IF AMPL
CHAN A RCV IF
1
RF AGC
P/O J5
CHAN B IF IN AMPL
CHAN B 2ND AMPL
CHAN B RCV IF
P/O TB1
CHAN A IF AGC
CHAN B IF AGC
NOTE:
1 REFER TO RECEIVE FUNCTION FOR RCV RF, RCV IF, AND RCV AF SIGNALS AND SIGNAL FLOW.
2 REFER TO RECEIVE AUDIO FOR SQUELCH CIRCUITS AND SIGNAL FLOW.


CHANNEL A IF A8
P/O P1
AGC ON/OFF SW
AGC TO AMPL
RMT AGC CONT
AGC CONT
CHAN A IF IN AMPL
CHAN A 2ND IF AMPL
AGC IF AMPL
RF GAIN AMPL
AGC AMPL
PRFM MON SW
P/O P1
P/O J6
CHAN A RCV IF
1
CHAN A RCV IF TO AF OUT
CHAN A RCV IF TO IF OUT
RF AGC
RF AGC AMPL
2
CHAN A IF PRFM MON
M
12
AGC MTR
H
21
CHAN A IF AGC
A
18
RF AGC
N
D
CHAN B AG
F
CHAN B AG
J
RMT FREQ
K
CROWBAR E
L
RMT RF GA
C
CHAN A AG
E
CHAN A A
I
LOCAL ENB
CHANNEL B IF A7
P/O P1
AGC ON/OFF SW
AGC TO AMPL
RMT AGC CONT
AGC CONT
CHAN B IF IN AMPL
CHAN B 2ND AMPL
AGC IN AMPL
RF GAIN AMPL
AGC AMPL
PRFM MON SW
P/O P1
P/O J5
CHAN B RCV IF
1
CHAN B RCV IF TO AF OUT
CHAN B RCV IF TO IF OUT
RF AGC AMPL
2
CHAN B IF PRFM MON
O
12
(NOT USED)
21
CHAN B IF AGC
B
18
RF AGC
N
I
LOCAL ENE
O
CHAN B IF
D
CHAN B AG
F
CHAN B AG
K
CROWBAR E
M
CHAN A IF
C
CHAN A AG
E
CHAN A AG
N
RF AGC

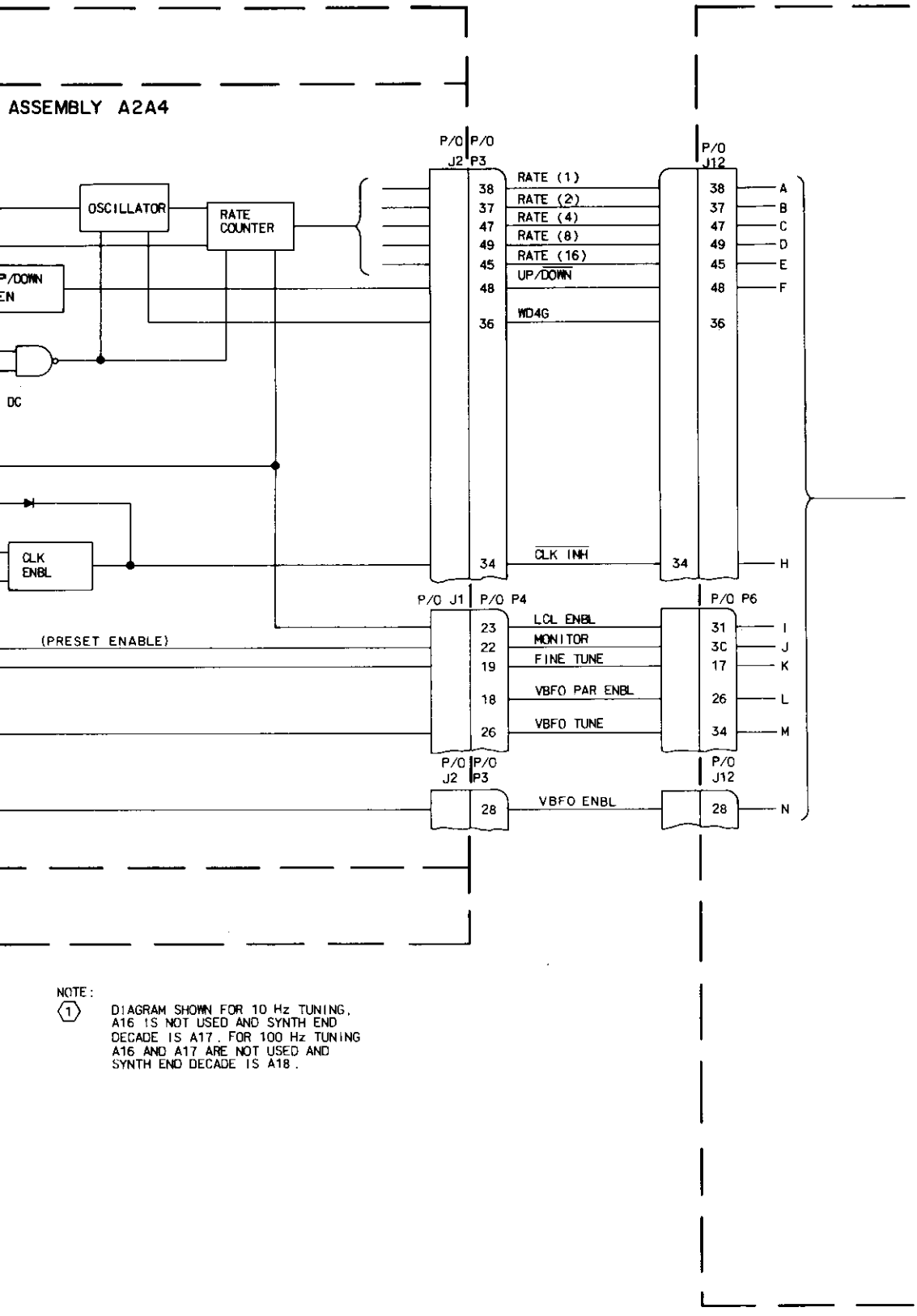


IF/RF Gain Control, Block Diagram
Figure 6



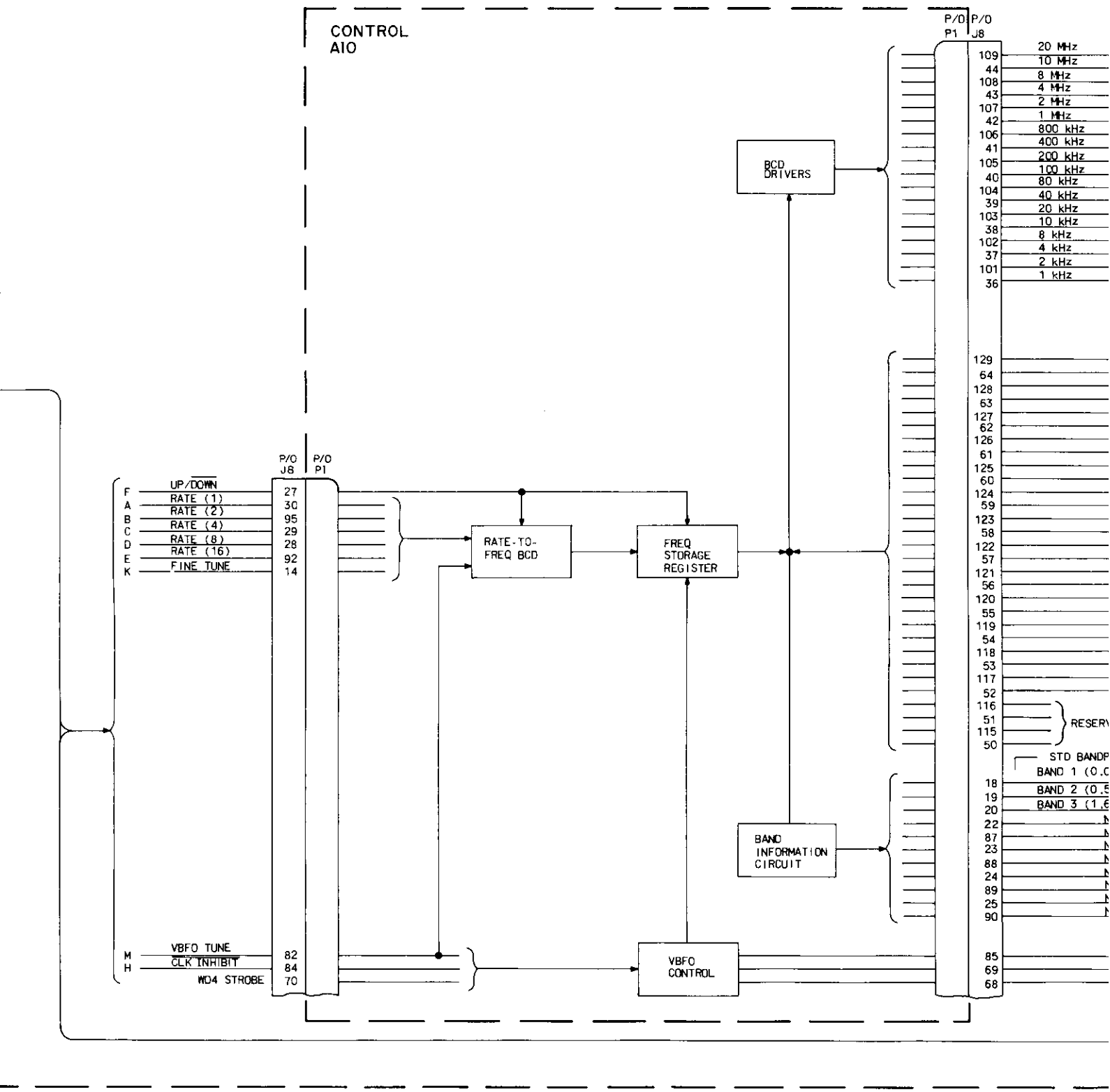
NOTE:

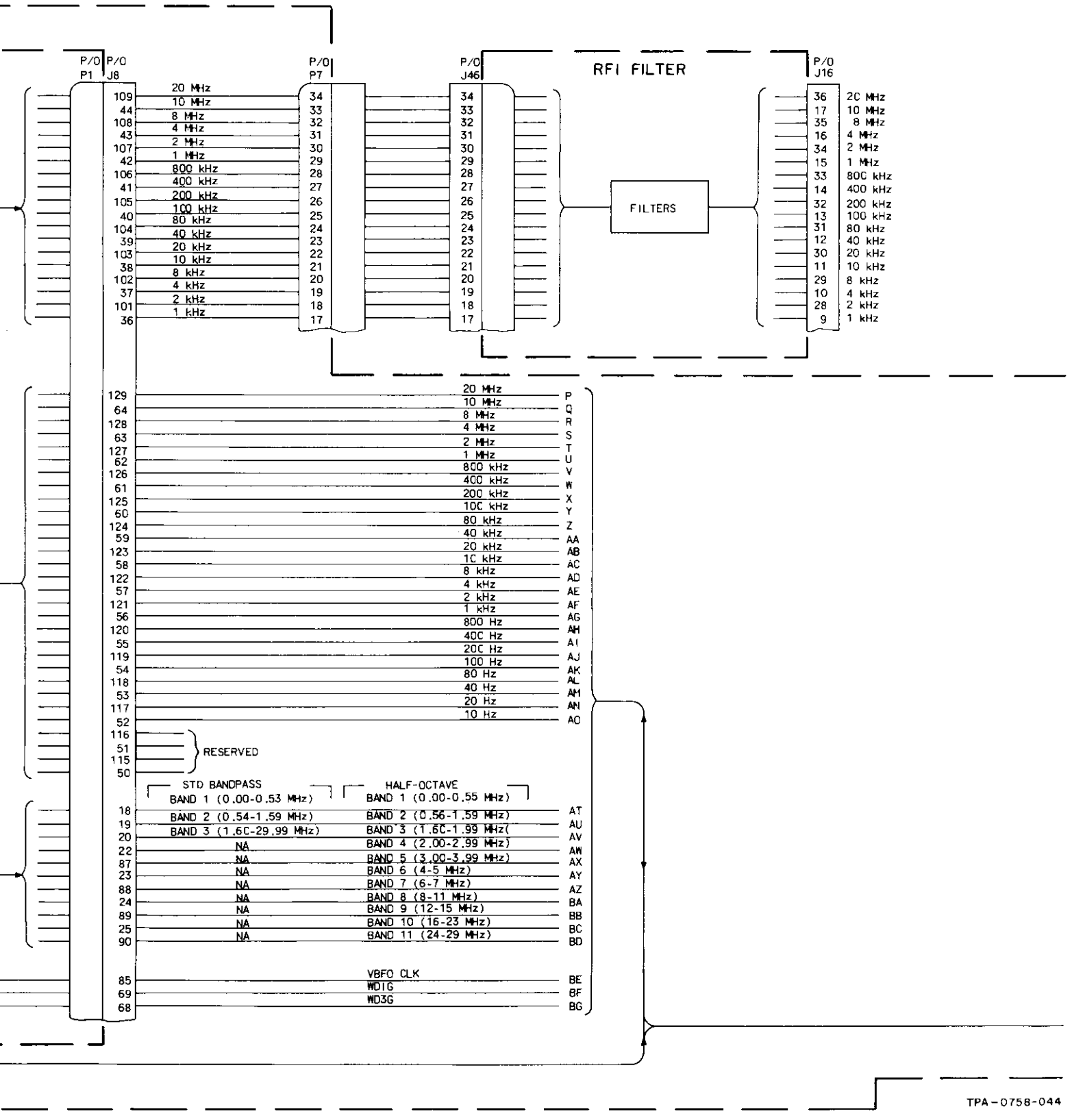
(1) DIAGRAM SHOWN FOR 10 Hz TUNING, A16 IS NOT USED AND SYNTH END DECADE IS A17. FOR 100 Hz TUNING A16 AND A17 ARE NOT USED AND SYNTH END DECADE IS A18.



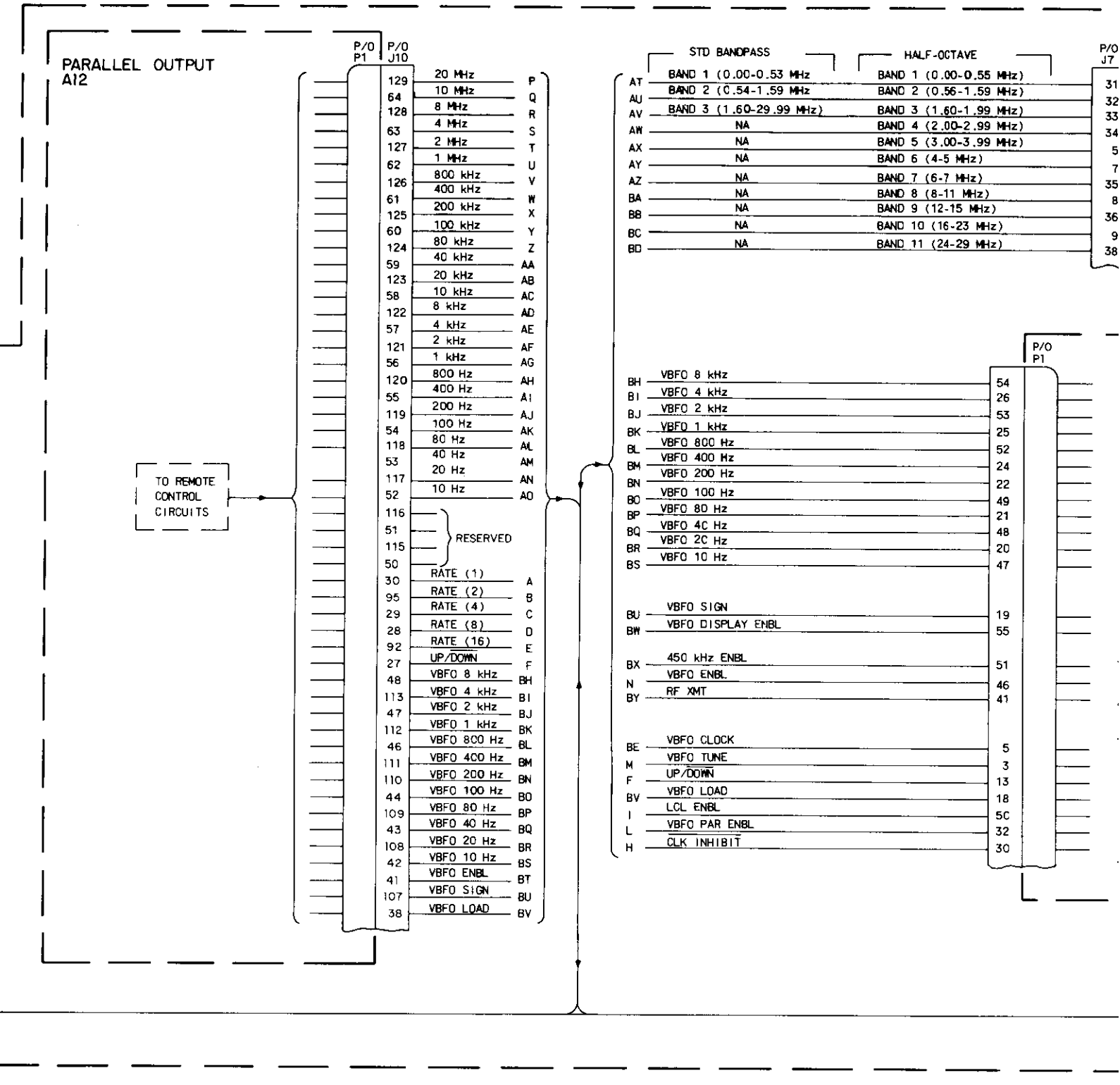
NOTE:
(1) DIAGRAM SHOWN FOR 10 Hz TUNING. A16 IS NOT USED AND SYNTH END DECADE IS A17. FOR 100 Hz TUNING A16 AND A17 ARE NOT USED AND SYNTH END DECADE IS A18.

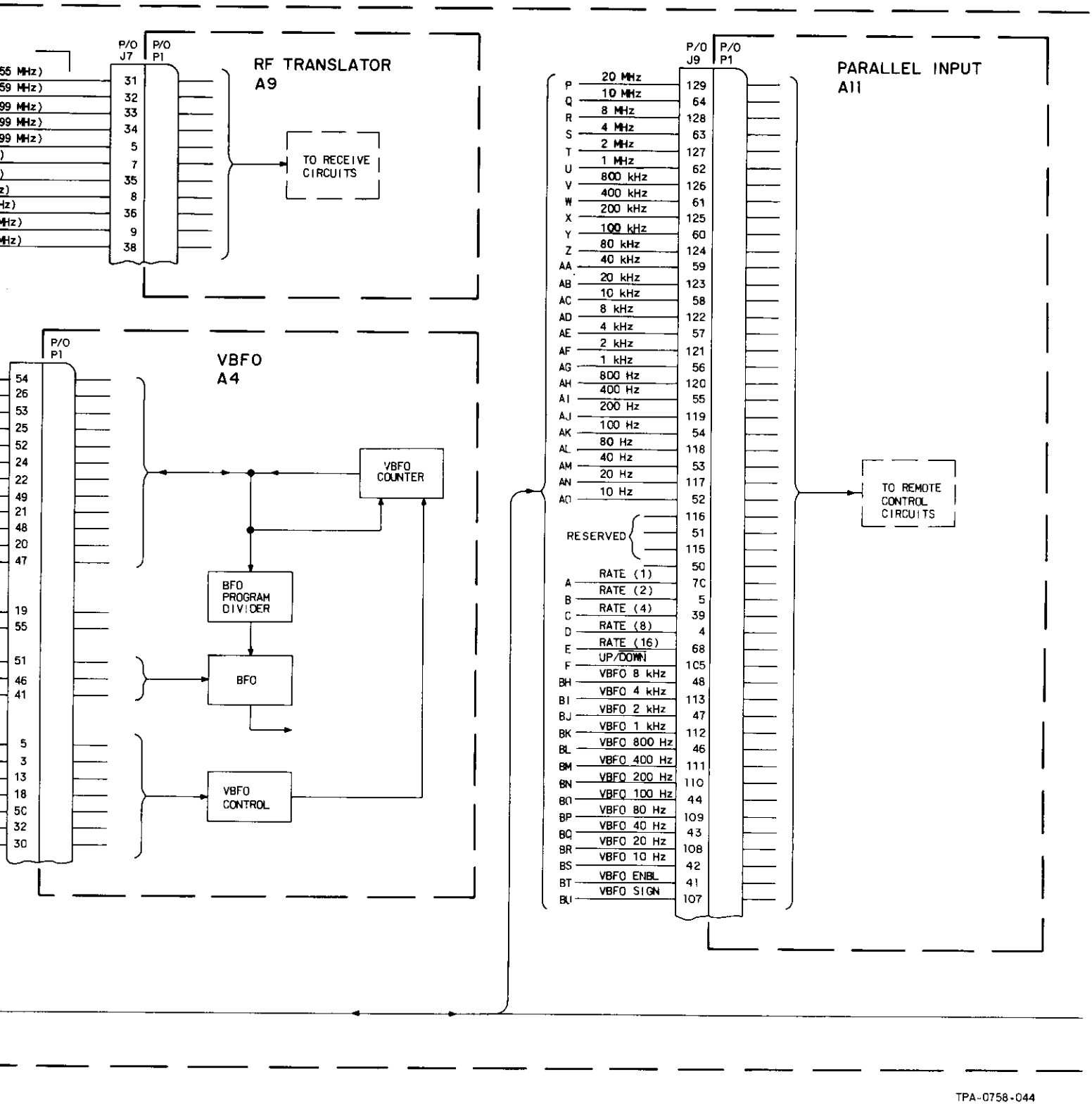
Frequency Control, Block Diagram
Figure 7 (Sheet 1 of 4)


CONTROL
A10
P/O J8
P/O P1
F UP/DOWN 27
A RATE (1) 30
B RATE (2) 95
C RATE (4) 29
D RATE (8) 28
E RATE (16) 92
K FINE TUNE 14
RATE-TO-FREQ BCD
FREQ STORAGE REGISTER
BCD DRIVERS
BAND INFORMATION CIRCUIT
M VBFO TUNE 82
H CLK INHIBIT 84
WD4 STROBE 70
VBFO CONTROL
P/O P1
P/O J8
20 MHz 109
10 MHz 44
8 MHz 108
4 MHz 43
2 MHz 107
1 MHz 42
800 kHz 106
400 kHz 41
200 kHz 105
100 kHz 40
80 kHz 104
40 kHz 39
20 kHz 103
10 kHz 38
8 kHz 102
4 kHz 37
2 kHz 101
1 kHz 36
129
64
128
63
127
62
126
61
125
60
124
59
123
58
122
57
121
56
120
55
119
54
118
53
117
52
116
51
115
50
RESERV
STD BANDP
BAND 1 (0.0
BAND 2 (0.5
BAND 3 (1,6
18
19
20
22
87
23
88
24
89
25
90
85
69
68

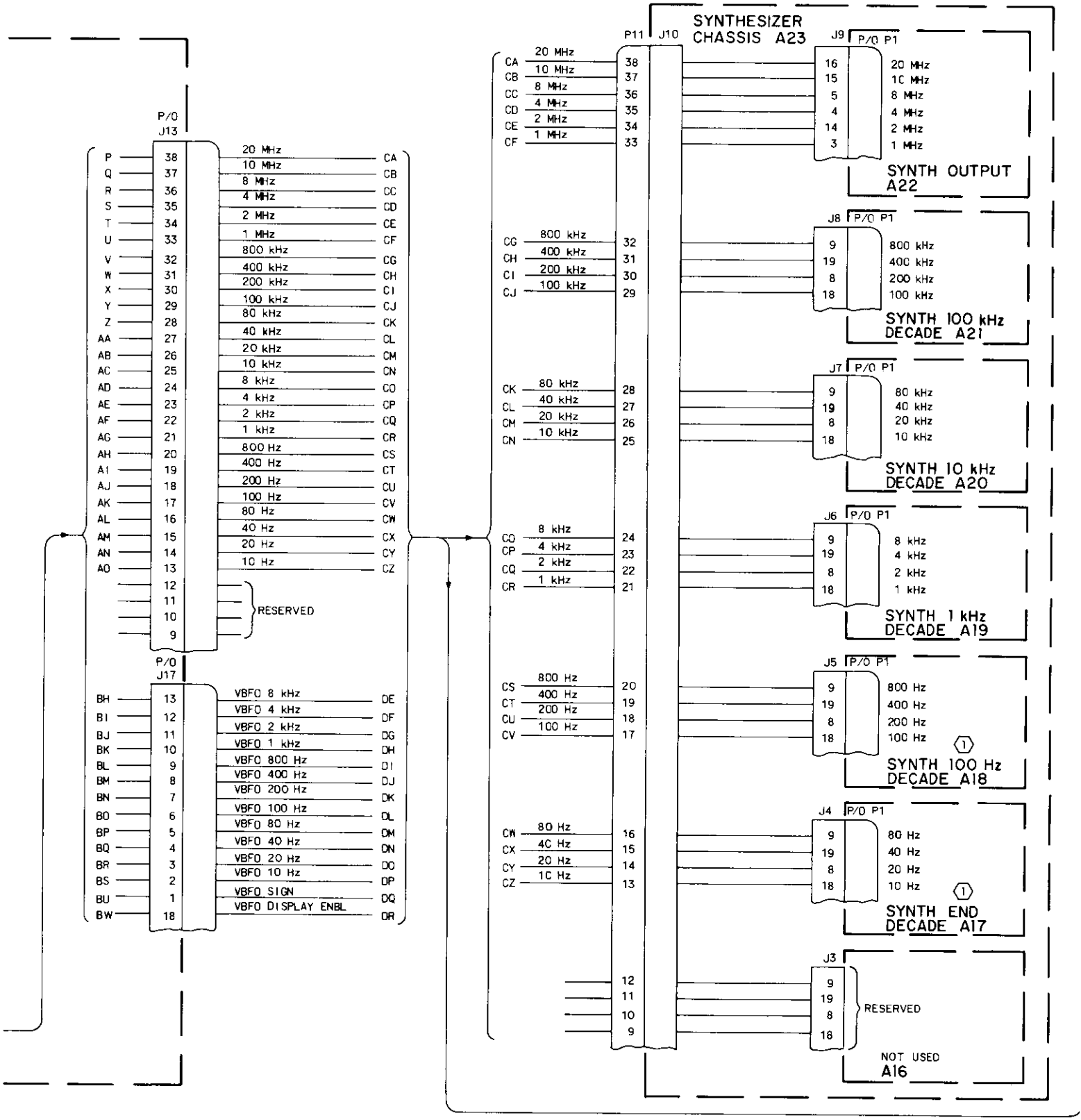


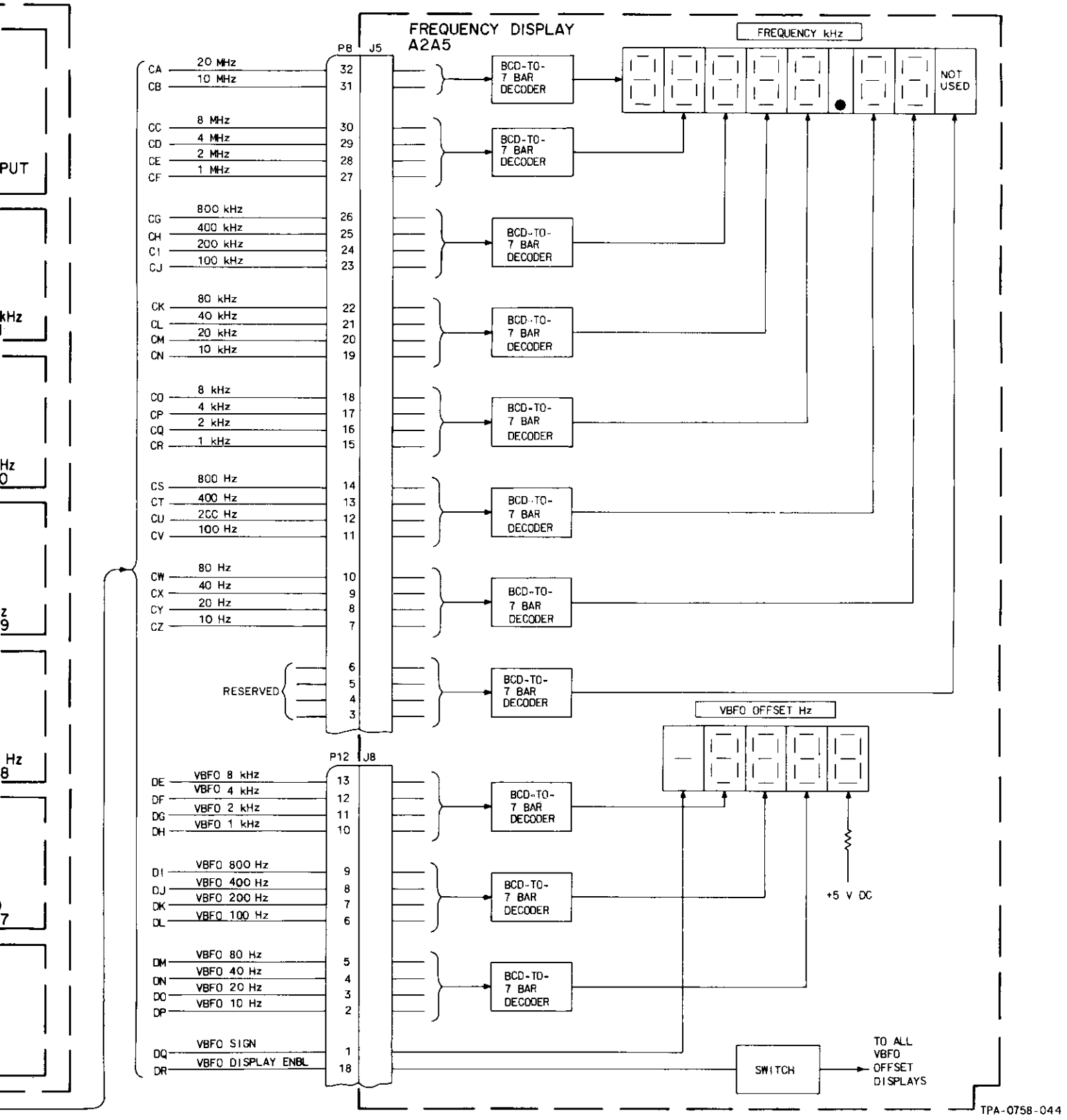
Frequency Control, Block Diagram
Figure 7 (Sheet 2)


PARALLEL OUTPUT
A12
P/O P1
P/O J10
TO REMOTE CONTROL CIRCUITS
20 MHz P
10 MHz Q
8 MHz R
4 MHz S
2 MHz T
1 MHz U
800 kHz V
400 kHz W
200 kHz X
100 kHz Y
80 kHz Z
40 kHz AA
20 kHz AB
10 kHz AC
8 kHz AD
4 kHz AE
2 kHz AF
1 kHz AG
800 Hz AH
400 Hz AI
200 Hz AJ
100 Hz AK
80 Hz AL
40 Hz AM
20 Hz AN
10 Hz AO
RESERVED
RATE (1) A
RATE (2) B
RATE (4) C
RATE (8) D
RATE (16) E
UP/DOWN F
VBFO 8 kHz BH
VBFO 4 kHz BI
VBFO 2 kHz BJ
VBFO 1 kHz BK
VBFO 800 Hz BL
VBFO 400 Hz BM
VBFO 200 Hz BN
VBFO 100 Hz BO
VBFO 80 Hz BP
VBFO 40 Hz BQ
VBFO 20 Hz BR
VBFO 10 Hz BS
VBFO ENBL BT
VBFO SIGN BU
VBFO LOAD BV
STD BANDPASS
HALF-OCTAVE
P/O J7
BAND 1 (0.00-0.53 MHz)
BAND 2 (0.54-1.59 MHz)
BAND 3 (1.60-29.99 MHz)
BAND 1 (0.00-0.55 MHz)
BAND 2 (0.56-1.59 MHz)
BAND 3 (1.60-1.99 MHz)
BAND 4 (2.00-2.99 MHz)
BAND 5 (3.00-3.99 MHz)
BAND 6 (4-5 MHz)
BAND 7 (6-7 MHz)
BAND 8 (8-11 MHz)
BAND 9 (12-15 MHz)
BAND 10 (16-23 MHz)
BAND 11 (24-29 MHz)
NA
P/O P1
VBFO 8 kHz
VBFO 4 kHz
VBFO 2 kHz
VBFO 1 kHz
VBFO 800 Hz
VBFO 400 Hz
VBFO 200 Hz
VBFO 100 Hz
VBFO 80 Hz
VBFO 40 Hz
VBFO 20 Hz
VBFO 10 Hz
VBFO SIGN
VBFO DISPLAY ENBL
450 kHz ENBL
VBFO ENBL
RF XMT
VBFO CLOCK
VBFO TUNE
UP/DOWN
VBFO LOAD
LCL ENBL
VBFO PAR ENBL
CLK INHIBIT

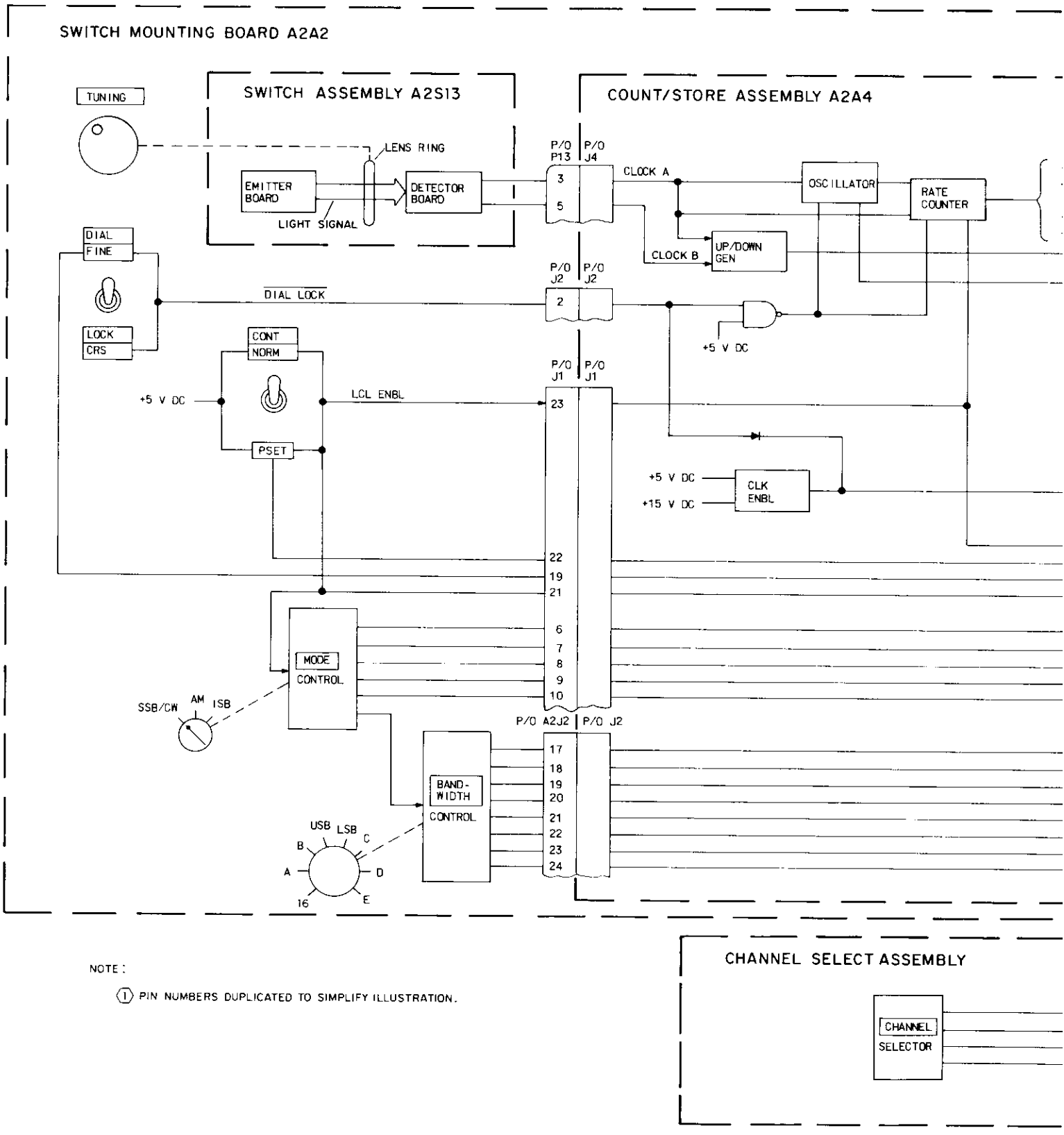


Frequency Control, Block Diagram
Figure 7 (Sheet 3)


SYNTHESIZER
CHASSIS A23
P/O J13
P11
J10
J9 P/O P1
J8 P/O P1
J7 P/O P1
J6 P/O P1
J5 P/O P1
J4 P/O P1
J3
P/O J17
SYNTH OUTPUT A22
SYNTH 100 kHz DECADE A21
SYNTH 10 kHz DECADE A20
SYNTH 1 kHz DECADE A19
SYNTH 100 Hz DECADE A18
SYNTH END DECADE A17
NOT USED A16
RESERVED
RESERVED
VBFO 8 kHz
VBFO 4 kHz
VBFO 2 kHz
VBFO 1 kHz
VBFO 800 Hz
VBFO 400 Hz
VBFO 200 Hz
VBFO 100 Hz
VBFO 80 Hz
VBFO 40 Hz
VBFO 20 Hz
VBFO 10 Hz
VBFO SIGN
VBFO DISPLAY ENBL
20 MHz
10 MHz
8 MHz
4 MHz
2 MHz
1 MHz
800 kHz
400 kHz
200 kHz
100 kHz
80 kHz
40 kHz
20 kHz
10 kHz
8 kHz
4 kHz
2 kHz
1 kHz
800 Hz
400 Hz
200 Hz
100 Hz
80 Hz
40 Hz
20 Hz
10 Hz

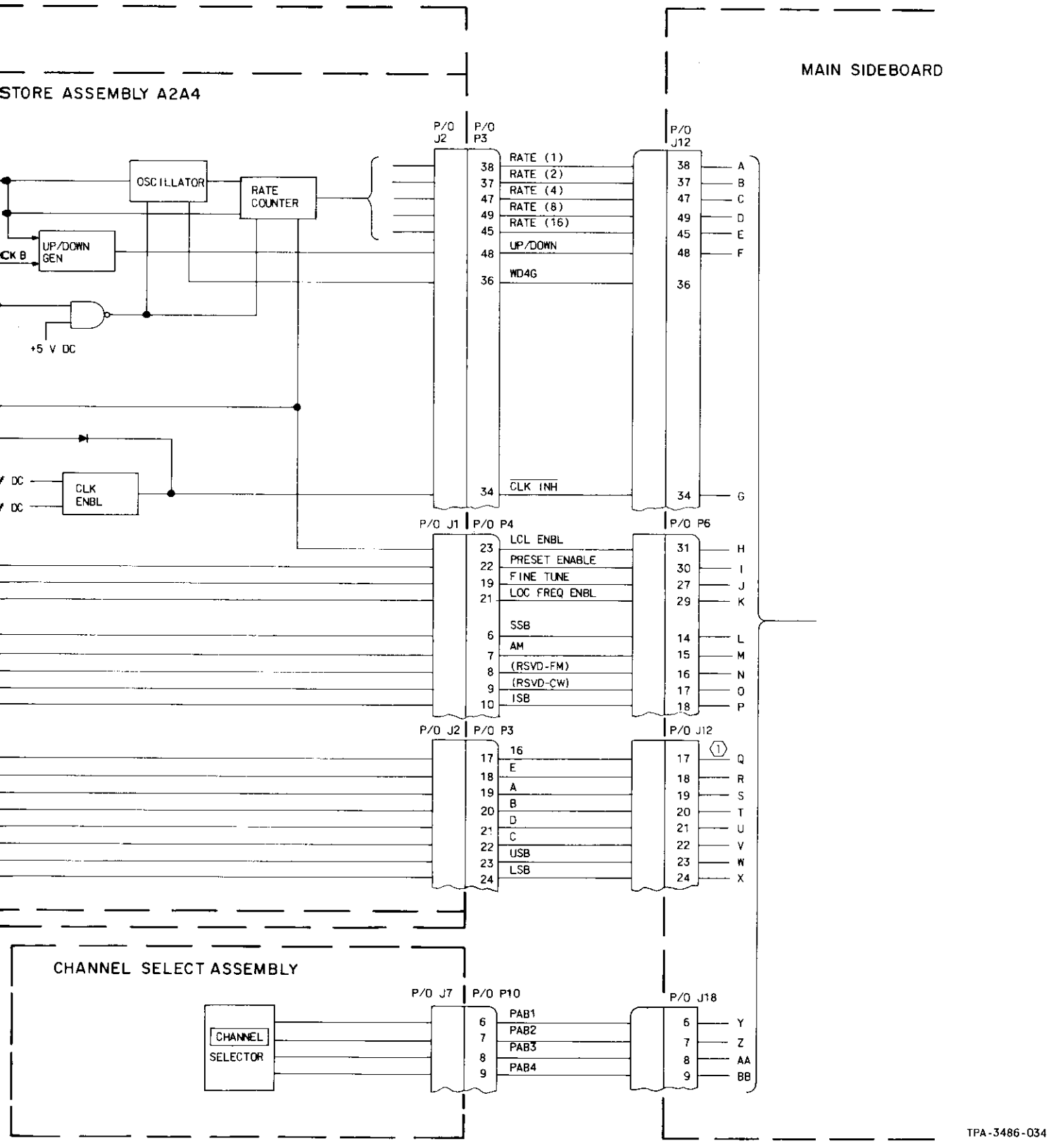


Frequency Control, Block Diagram
Figure 7 (Sheet 4)

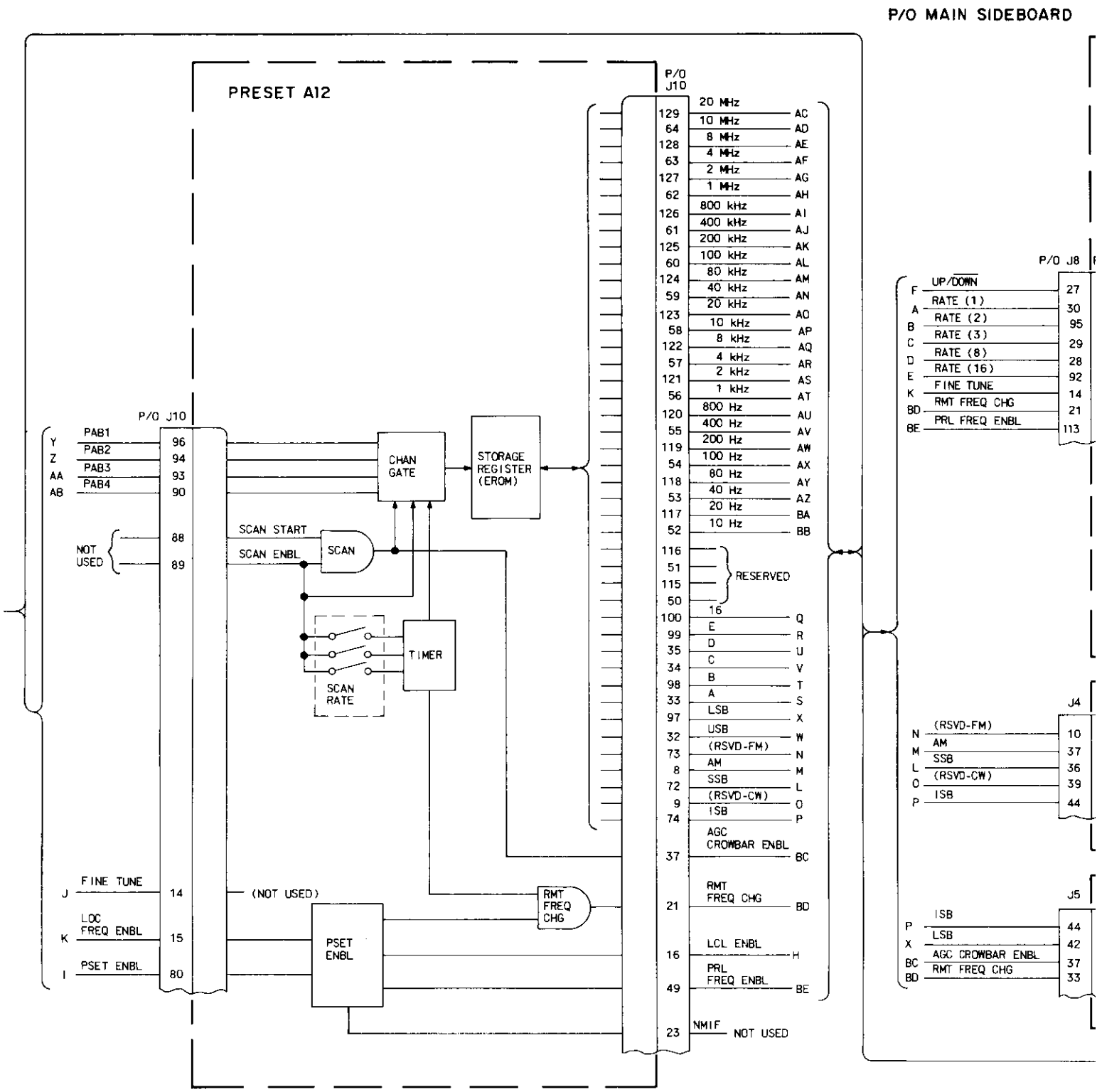


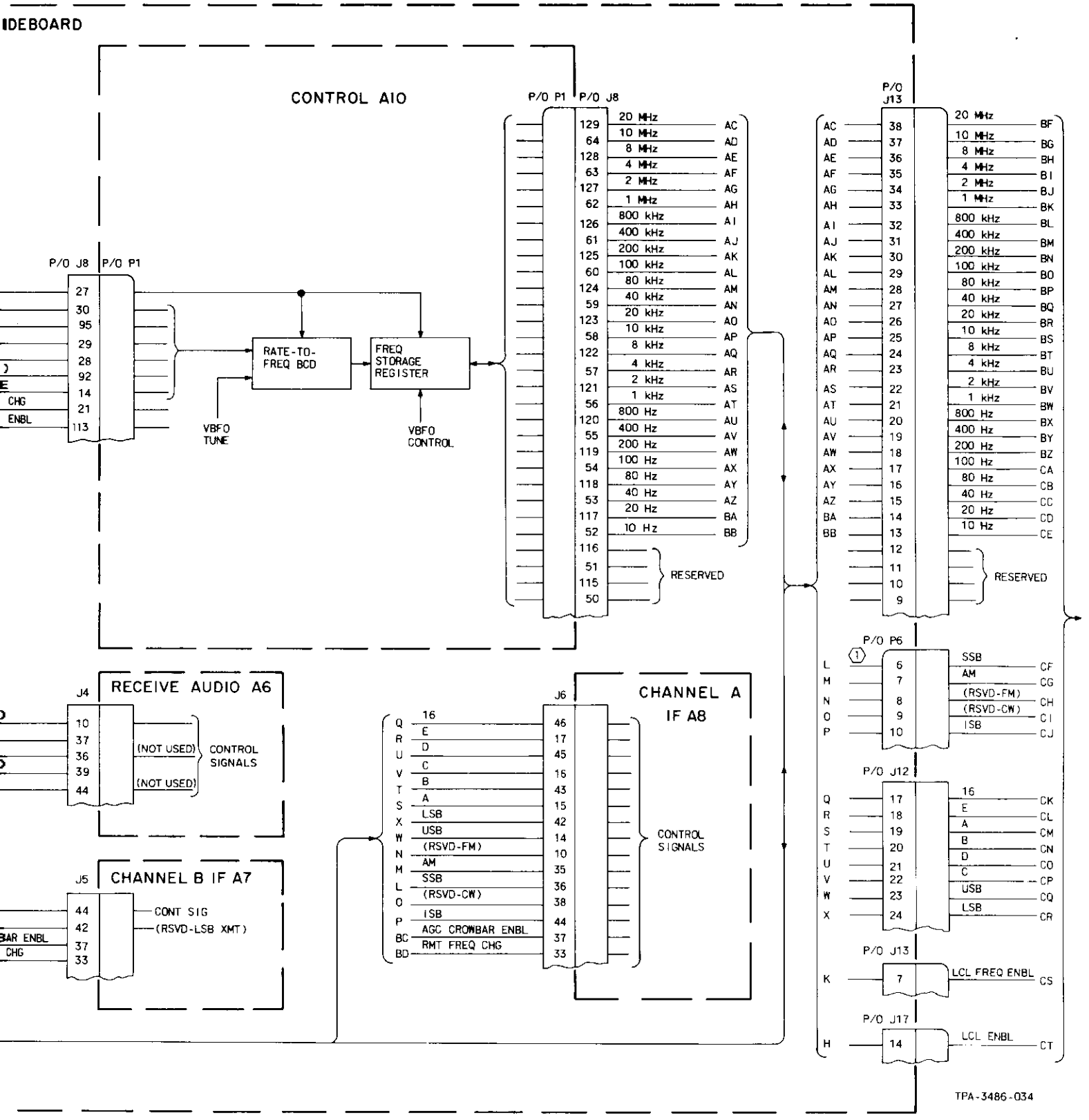
NOTE :

(1) PIN NUMBERS DUPLICATED TO SIMPLIFY ILLUSTRATION.

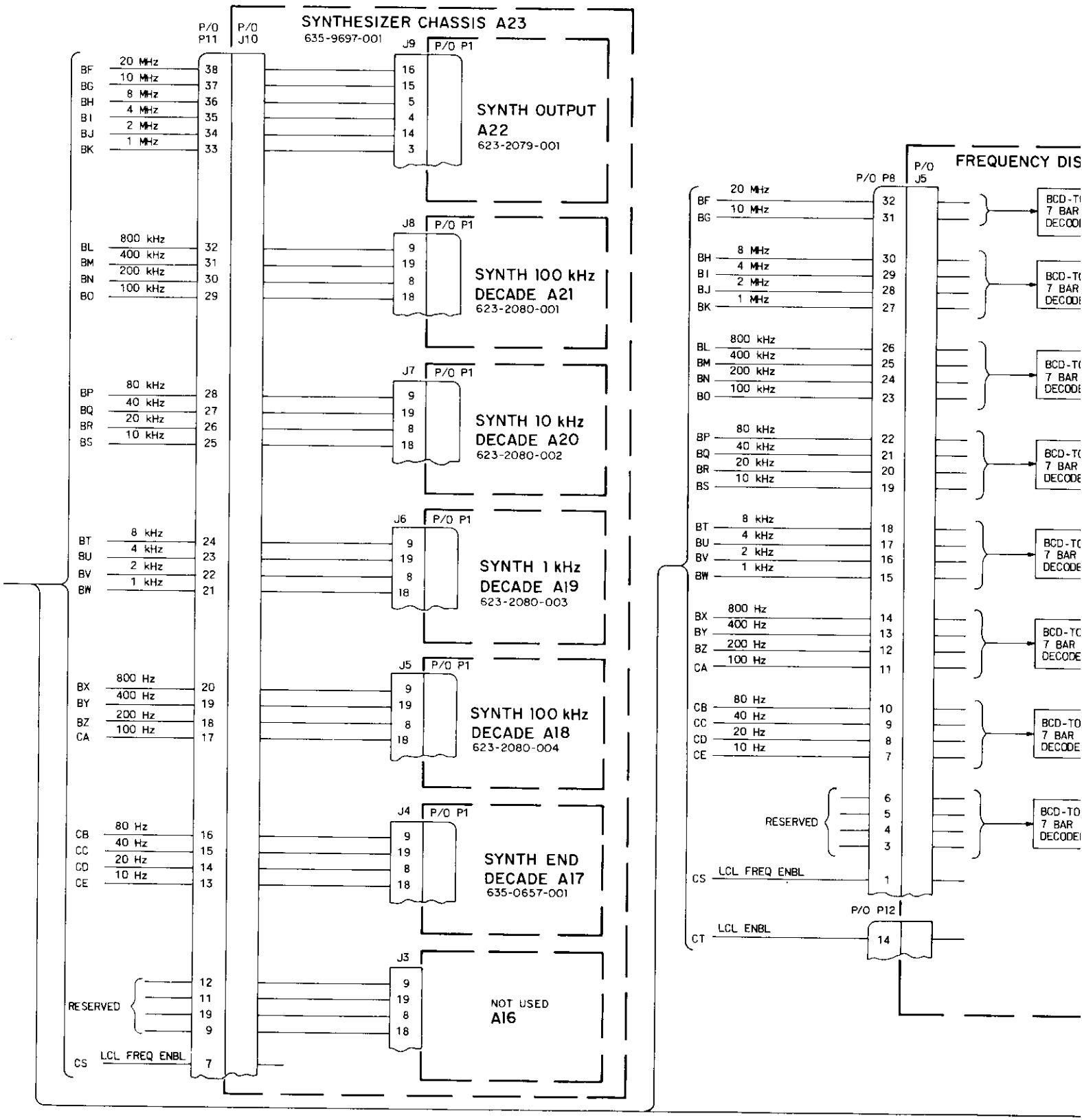


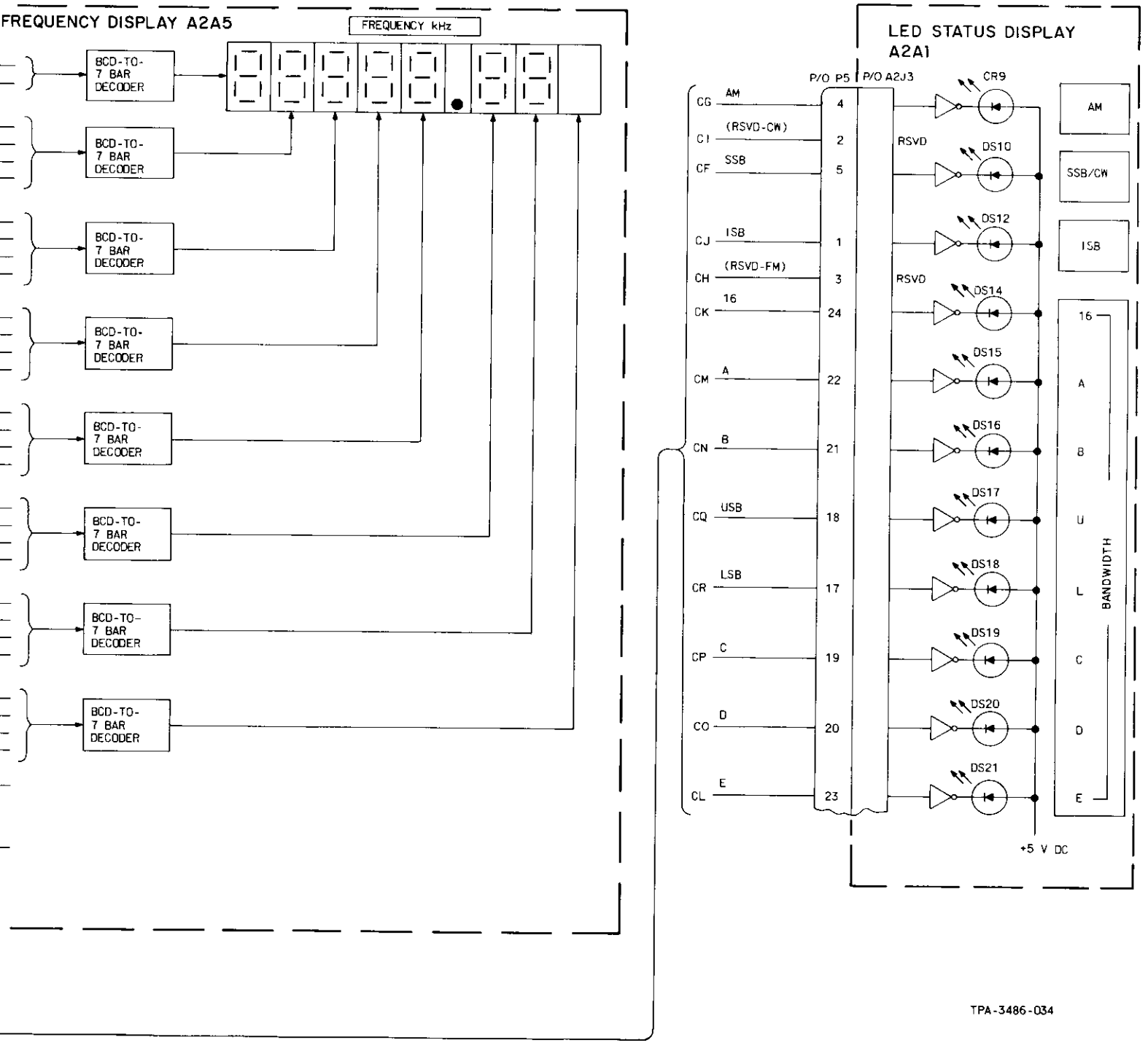
Preset Control, Block Diagram
Figure 7A (Sheet 1 of 3)


P/O MAIN SIDEBOARD
PRESET A12
P/O J10
P/O J8
J4
J5
PAB1
PAB2
PAB3
PAB4
NOT USED
CHAN GATE
STORAGE REGISTER (EROM)
SCAN START
SCAN ENBL
SCAN
TIMER
SCAN RATE
FINE TUNE
LOC FREQ ENBL
PSET ENBL
(NOT USED)
PSET ENBL
RMT FREQ CHG
20 MHz
10 MHz
8 MHz
4 MHz
2 MHz
1 MHz
800 kHz
400 kHz
200 kHz
100 kHz
80 kHz
40 kHz
20 kHz
10 kHz
8 kHz
4 kHz
2 kHz
1 kHz
800 Hz
400 Hz
200 Hz
100 Hz
80 Hz
40 Hz
20 Hz
10 Hz
RESERVED
16
E
D
C
B
A
LSB
USB
(RSVD-FM)
AM
SSB
(RSVD-CW)
ISB
AGC CROWBAR ENBL
RMT FREQ CHG
LCL ENBL
PRL FREQ ENBL
NMIF
NOT USED
UP/DOWN
RATE (1)
RATE (2)
RATE (3)
RATE (8)
RATE (16)
FINE TUNE
RMT FREQ CHG
PRL FREQ ENBL
(RSVD-FM)
AM
SSB
(RSVD-CW)
ISB
ISB
LSB
AGC CROWBAR ENBL
RMT FREQ CHG



Preset Control, Block Diagram
Figure 7A (Sheet 2)


SYNTHESIZER CHASSIS A23
635-9697-001
P/O P11
P/O J10
BF 20 MHz 38
BG 10 MHz 37
BH 8 MHz 36
BI 4 MHz 35
BJ 2 MHz 34
BK 1 MHz 33
J9 P/O P1
16 15 5 4 14 3
SYNTH OUTPUT A22
623-2079-001
BL 800 kHz 32
BM 400 kHz 31
BN 200 kHz 30
BO 100 kHz 29
J8 P/O P1
9 19 8 18
SYNTH 100 kHz DECADE A21
623-2080-001
BP 80 kHz 28
BQ 40 kHz 27
BR 20 kHz 26
BS 10 kHz 25
J7 P/O P1
9 19 8 18
SYNTH 10 kHz DECADE A20
623-2080-002
BT 8 kHz 24
BU 4 kHz 23
BV 2 kHz 22
BW 1 kHz 21
J6 P/O P1
9 19 8 18
SYNTH 1 kHz DECADE A19
623-2080-003
BX 800 Hz 20
BY 400 Hz 19
BZ 200 Hz 18
CA 100 Hz 17
J5 P/O P1
9 19 8 18
SYNTH 100 kHz DECADE A18
623-2080-004
CB 80 Hz 16
CC 40 Hz 15
CD 20 Hz 14
CE 10 Hz 13
J4 P/O P1
9 19 8 18
SYNTH END DECADE A17
635-0657-001
RESERVED 12 11 19 9
J3
9 19 8 18
NOT USED A16
CS LCL FREQ ENBL 7
FREQUENCY DIS
P/O P8
P/O J5
BF 20 MHz 32
BG 10 MHz 31
BH 8 MHz 30
BI 4 MHz 29
BJ 2 MHz 28
BK 1 MHz 27
BL 800 kHz 26
BM 400 kHz 25
BN 200 kHz 24
BO 100 kHz 23
BP 80 kHz 22
BQ 40 kHz 21
BR 20 kHz 20
BS 10 kHz 19
BT 8 kHz 18
BU 4 kHz 17
BV 2 kHz 16
BW 1 kHz 15
BX 800 Hz 14
BY 400 Hz 13
BZ 200 Hz 12
CA 100 Hz 11
CB 80 Hz 10
CC 40 Hz 9
CD 20 Hz 8
CE 10 Hz 7
RESERVED 6 5 4 3
CS LCL FREQ ENBL 1
P/O P12
CT LCL ENBL 14
BCD-TO 7 BAR DECODE
BCD-TO 7 BAR DECODE
BCD-TO 7 BAR DECODE
BCD-TO 7 BAR DECODE
BCD-TO 7 BAR DECODE
BCD-TO 7 BAR DECODE
BCD-TO 7 BAR DECODE
BCD-TO 7 BAR DECODE



Preset Control, Block Diagram
Figure 7A (Sheet 3)

information will be stored on the selected channel only if the PRESET switch is pressed to STORE. When PRESET switch is pressed to STORE, a logic 1 is applied to local frequency enable input through A2A2J1-21, A2A4J1-21, P4-21, P6-29, and J10-15 to preset A12. The preset control is adaptable to a 100 ms to 5 s per channel scan rate when used with an appropriate scanner option. The scan enable (logic 1) is applied to J10-89 and enables scan circuits. With the scan circuits enabled, a scan start (logic 1) at J10-88 initiates the start of the scan cycle. Starting at the addressed channel the scanner will count down to 0 where it receives a counter overrun. When the overrun is received, a preset enable pulse is generated causing the scanner to restart scanning at preset channel selected.

2.3 Remote Control Operation (Remote Control Only)

The HF-8095 Receiver Control unit is designed as a companion to the remote controlled 851S-1 Receiver. This control unit provides all the functions required to remotely control and monitor the operation of the receiver. The control unit generates the serial data required to control the receiver, and accepts serial monitor data from the receiver for display of the current operating status. When remote processor control of the receiver is desired, the processor must generate the serial data characters required to control the receiver and interpret the monitor data from the receiver. In processor control applications, the receiver control interface requirements are similar to a serial data terminal in operation, with formatted messages from the processor controlling operation of the receiver and messages from the receiver to the processor reporting operating status of the receiver. An RS-232C serial, asynchronous, input/output interface capability is required in the processor for remote control of the receiver.

The following paragraphs describe the characteristics applicable to remote control of the receiver and the operation of the remote control circuits in the receiver.

2.3.1 General

Two methods of serial data signaling are available in the remote controlled 851S-1 receiver. Each method is strap selectable on the serial interface card. The two methods are frequency shift keyed audio tones (FSK) and RS-232C data logic levels. In conjunction with selection of the RS-232C signaling, strapping is available to invert the polarity of the RS-232C data for compatibility with the logic polarity and voltage levels defined in MIL-STD-188C.

When the FSK method is selected, only one receiver may be controlled and monitored by a single HF-8091 control unit. When the RS-232C logic level signaling method is selected, up to 16 individually addressable receivers may be controlled and monitored by a single HF-8095 control unit or processor. The RS-232C control can be by direct connection to the control unit or processor, or by transmission over data modems over longer distances.

Two separate sets of data lines are used for serial control of the receiver. One set, called the control bus, is used to receive command data. The other set, called the monitor bus, is used to transmit status information. When using FSK signaling, the control and monitor buses are balanced 600-ohm audio lines. When strapped for RS-232C signaling, the control and monitor buses are unbalanced line to ground. The data transmission rate on the control and monitor buses are strap selectable on the serial interface card. Transmission rates are 75, 150, 300, 600, 1200, 2400, 4800, 9600, and 19,200 bauds. The usable data rates for the FSK signaling method are limited to not more than 600 bauds. Each remote receiver must be strapped for the same data rate and parity as the associated control unit or processor.

Data transmitted and received on the control and monitor buses is serial, asynchronous, and organized in one of two formats, 8-bit character or ASCII. In the 8-bit character format the characters are made up of 11 bits, consisting of one start bit, eight data bits, one parity bit, and one stop bit, in that order. Control data bits are determined by settings of the front panel switches and controls on the control unit, or by program control for processor control applications. Monitor data bits are determined by the current operational status of the remote unit. In the ASCII format, the characters are made up of 9, 10, or 11 bits consisting of one start bit, seven data bits, one parity bit (optional), and one or two (optional) stop bits, in that order. The ASCII characters are then organized into 13 character words. Note that when using ASCII format the remote control must provide direct bcd frequency control signals rather than rate control signals.

Except for those monitor bits that have no corresponding control functions (such as fault bits and performance monitoring bits), the control and monitor words have identical data formats. The formats are summarized in figures 7B, 7C, and 7D and are explained in detail in the operations section of this manual.
(Table 1 deleted.)

WORD	CHAR-ACTER	STOP BIT	PARITY BIT	CHARACTER BIT POSITION B8	B7	B6	B5	B4	B3	B2	B1	START BIT
1	1	1	X	WORD SYNC 1	1	SUBADDRESS 0	0	ADDRESS A4	A3	A2	A1	0
	2	1	X	CMD/STATUS RQST $\overline{C}$	$\overline{S}$	FREQ (10 MHz) (2)	(1)	FREQ (1 MHz) (8)	(4)	(2)	(1)	0 ①
	3	1	X	FREQ (100 kHz) (8)	(4)	(2)	(1)	FREQ (10 kHz) (8)	(4)	(2)	(1)	0
	4	1	X	FREQ (1 kHz) (8)	(4)	(2)	(1)	FREQ (100 Hz) (8)	(4)	(2)	(1)	0
	5	1	X	FREQ (10 Hz) (8)	(4)	(2)	(1)	FREQ (1 Hz) (8)	(4)	(2)	(1)	0
2	1	1	X	WORD SYNC 1	1	SUBADDRESS 0	1	ADDRESS A4	A3	A2	A1	0
	2	1	X	CMD/STATUS RQST $\overline{C}$	$\overline{S}$	0	(16)	RF GAIN CONTROL (8)	(4)	(2)	(1)	0 ①②
	3	1	X	0	VBFO ENABLE	AFC ENABLE	AGC CROWBAR ENABLE	USB AGC OFF	FAST	LSB AGC OFF	FAST	0
	4	1	X	BANDWIDTH FILTER ENABLES FL8	FL7	FL6	FL5	FL4	FL3	FL2	FL1	0 ③
	5	1	X	MODE ENABLES FM	AM	SSB	CW	ISB	RESERVED			0
3	1	1	X	WORD SYNC 1	1	SUBADDRESS 1	0	ADDRESS A4	A3	A2	A1	0
	2	1	X	CMD/STATUS RQST $\overline{C}$	$\overline{S}$	0	VBFO SIGN	VBFO OFFSET FREQ (1 kHz) (8)	(4)	(2)	(1)	0 ①
	3	1	X	VBFO OFFSET FREQ (100 Hz) (8)	(4)	(2)	(1)	VBFO OFFSET FREQ (10 Hz) (8)	(4)	(2)	(1)	0
	4	1	X	RESERVED								0
	5	1	X	RESERVED				VBFO TUNE	VBFO PRL ENABLE	FINE TUNE	RSVD	0
4	1	1	X	WORD SYNC 1	1	SUBADDRESS 1	1	ADDRESS A4	A3	A2	A1	0
	2	1	X	CMD/STATUS RQST $\overline{C}$	$\overline{S}$	UP/$\overline{\text{DOWN}}$	(16)	TUNING RATE CONTROL (8)	(4)	(2)	(1)	0 ①④
	3	1	X	AFC LOCK IND	RESERVED		CHAN A AUDIO MON	CHAN A AGC MON	RSVD	CHAN B AUDIO MON	CHAN B AGC MON	0 ⑤
	4	1	X	RESERVED				RECEIVE OVLD	SYNTH FAULT	PS FAULT	RCV FAULT	0 ⑤
	5	1	X	RESERVED		VBFO SYNTH FAULT	RSVD	PRESEL FAULT	DATA ERROR	LOCAL CONTROL	MONITOR	0 ⑤

NOTES:

① THE COMMAND (C) AND STATUS (S) REQUEST BITS ARE CODED AS FOLLOWS:

B8 $\overline{C}$	B7 $\overline{S}$	SIGNFICANCE
0	0	COMMAND WORD WITH STATUS REQUEST
0	1	COMMAND WORD ONLY-NO STATUS DESIRED
1	0	STATUS REQUEST ONLY (2 CHARACTER SEQUENCE)
1	1	THIS COMBINATION NOT ALLOWED

② RF GAIN CONTROL IS FIVE BITS BINARY CODED, APPROXIMATELY 3-dB GAIN REDUCTION PER STEP (PROCESSOR CONTROL APPLICATIONS) OR FOUR BITS (LEAST SIGNIFICANT BIT SET TO ZERO). APPROXIMATELY 6-dB GAIN REDUCTION PER STEP (CONTROL UNIT APPLICATIONS). ALL "ZERO" CODE INDICATES NO GAIN REDUCTION. PROGRESSING IN BINARY STEPS TO THE ALL "ONES" CODE FOR MAXIMUM GAIN REDUCTION.

③ FILTER BANDWIDTH DESIGNATIONS ARE DEFINED AS FOLLOWS:

FL1 -- USB	FL5 -- C
FL2 -- LSB	FL6 -- D
FL3 -- A	FL7 -- E
FL4 -- B	FL8 -- 16 kHz

④ WORD 4 COMMAND OR STATUS REQUEST IS ONLY TWO CHARACTERS LONG.

⑤ CHARACTERS 3,4, AND 5 OF MONITOR WORD 4 CONTAIN FAULT AND PERFORMANCE MONITOR BITS FOR WHICH NO CORRESPONDING CONTROL BITS EXIST. THE "DATA ERROR" BIT IS THE LOGICAL SUM OF THE FOLLOWING CONDITIONS:

A. RECEIVED CHARACTER PARITY ERROR.
B. FRAMING ERROR (NO VALID STOP RECEIVED WITH THE CHARACTER).
C. OVERRUN ERROR (PREVIOUS CHARACTER WAS NOT PROCESSED BEFORE THE CURRENT CHARACTER WAS RECEIVED).
D. INVALID CHARACTER SEQUENCE.

⑥ 1 = LOGIC 1
0 = LOGIC 0
(1) = BIT WEIGHT
X = FUNCTION OF STRAPPING

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8-Bit Control and Monitor Word Format
Figure 7B

CHARACTER SIGNIFICANCE		ASCII PRINT CHAR'S	FUNCTIONAL BIT CODING			
			WT 8	WT 4	WT 2	WT 1
CR LF A1 A2 SD F1 F2 F3 F4 F5 F6 F7 F8 X		WORD 1 CHARACTER SEQUENCE				
CR	CARRIAGE RETURN	CR	NA	NA	NA	NA
LF	LINE FEED	LF	NA	NA	NA	NA
A1	ADDRESS M.S.D. (BCD)	0-3	0	0	A1 (2)	A1 (1)
A2	ADDRESS L.S.D. (BCD)	0-9	A2 (8)	A2 (4)	A2 (2)	A2 (1)
SD	SEQUENCE DESIGNATOR	0,1,2	NA	NA	NA	NA
F1	FREQUENCY- 10 MHz (BCD)	0,1,2	0	0	10 MHz (2)	10 MHz (1)
F2	FREQUENCY- 1 MHz (BCD)	0-9	1 MHz (8)	1 MHz (4)	1 MHz (2)	1 MHz (1)
F3	FREQUENCY- 100 kHz (BCD)	0-9	100 kHz (8)	100 kHz (4)	100 kHz (2)	100 kHz (1)
F4	FREQUENCY- 10 kHz (BCD)	0-9	10 kHz (8)	10 kHz (4)	10 kHz (2)	10 kHz (1)
F5	FREQUENCY- 1 kHz (BCD)	0-9	1 kHz (8)	1 kHz (4)	1 kHz (2)	1 kHz (1)
F6	FREQUENCY- 100 Hz (BCD)	0-9	100 Hz (8)	100 Hz (4)	100 Hz (2)	100 Hz (1)
F7	FREQUENCY- 10 Hz (BCD)	0-9	10 Hz (8)	10 Hz (4)	10 Hz (2)	10 Hz (1)
F8	FREQUENCY- 1 Hz (BCD)	0-9	1 Hz (8)	1 Hz (4)	1 Hz (2)	1 Hz (1)
X	EXECUTE	X	NA	NA	NA	NA
CR LF A1 A2 SD M1 M2 M3 M4 M5 M6 M7 M8 X		WORD 2 CHARACTER SEQUENCE				
CR	CARRIAGE RETURN	CR	NA	NA	NA	NA
LF	LINE FEED	LF	NA	NA	NA	NA
A1	ADDRESS M.S.D. (BCD)	0-3	0	0	A1 (2)	A1 (1)
A2	ADDRESS L.S.D. (BCD)	0-9	A2 (8)	A2 (4)	A2 (2)	A2 (1)
SD	SEQUENCE DESIGNATOR	4,5,6	NA	NA	NA	NA
M1	RF GAIN CONTROL	0-9, A-F	0	0	0	RF GAIN (16)
M2	RF GAIN CONTROL	0-9, A-F	RF GAIN (8)	RF GAIN (4)	RF GAIN (2)	RF GAIN (1)
M3	VBFO/AFC/AGC CROWBAR ENABLES	0-9, A-F	0	VBFO ENABLE	AFC ENABLE	AGC CROWBAR
M4	AGC TIME CONSTANTS	0-9, A-F	USB AGC OFF	USB AGC FAST	LSB AGC OFF	LSB AGC FAST
M5	BANDWIDTH FILTER ENABLES	0-9, A-F	FL8 (16)	FL7 (E)	FL6 (D)	FL5 (C)
M6	BANDWIDTH FILTER ENABLES	0-9, A-F	FL4 (B)	FL3 (A)	FL2 (LSB)	FL1 (USB)
M7	MODE SELECT ENABLES	0-9, A-F	FM	AM	SSB	CW
M8	ISB ENABLE	0-9, A-F	ISB	0	0	0
X	EXECUTE	X	NA	NA	NA	NA
CR LF A1 A2 SD V1 V2 V3 V4 V5 V6 V7 V8 X		WORD 3 CHARACTER SEQUENCE				
CR	CARRIAGE RETURN	CR	NA	NA	NA	NA
LF	LINE FEED	LF	NA	NA	NA	NA
A1	ADDRESS M.S.D. (BCD)	0-3	0	0	A1 (2)	A1 (1)
A2	ADDRESS L.S.D. (BCD)	0-9	A2 (8)	A2 (4)	A2 (2)	A2 (1)
SD	SEQUENCE DESIGNATOR	8,9,A	NA	NA	NA	NA
V1	VBFO SIGN (0=+)	0,1	0	0	0	VBFO SIGN
V2	VBFO FREQUENCY, 1 kHz (BCD)	0-9	1 kHz (8)	1 kHz (4)	1 kHz (2)	1 kHz (1)
V3	VBFO FREQUENCY, 100 Hz (BCD)	0-9	100 Hz (8)	100 Hz (4)	100 Hz (2)	100 Hz (1)
V4	VBFO FREQUENCY, 10 Hz (BCD)	0-9	10 Hz (8)	10 Hz (4)	10 Hz (2)	10 Hz (1)
V5	AUXILIARY	0-9,A-F	-	-	-	-
V6	AUXILIARY	0-9, A-F	-	-	-	-
V7	RESERVED	0	0	0	0	0
V8	VBFO TUNE, VBFO PAR ENABLE, FINE TUNE	0-9, A-F	VBFO TUNE	VBFO PAR ENBL	FINE TUNE	0
X	EXECUTE	X	NA	NA	NA	NA
CR LF A1 A2 SD K1 X		WORD 4 CHARACTER SEQUENCE				
CR	CARRIAGE RETURN	CR	NA	NA	NA	NA
LF	LINE FEED	LF	NA	NA	NA	NA
A1	ADDRESS M.S.D. (BCD)	0-3	0	0	A1 (2)	A1 (1)
A2	ADDRESS L.S.D. (BCD)	0-9	A2 (8)	A2 (4)	A2 (2)	A2 (1)
SD	SEQUENCE DESIGNATOR	C,D,E	NA	NA	NA	NA
K1	RESERVED	0	0	0	0	0
X	EXECUTE	X	NA	NA	NA	NA

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ASCII Character Control Word Format
Figure 7C

CHARACTER SIGNIFICANCE		ASCII PRINT CHAR'S	FUNCTIONAL BIT CODING			
			WT 8	WT 4	WT 2	WT 1
- - A1 A2 SD F1 F2 F3 F4 F5 F6 F7 F8 $		WORD 1 CHARACTER SEQUENCE				
-	HYPHEN	-	NA	NA	NA	NA
-	HYPHEN	-	NA	NA	NA	NA
A1	ADDRESS, M.S.D. (BCD)	0-3	0	0	A1 (2)	A1 (1)
A2	ADDRESS, L.S.D. (BCD)	0-9	A2 (8)	A2 (4)	A2 (2)	A2 (1)
SD	SEQUENCE DESIGNATOR	1	NA	NA	NA	NA
F1	FREQUENCY- 10 MHz (BCD)	0,1,2	0	0	10 MHz (2)	10 MHz (1)
F2	FREQUENCY- 1 MHz (BCD)	0-9	1 MHz (8)	1 MHz (4)	1 MHz (2)	1 MHz (1)
F3	FREQUENCY-100 kHz (BCD)	0-9	100 kHz (8)	100 kHz (4)	100 kHz (2)	100 kHz (1)
F4	FREQUENCY- 10 kHz (BCD)	0-9	10 kHz (8)	10 kHz (4)	10 kHz (2)	10 kHz (1)
F5	FREQUENCY- 1 kHz (BCD)	0-9	1 kHz (8)	1 kHz (4)	1 kHz (2)	1 kHz (1)
F6	FREQUENCY-100 Hz (BCD)	0-9	100 Hz (8)	100 Hz (4)	100 Hz (2)	100 Hz (1)
F7	FREQUENCY- 10 Hz (BCD)	0-9	10 Hz (8)	10 Hz (4)	10 Hz (2)	10 Hz (1)
F8	FREQUENCY- 1 kHz (BCD)	0-9	1 Hz (8)	1 Hz (4)	1 Hz (2)	1 Hz (1)
$	END DELIMETER	$	NA	NA	NA	NA
- - A1 A2 SD M1 M2 M3 M4 M5 M6 M7 M8 $		WORD 2 CHARACTER SEQUENCE				
-	HYPHEN	-	NA	NA	NA	NA
-	HYPHEN	-	NA	NA	NA	NA
A1	ADDRESS, M.S.D. (BCD)	0-3	0	0	A1 (2)	A1 (1)
A2	ADDRESS, L.S.D. (BCD)	0-9	A2 (8)	A2 (4)	A2 (2)	A2 (1)
SD	SEQUENCE DESIGNATOR	5	NA	NA	NA	NA
M1	RF GAIN CONTROL	0-9, A-F	0	0	0	RF GAIN (16)
M2	RF GAIN CONTROL	0-9, A-F	RF GAIN (8)	RF GAIN (4)	RF GAIN (2)	RF GAIN (1)
M3	VBFO/AFC/AGC CROWBAR ENABLES	0-9, A-F	0	VBFO ENBL	AFC ENBL	AGC CROWBAR
M4	AGC TIME CONSTANTS	0-9, A-F	USB AGC OFF	USB AGC FAST	LSB AGC OFF	LSB AGC FAST
M5	BANDWIDTH FILTER ENABLES	0-9, A-F	FL8 (16)	FL7 (E)	FL6 (D)	FL5 (C)
M6	BANDWIDTH FILTER ENABLES	0-9, A-F	FL4 (8)	FL3 (A)	FL2 (LSB)	FL1 (USB)
M7	MODE SELECT ENABLES	0-9, A-F	FM	AM	SSB	CW
M8	ISB ENABLE	0-9, A-F	ISB	0	0	0
$	END DELIMITER	$	NA	NA	NA	NA
- - A1 A2 SD V1 V2 V3 V4 V5 V6 V7 V8 $		WORD 3 CHARACTER SEQUENCE				
-	HYPHEN	-	NA	NA	NA	NA
-	HYPHEN	-	NA	NA	NA	NA
A1	ADDRESS, M.S.D. (BCD)	0-3	0	0	A1 (2)	A1 (1)
A2	ADDRESS, L.S.D. (BCD)	0-9	A2 (8)	A2 (4)	A2 (2)	A2 (1)
SD	SEQUENCE DESIGNATOR	9	NA	NA	NA	NA
V1	VBFO SIGN (0=+)	0,1	0	0	0	VBFO SIGN
V2	VBFO FREQUENCY, 1 kHz (BCD)	0-9	1 kHz (8)	1 kHz (4)	1 kHz (2)	1 kHz (1)
V3	VBFO FREQUENCY, 100 Hz (BCD)	0-9	100 Hz (8)	100 Hz (4)	100 Hz (2)	100 Hz (1)
V4	VBFO FREQUENCY, 10 Hz (BCD)	0-9	10 Hz (8)	10 Hz (4)	10 Hz (2)	10 Hz (1)
V5	AUXILIARY	0	-	-	-	-
V6	AUXILIARY	0	-	-	-	-
V7	RESERVED	0	0	0	0	0
V8	VBFO TUNE, VBFO PAR ENABLE, FINE TUNE	0-9, A-F	VBFO TUNE	VBFO PAR ENBL	FINE TUNE	0
$	END DELIMITER	$	NA	NA	NA	NA
- - A1 A2 SD S1 S2 S3 S4 S5 S6 S7 S8 $		WORD 4 CHARACTER SEQUENCE				
-	HYPHEN	-	NA	NA	NA	NA
-	HYPHEN	-	NA	NA	NA	NA
A1	ADDRESS, M.S.D. (BCD)	0-3	0	0	A1 (2)	A1 (1)
A2	ADDRESS, L.S.D. (BCD)	0-9	A2 (8)	A2 (4)	A2 (2)	A2 (1)
SD	SEQUENCE DESIGNATOR	D	NA	NA	NA	NA
S1	UP/DOWN, TUNE RATE (16)	0-3	0	0	UP/$\overline{\text{DOWN}}$	TUNE RATE (16)
S2	TUNE RATES	0-9, A-F	TUNE RATE (8)	TUNE RATE (4)	TUNE RATE (2)	TUNE RATE (1)
S3	AFC LOCK IND, CHAN A AF MONITOR	0-9, A-F	AFC LOCK	0	0	CHAN A AF
S4	CHAN A AGC/CHAN B AF/CHAN B AGC MONITORS	0-9, A-F	CHAN A AGC	0	CHAN B AF	CHAN B AGC
S5	RESERVED	0-7	0	0	0	0
S6	RF OVLD/SYNTH/PWR SPLY/RCVR FAULTS	0-9, A-F	RF OVLD	SYNTH	PWR SPLY	RCVR
S7	VBFO SYNTH FAULT	0-3	0	0	VBFO SYNTH	0
S8	PRESEL FAULT, DATA ERROR, LOCAL CONTROL, MONITOR	0-9, A-F	PRESEL FAULT	DATA ERROR	LOCAL CONTROL	MONITOR
$	END DELIMITER	$	NA	NA	NA	NA

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ASCII Character Monitor Word Format
Figure 7D

2.3.2 Receiver Serial Control Operation

2.3.2.1 Control Inputs (Refer to figure 8.)

Control data signals generated by the HF-8095 Receiver Control or processor are applied to the receiver as control information. These control signals are transferred over the control bus in serial format. If the receiver CONT switch is in the REM position, the serial information received controls the operation of the receiver.

Control data is applied to a serial data processor on the receiver serial interface A13. Word and status information is decoded from the control data and is used to determine strobe address information. The control data is then applied to the data input of four word serial-to-parallel converters on the receiver parallel output A12. Each serial-to-parallel converter is enabled before it accepts and processes the control data. This occurs when the strobe address input is decoded and an enable signal is generated by the word enable circuit.

The serial-to-parallel converters decode the serial input information and convert it to parallel output levels. These outputs provide all control signals necessary to control the receiver remotely. The outputs are also supplied to the parallel input A11 where they are processed and returned to the receiver control or processor as monitor data. This provides an indication on the front panel of the receiver control or to the processor of the control information received by the receiver. When the receiver CONT switch is in the LCL or MON position, the register outputs of the parallel output A12 are disabled, and the internal parallel control lines are controlled by the receiver front panel controls.

2.3.2.2 Monitor Outputs (Refer to figure 8.)

With the receiver CONT switch in the REM position, monitor signals indicating frequency, rf gain, AGC, bandwidth, mode, and related control and enable signals are applied, in parallel, from the receiver parallel output A12 to the receiver parallel input A11 for processing and application to the receiver serial interface A13. Fault and performance monitor indications are applied from appropriate areas of the receiver to the receiver parallel input A11 for processing and application to the receiver serial interface A13. The receiver serial interface A13 output to the receiver control is a series of monitor words in serial format. (The monitor word format is identical to the control word format, figure 7B.)

Four separate words are required to supply a complete status report to the remote control. These four words are independent of each other, thus can be transmitted at any time and in any sequence. Each monitor word is composed of five 11-bit characters. The last two bits of each character group are stop and parity bits. The first bit is a start bit. The first character of each monitor word is reserved for equipment address, word identification (subaddress), and word sync information. Bits seven and eight of the second character in each word are reserved for command and status request. The remaining characters of each word carry frequency, control, and monitor information.

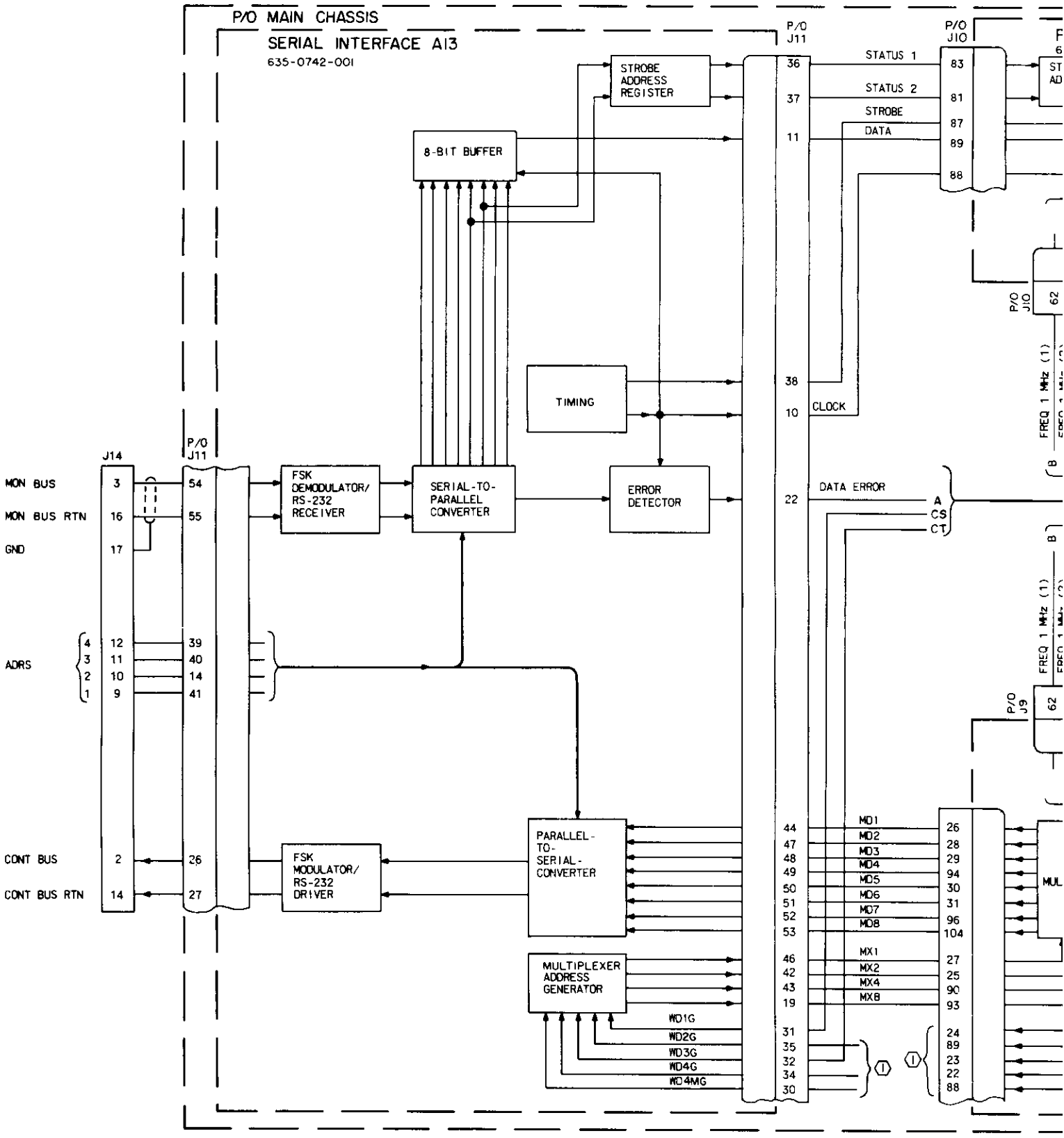
Monitor (and control) word timing is accomplished by a crystal-controlled oscillator on the receiver serial interface A13. A divider reduces the frequency to the desired values. Strapping permits selection of the baud rate for clock inputs to the various circuits. Selection is from 75, 150, 300, 600, 1200, 2400, 4800, 9600, and 19 200 bauds.

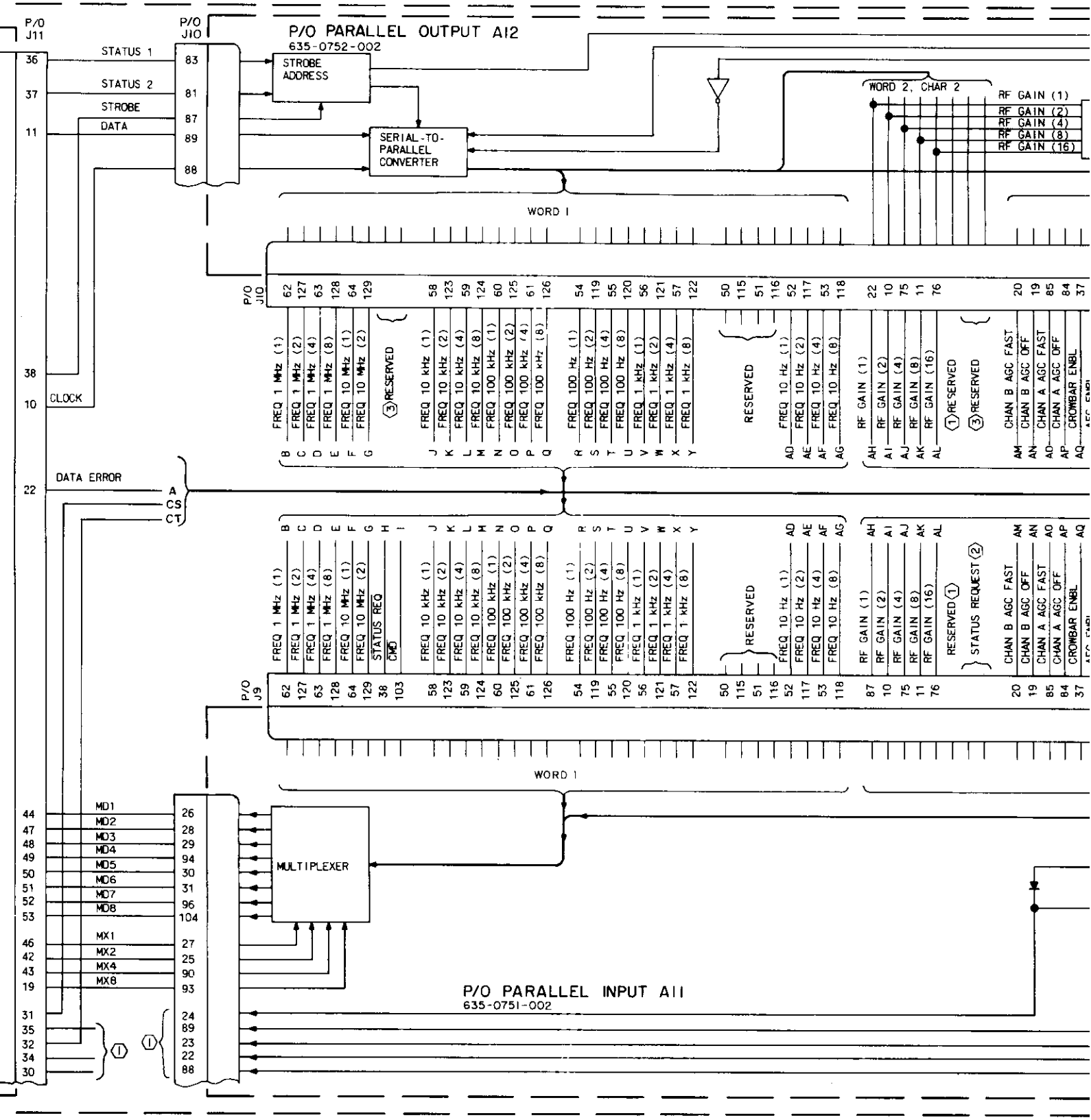
Figure 7B shows the format and function of each of the 11-bit characters in the four monitor words.

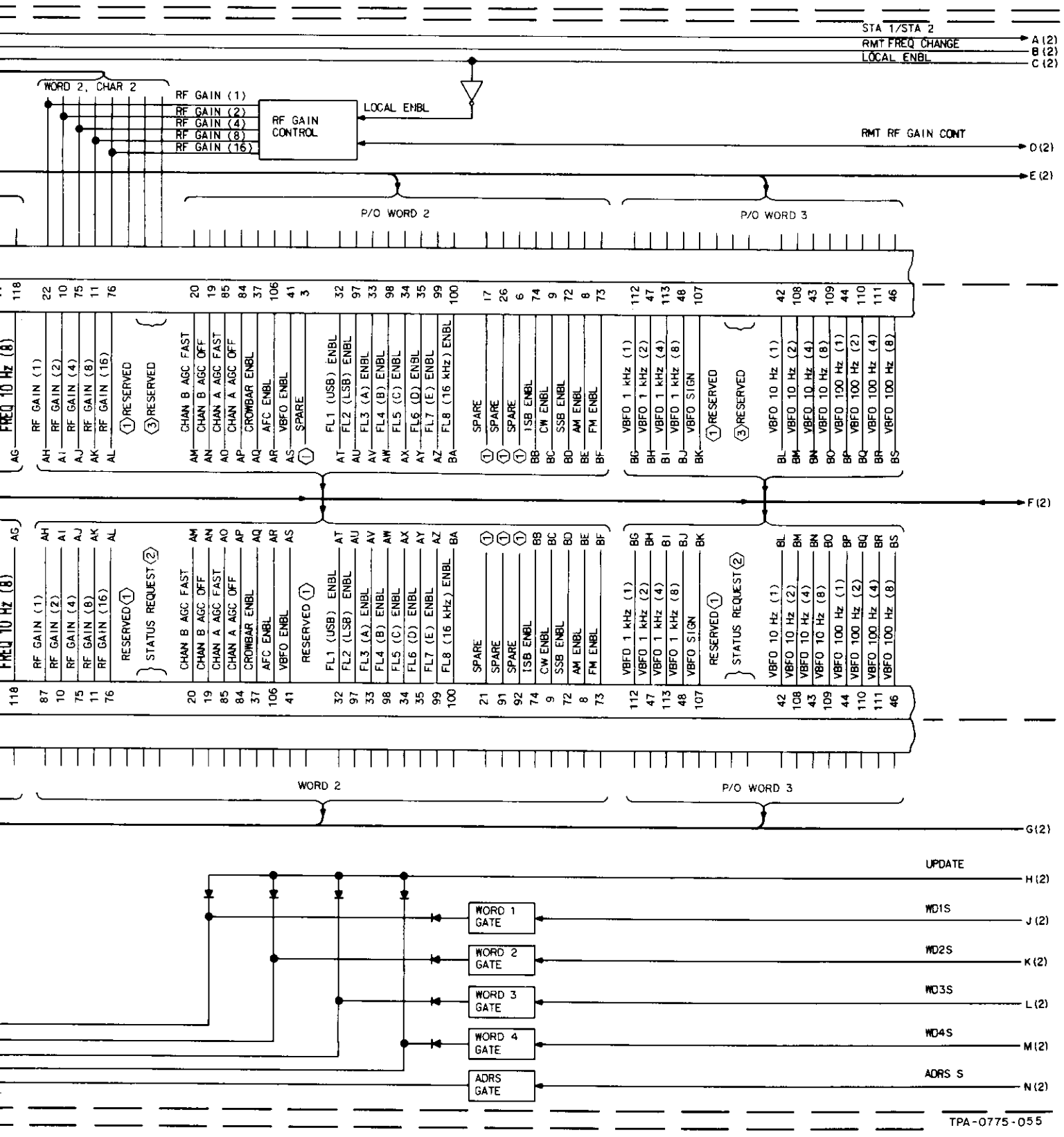
Monitor information (performance monitors and faults) from the receiver is fed to multiplexers on the receiver parallel input A11. This monitor data is clocked out through the receiver serial interface A13, which shifts the serial data through the FSK keyer or RS-232C driver circuit to the external monitor bus and receiver control.

With the receiver CONT switch in the LCL or MON position, operation of the monitor circuits is identical to that described above. However, the outputs of the storage registers on the parallel output A12 (which store the receiver control data) are disabled and the internal control lines (mode, frequency, bandwidth, etc) are controlled by the receiver front panel controls. Thus, the receiver front panel controls determine receiver operation and their control signals are applied to the parallel input A11 for processing and application to the receiver control as monitor data. Because of this, the monitor data from the receiver always contains the applied operational status of the receiver whether it is operated locally or remotely.

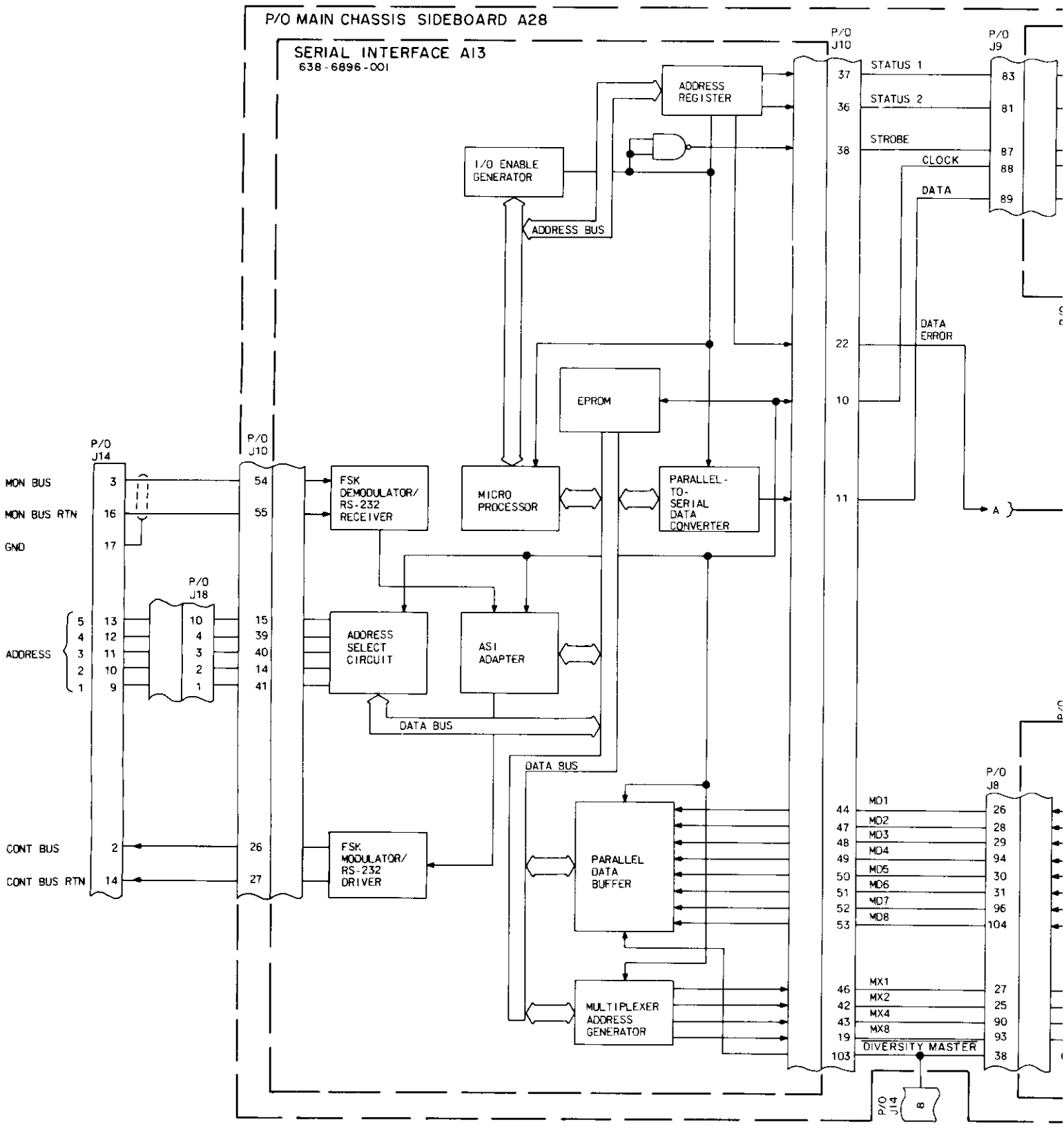
The LCL and MON positions of the CONT switch are identical, except that in the LCL position the local control bit (word 4, character 5, bit 2) of the monitor data is set to logic 1. In the MON position, both the local control bit and the monitor bit (word 4, character 5, bit 1) of monitor data are set to logic 1. The monitor bit may be used as a flag in processor control applications, indicating that some programmed action needs to be initiated by the processor control.

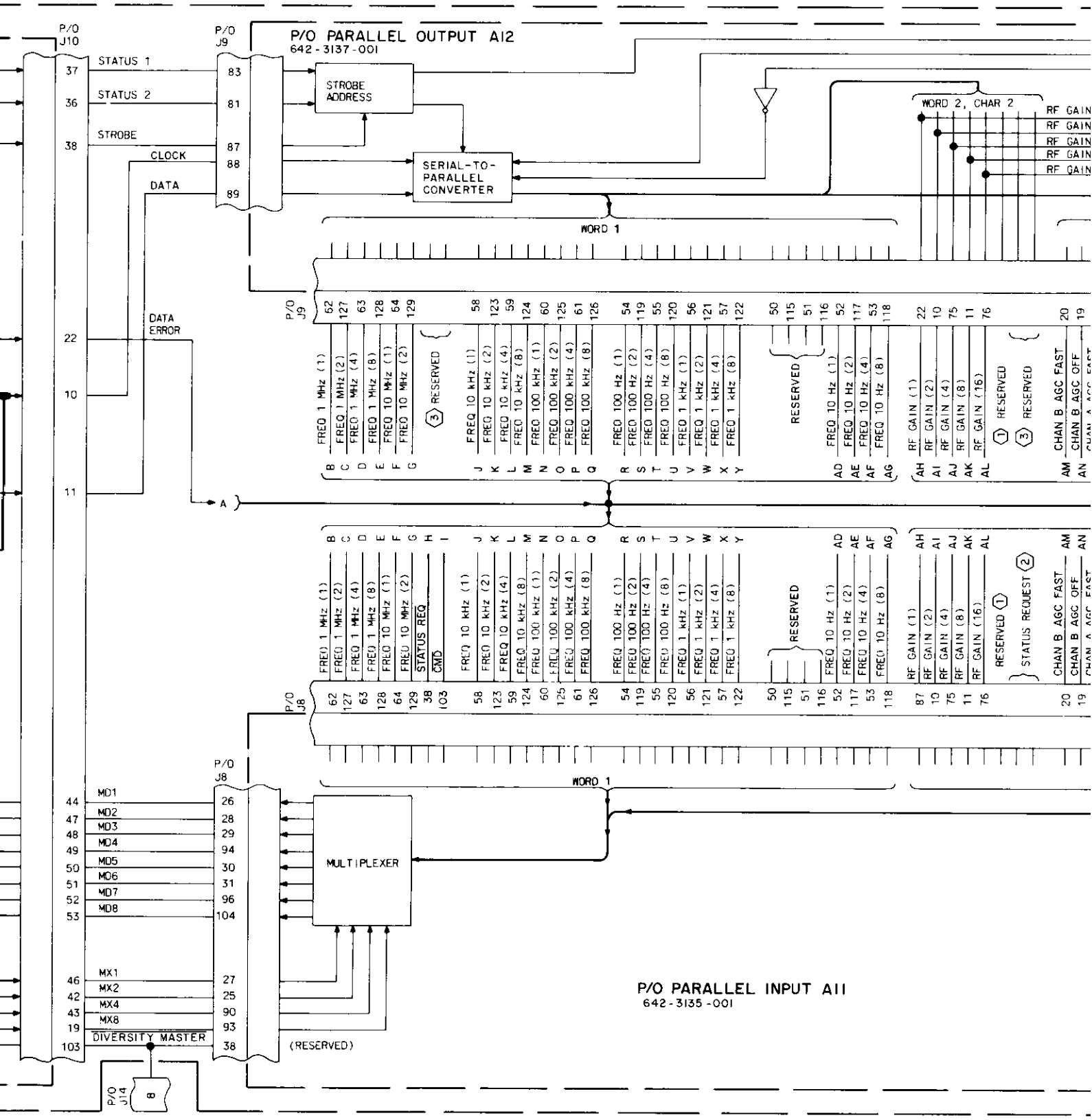

P/O MAIN CHASSIS
SERIAL INTERFACE A13
635-0742-001
P/O J11
P/O J10
STROBE ADDRESS REGISTER
8-BIT BUFFER
TIMING
FSK DEMODULATOR/ RS-232 RECEIVER
SERIAL-TO-PARALLEL CONVERTER
ERROR DETECTOR
PARALLEL-TO-SERIAL-CONVERTER
FSK MODULATOR/ RS-232 DRIVER
MULTIPLEXER ADDRESS GENERATOR
J14
MON BUS
MON BUS RTN
GND
ADRS
CONT BUS
CONT BUS RTN
STATUS 1
STATUS 2
STROBE
DATA
CLOCK
DATA ERROR
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MD8
MX1
MX2
MX4
MX8
WD1G
WD2G
WD3G
WD4G
WD4MG
FREQ 1 MHz (1)
P/O J9

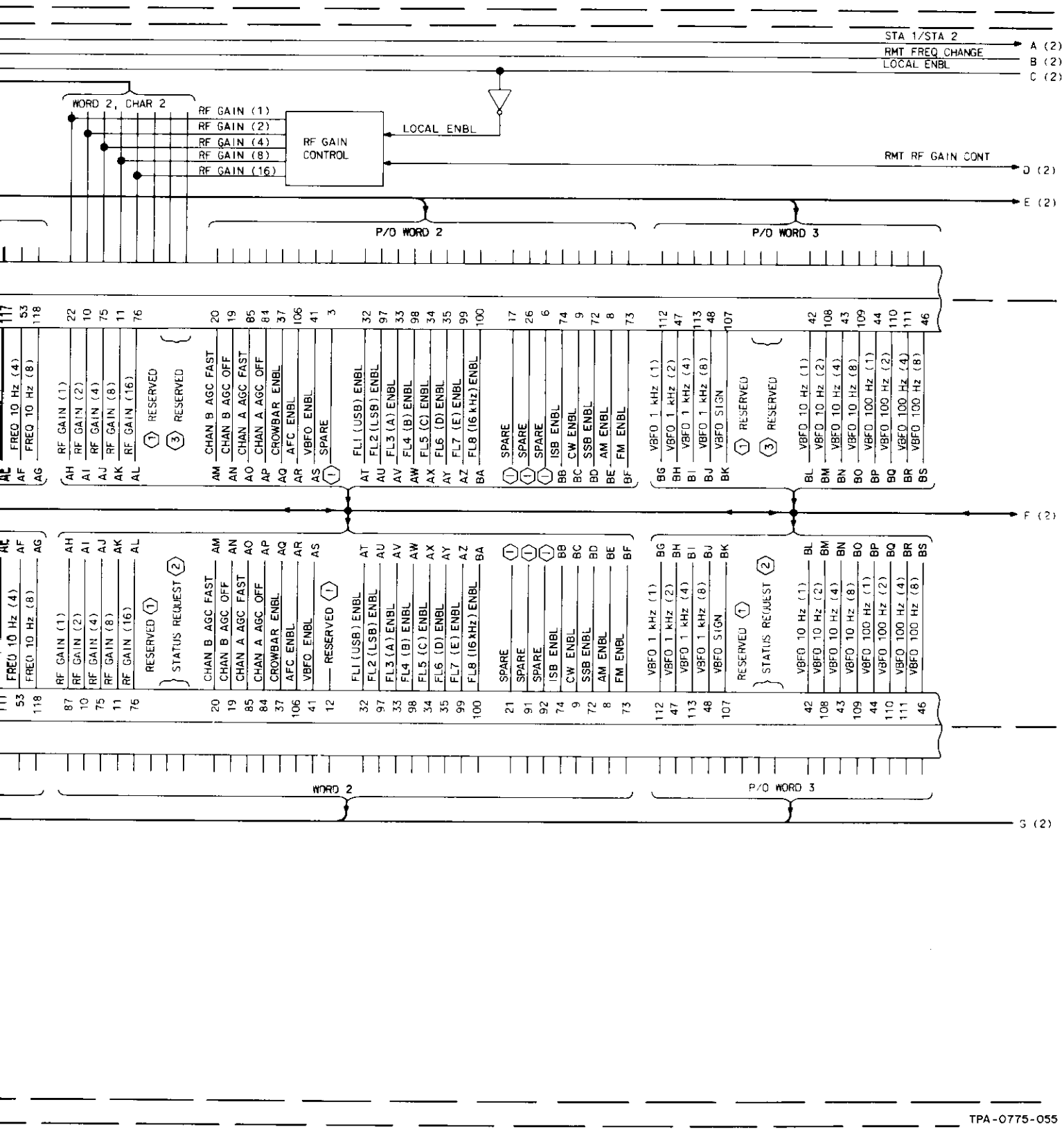

P/O J11
P/O J10
P/O PARALLEL OUTPUT A12
635-0752-002
STATUS 1
STATUS 2
STROBE
DATA
CLOCK
STROBE ADDRESS
SERIAL-TO-PARALLEL CONVERTER
WORD 2, CHAR 2
RF GAIN (1)
RF GAIN (2)
RF GAIN (4)
RF GAIN (8)
RF GAIN (16)
WORD 1
FREQ 1 MHz (1)
FREQ 1 MHz (2)
FREQ 1 MHz (4)
FREQ 1 MHz (8)
FREQ 10 MHz (1)
FREQ 10 MHz (2)
RESERVED
FREQ 10 kHz (1)
FREQ 10 kHz (2)
FREQ 10 kHz (4)
FREQ 10 kHz (8)
FREQ 100 kHz (1)
FREQ 100 kHz (2)
FREQ 100 kHz (4)
FREQ 100 kHz (8)
FREQ 100 Hz (1)
FREQ 100 Hz (2)
FREQ 100 Hz (4)
FREQ 100 Hz (8)
FREQ 1 kHz (1)
FREQ 1 kHz (2)
FREQ 1 kHz (4)
FREQ 1 kHz (8)
RESERVED
FREQ 10 Hz (1)
FREQ 10 Hz (2)
FREQ 10 Hz (4)
FREQ 10 Hz (8)
RF GAIN (1)
RF GAIN (2)
RF GAIN (4)
RF GAIN (8)
RF GAIN (16)
RESERVED
RESERVED
CHAN B AGC FAST
CHAN B AGC OFF
CHAN A AGC FAST
CHAN A AGC OFF
CROWBAR ENBL
DATA ERROR
A
CS
CT
P/O J9
STATUS REQ
CMD
STATUS REQUEST
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MD8
MX1
MX2
MX4
MX8
MULTIPLEXER
P/O PARALLEL INPUT A11
635-0751-002



Remote Control, Block Diagram
Figure 8 (Sheet 1 of 5)


P/O MAIN CHASSIS SIDEBOARD A28
SERIAL INTERFACE A13
638-6896-001
P/O J10
P/O J9
ADDRESS REGISTER
I/O ENABLE GENERATOR
ADDRESS BUS
STATUS 1
STATUS 2
STROBE
CLOCK
DATA
DATA ERROR
EPROM
MICRO PROCESSOR
PARALLEL-TO-SERIAL DATA CONVERTER
P/O J14
P/O J10
MON BUS
MON BUS RTN
GND
FSK DEMODULATOR/ RS-232 RECEIVER
P/O J18
ADDRESS
ADDRESS SELECT CIRCUIT
ASI ADAPTER
DATA BUS
CONT BUS
CONT BUS RTN
FSK MODULATOR/ RS-232 DRIVER
PARALLEL DATA BUFFER
MULTIPLEXER ADDRESS GENERATOR
P/O J8
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MD8
MX1
MX2
MX4
MX8
DIVERSITY MASTER
A
P/O J14
8


P/O PARALLEL OUTPUT A12
642-3137-001
P/O J10
P/O J9
STATUS 1
STATUS 2
STROBE
CLOCK
DATA
DATA ERROR
STROBE ADDRESS
SERIAL-TO-PARALLEL CONVERTER
WORD 1
WORD 2, CHAR 2
RF GAIN
RESERVED
P/O J8
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MD8
MX1
MX2
MX4
MX8
DIVERSITY MASTER
MULTIPLEXER
(RESERVED)
P/O J14
P/O PARALLEL INPUT A11
642-3135-001



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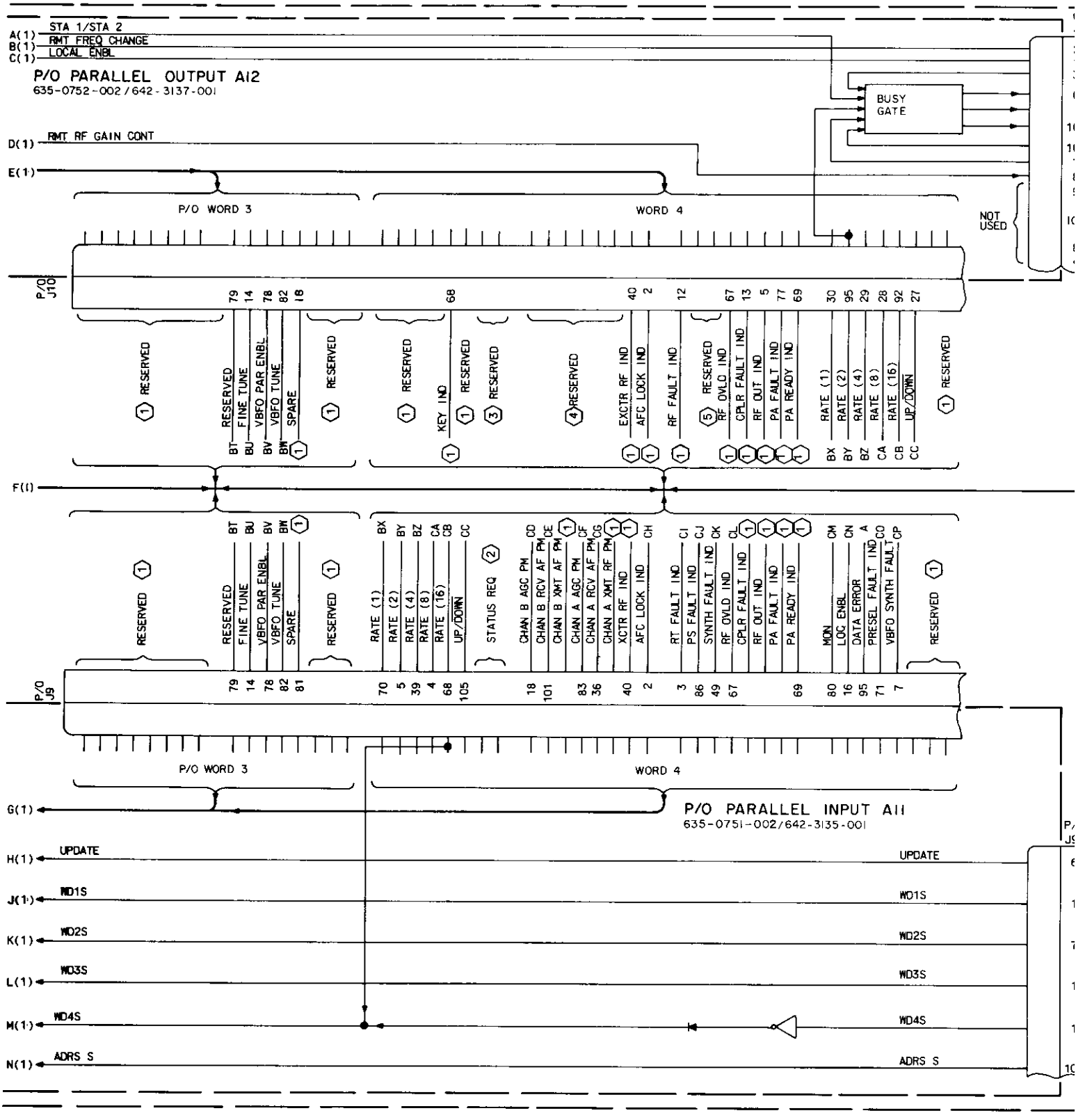
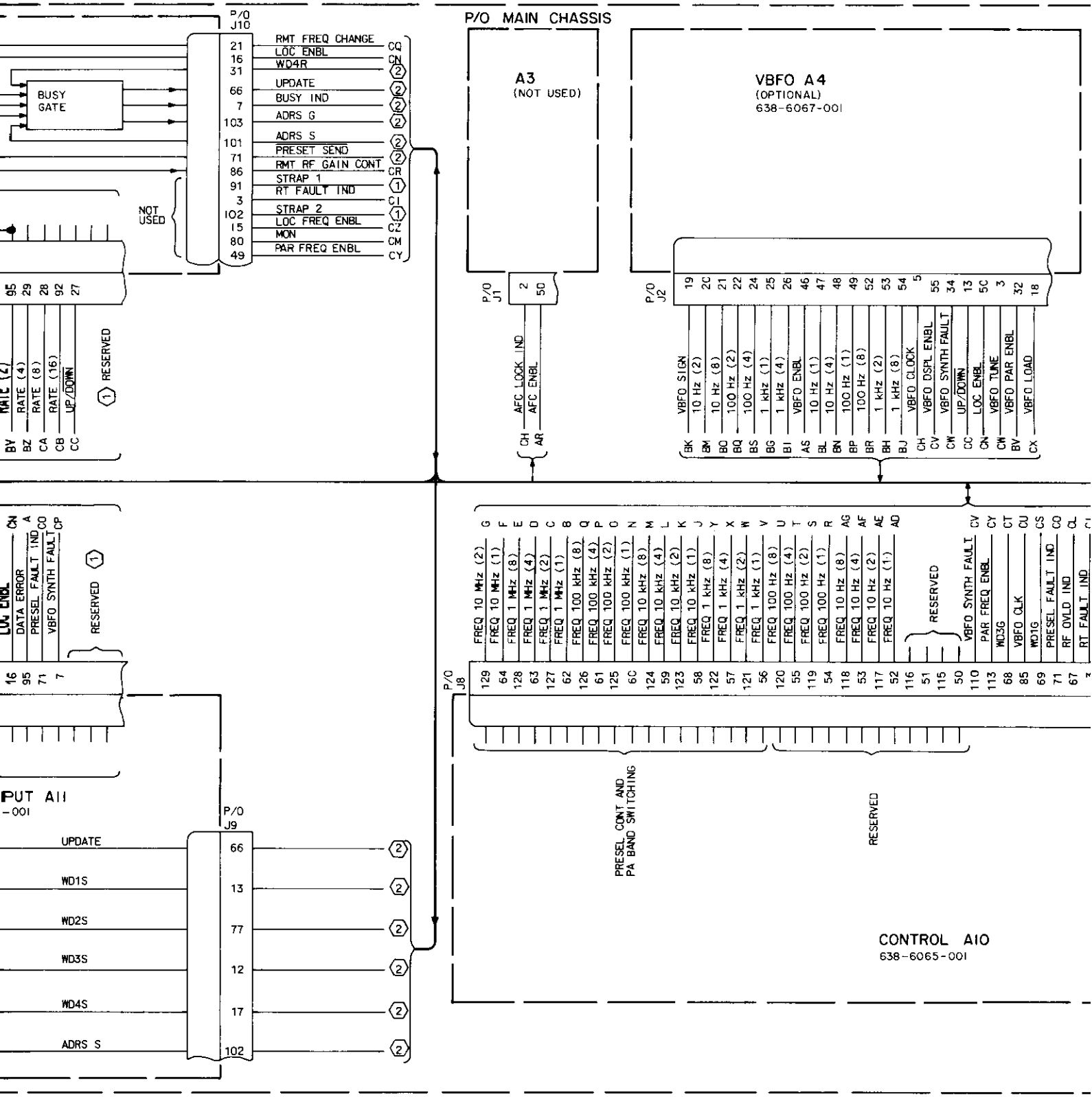
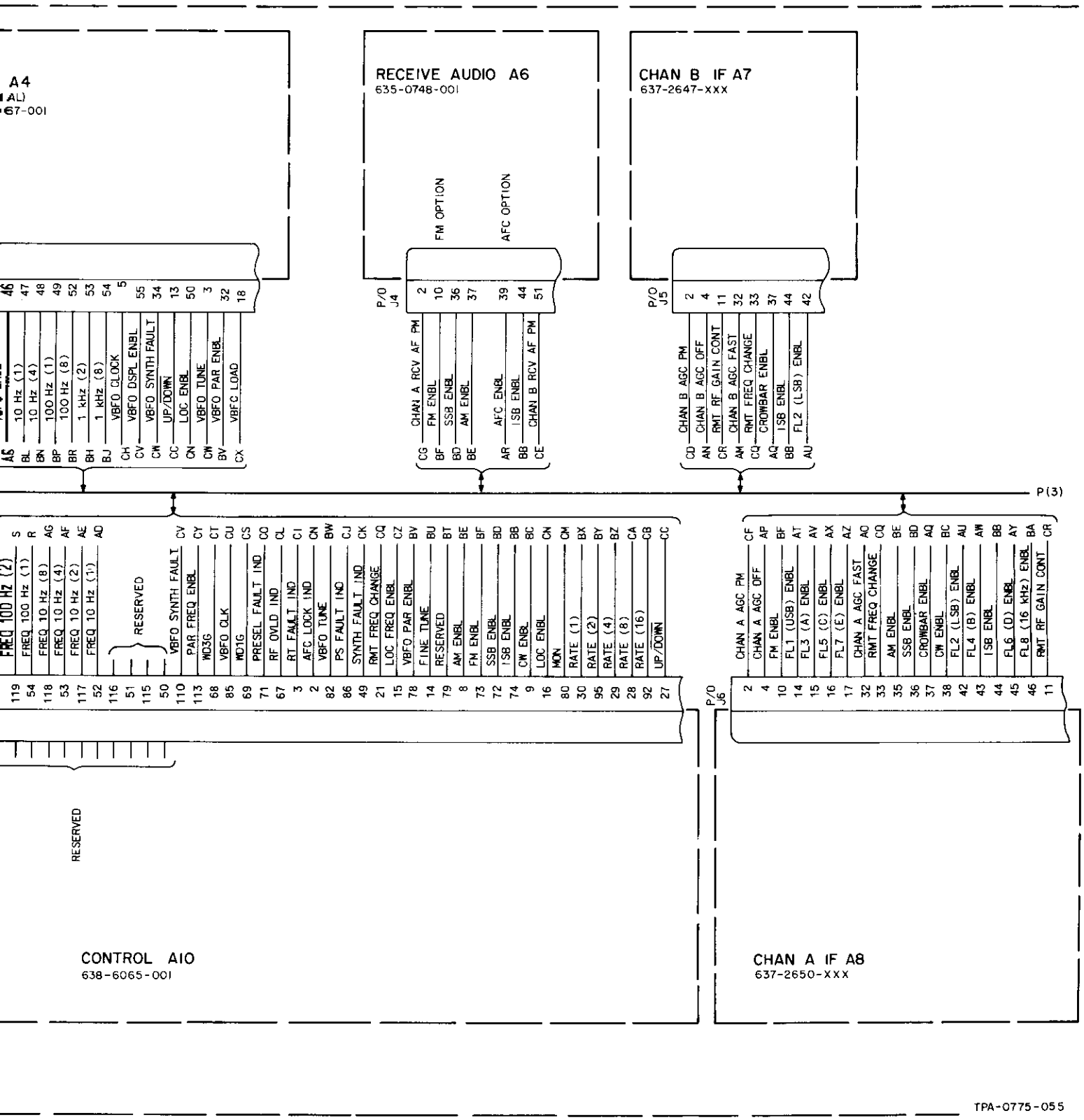
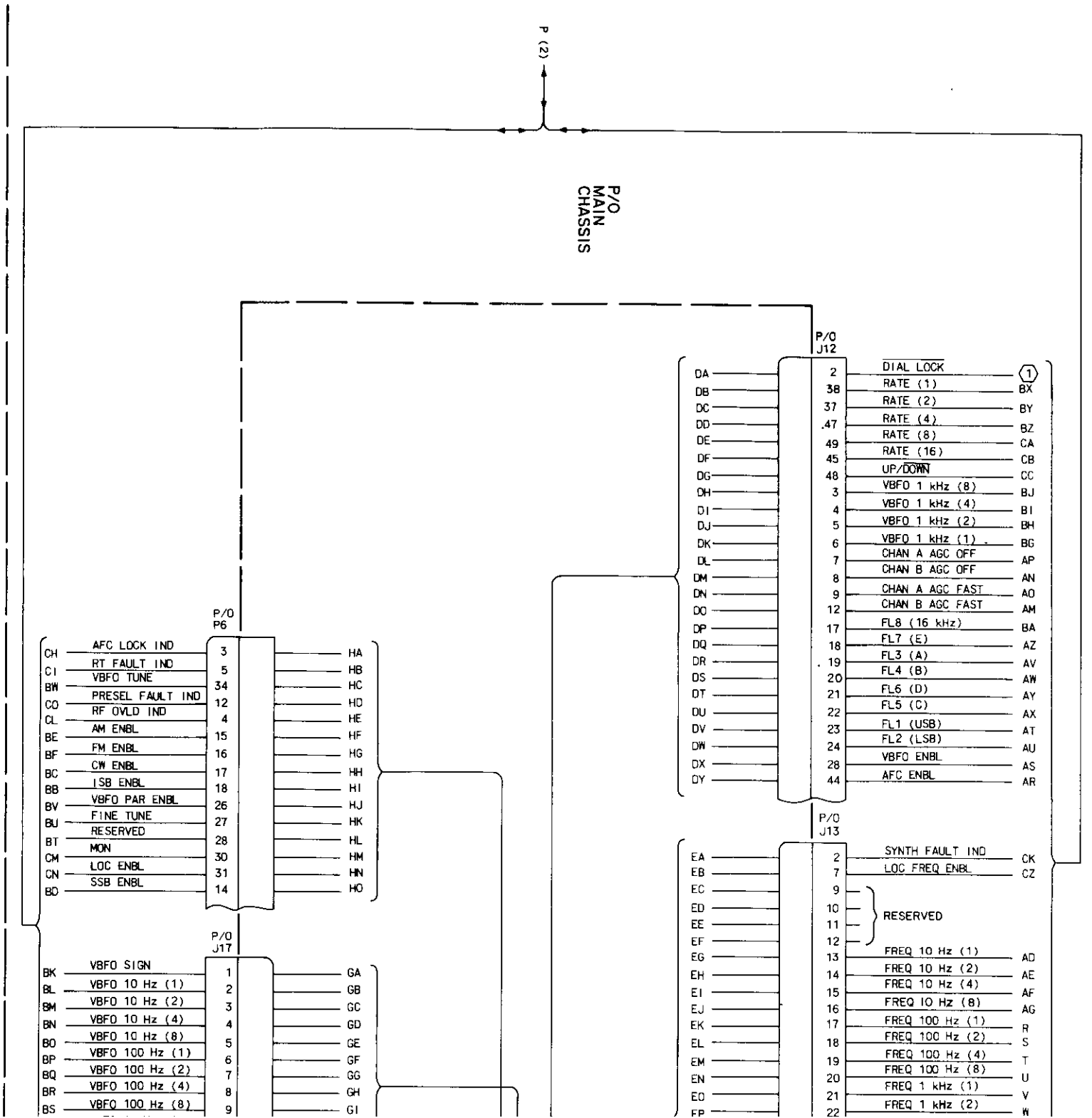
Remote Control, Block Diagram
Figure 8 (Sheet 1A)

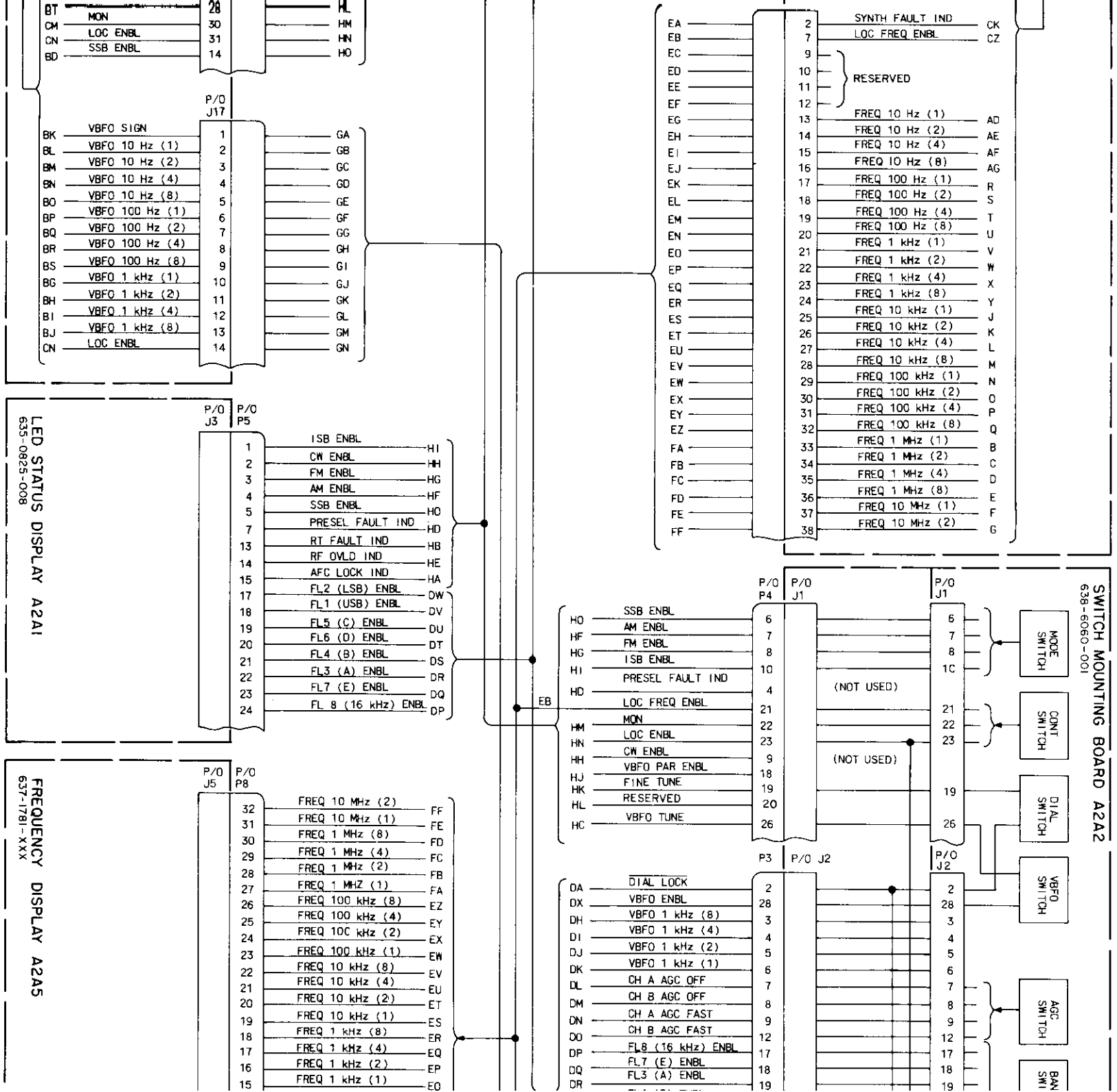

A(1) STA 1/STA 2
B(1) RMT FREQ CHANGE
C(1) LOCAL ENBL
P/O PARALLEL OUTPUT AI2
635-0752-002/642-3137-001
BUSY GATE
D(1) RMT RF GAIN CONT
E(1)
P/O WORD 3
WORD 4
NOT USED
P/O J10
RESERVED
FINE TUNE
VBFO PAR ENBL
VBFO TUNE
SPARE
KEY IND
EXCTR RF IND
AFC LOCK IND
RF FAULT IND
RF OVLD IND
CPLR FAULT IND
RF OUT IND
PA FAULT IND
PA READY IND
RATE (1)
RATE (2)
RATE (4)
RATE (8)
RATE (16)
UP/DOWN
F(1)
P/O J9
STATUS REQ
CHAN B AGC PM
CHAN B RCV AF PM
CHAN B XMT AF PM
CHAN A AGC PM
CHAN A RCV AF PM
CHAN A XMT RF PM
XCTR RF IND
RT FAULT IND
PS FAULT IND
SYNTH FAULT IND
MON
LOC ENBL
DATA ERROR
PRESEL FAULT IND
VBFO SYNTH FAULT
P/O WORD 3
WORD 4
G(1)
P/O PARALLEL INPUT AI1
635-0751-002/642-3135-001
H(1) UPDATE
J(1) WD1S
K(1) WD2S
L(1) WD3S
M(1) WD4S
N(1) ADRS S

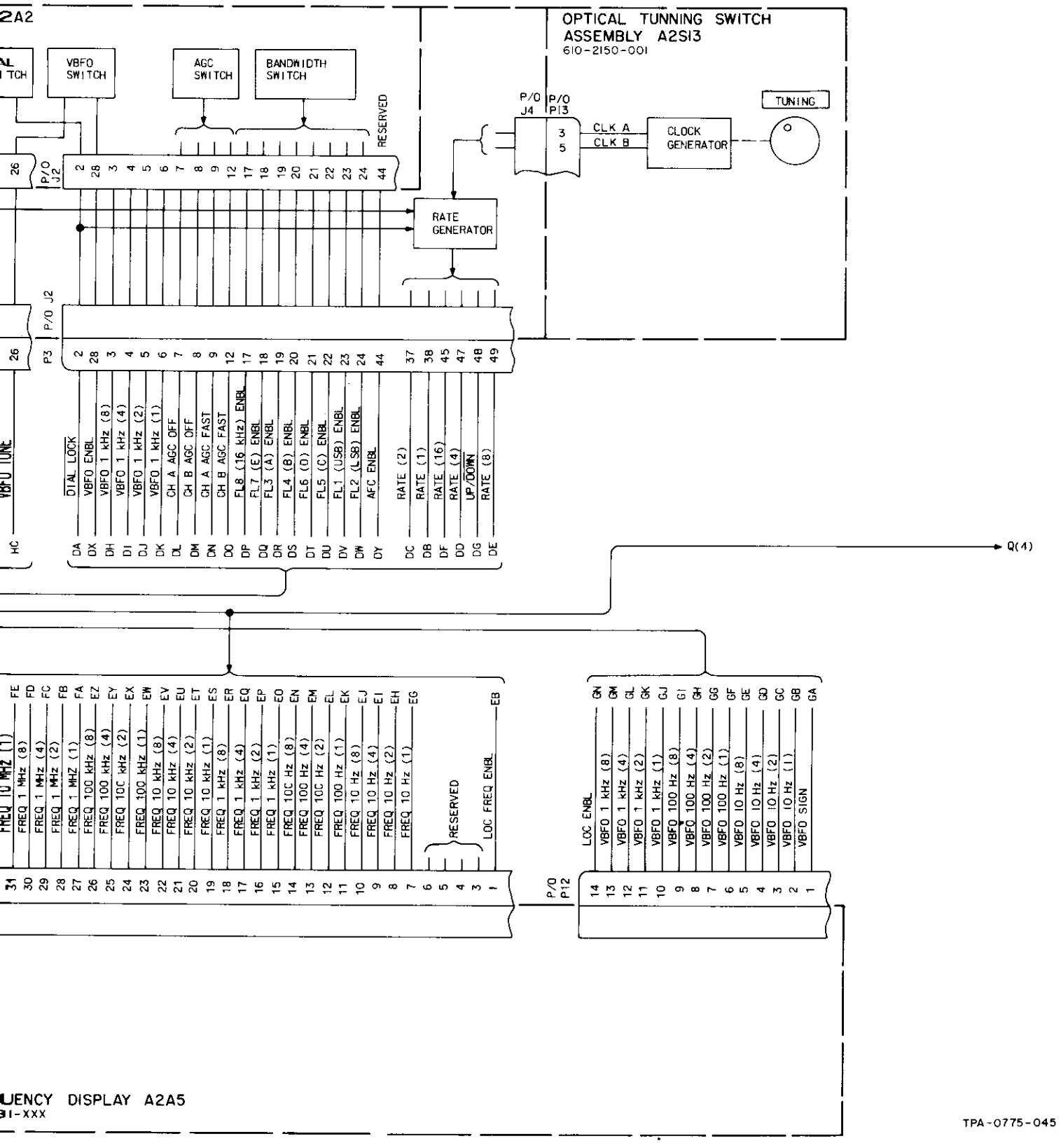

P/O MAIN CHASSIS
A3
(NOT USED)
VBFO A4
(OPTIONAL)
638-6067-001
P/O J10
P/O J1
P/O J2
P/O J8
P/O J9
BUSY GATE
NOT USED
RMT FREQ CHANGE
LOC ENBL
WD4R
UPDATE
BUSY IND
ADRS G
ADRS S
PRESET SEND
RMT RF GAIN CONT
STRAP 1
RT FAULT IND
STRAP 2
LOC FREQ ENBL
MON
PAR FREQ ENBL
AFC LOCK IND
AFC ENBL
VBFO SIGN
10 Hz (2)
10 Hz (8)
100 Hz (2)
100 Hz (4)
1 kHz (1)
1 kHz (4)
VBFO ENBL
10 Hz (1)
10 Hz (4)
100 Hz (1)
100 Hz (8)
1 kHz (2)
1 kHz (8)
VBFO CLOCK
VBFO DSPL ENBL
VBFO SYNTH FAULT
UP/DOWN
LOC ENBL
VBFO TUNE
VBFO PAR ENBL
VBFO LOAD
RESERVED
DATA ERROR
PRESEL FAULT IND
VBFO SYNTH FAULT
FREQ 10 MHz (2)
FREQ 10 MHz (1)
FREQ 1 MHz (8)
FREQ 1 MHz (4)
FREQ 1 MHz (2)
FREQ 1 MHz (1)
FREQ 100 kHz (8)
FREQ 100 kHz (4)
FREQ 100 kHz (2)
FREQ 100 kHz (1)
FREQ 10 kHz (8)
FREQ 10 kHz (4)
FREQ 10 kHz (2)
FREQ 10 kHz (1)
FREQ 1 kHz (8)
FREQ 1 kHz (4)
FREQ 1 kHz (2)
FREQ 1 kHz (1)
FREQ 100 Hz (8)
FREQ 100 Hz (4)
FREQ 100 Hz (2)
FREQ 100 Hz (1)
FREQ 10 Hz (8)
FREQ 10 Hz (4)
FREQ 10 Hz (2)
FREQ 10 Hz (1)
PAR FREQ ENBL
WD3G
VBFO CLK
WD1G
PRESEL FAULT IND
RF OVLD IND
RT FAULT IND
PRESEL CONT AND PA BAND SWITCHING
RESERVED
CONTROL A10
638-6065-001
UPDATE
WD1S
WD2S
WD3S
WD4S
ADRS S



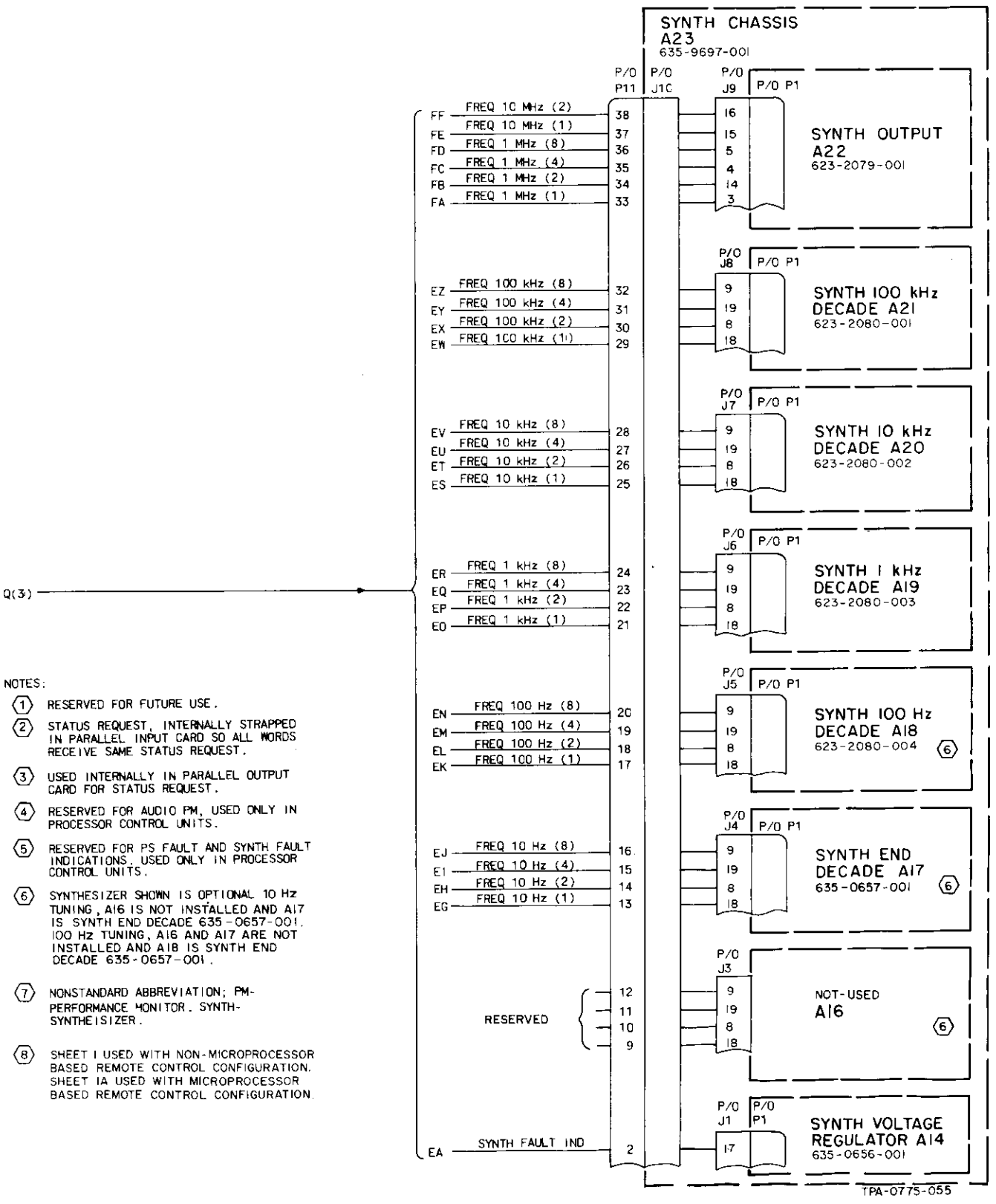
Remote Control, Block Diagram
Figure 8 (Sheet 2)


P (2)
P/O MAIN CHASSIS
P/O J12
DA
DB
DC
DD
DE
DF
DG
DH
DI
DJ
DK
DL
DM
DN
DO
DP
DQ
DR
DS
DT
DU
DV
DW
DX
DY
2 DIAL LOCK
38 RATE (1)
37 RATE (2)
47 RATE (4)
49 RATE (8)
45 RATE (16)
48 UP/DOWN
3 VBFO 1 kHz (8)
4 VBFO 1 kHz (4)
5 VBFO 1 kHz (2)
6 VBFO 1 kHz (1)
7 CHAN A AGC OFF
8 CHAN B AGC OFF
9 CHAN A AGC FAST
12 CHAN B AGC FAST
17 FL8 (16 kHz)
18 FL7 (E)
19 FL3 (A)
20 FL4 (B)
21 FL6 (D)
22 FL5 (C)
23 FL1 (USB)
24 FL2 (LSB)
28 VBFO ENBL
44 AFC ENBL
1
BX
BY
BZ
CA
CB
CC
BJ
BI
BH
BG
AP
AN
AO
AM
BA
AZ
AV
AW
AY
AX
AT
AU
AS
AR
P/O P6
CH AFC LOCK IND 3 HA
CI RT FAULT IND 5 HB
BW VBFO TUNE 34 HC
CO PRESEL FAULT IND 12 HD
CL RF OVLD IND 4 HE
BE AM ENBL 15 HF
BF FM ENBL 16 HG
BC CW ENBL 17 HH
BB LSB ENBL 18 HI
BV VBFO PAR ENBL 26 HJ
BU FINE TUNE 27 HK
BT RESERVED 28 HL
CM MON 30 HM
CN LOC ENBL 31 HN
BD SSB ENBL 14 HO
P/O J13
EA
EB
EC
ED
EE
EF
EG
EH
EI
EJ
EK
EL
EM
EN
EO
EP
2 SYNTH FAULT IND CK
7 LOC FREQ ENBL CZ
9
10
11
12 RESERVED
13 FREQ 10 Hz (1) AD
14 FREQ 10 Hz (2) AE
15 FREQ 10 Hz (4) AF
16 FREQ 10 Hz (8) AG
17 FREQ 100 Hz (1) R
18 FREQ 100 Hz (2) S
19 FREQ 100 Hz (4) T
20 FREQ 100 Hz (8) U
21 FREQ 1 kHz (1) V
22 FREQ 1 kHz (2) W
P/O J17
BK VBFO SIGN 1 GA
BL VBFO 10 Hz (1) 2 GB
BM VBFO 10 Hz (2) 3 GC
BN VBFO 10 Hz (4) 4 GD
BO VBFO 10 Hz (8) 5 GE
BP VBFO 100 Hz (1) 6 GF
BQ VBFO 100 Hz (2) 7 GG
BR VBFO 100 Hz (4) 8 GH
BS VBFO 100 Hz (8) 9 GI


BT MON 28 HL
CM LOC ENBL 30 HM
CN SSB ENBL 31 HN
BD 14 HO
P/O J17
BK VBFO SIGN 1 GA
BL VBFO 10 Hz (1) 2 GB
BM VBFO 10 Hz (2) 3 GC
BN VBFO 10 Hz (4) 4 GD
BO VBFO 10 Hz (8) 5 GE
BP VBFO 100 Hz (1) 6 GF
BQ VBFO 100 Hz (2) 7 GG
BR VBFO 100 Hz (4) 8 GH
BS VBFO 100 Hz (8) 9 GI
BG VBFO 1 kHz (1) 10 GJ
BH VBFO 1 kHz (2) 11 GK
BI VBFO 1 kHz (4) 12 GL
BJ VBFO 1 kHz (8) 13 GM
CN LOC ENBL 14 GN
EA 2 SYNTH FAULT IND CK
EB 7 LOC FREQ ENBL CZ
EC 9
ED 10 RESERVED
EE 11
EF 12
EG 13 FREQ 10 Hz (1) AD
EH 14 FREQ 10 Hz (2) AE
EI 15 FREQ 10 Hz (4) AF
EJ 16 FREQ 10 Hz (8) AG
EK 17 FREQ 100 Hz (1) R
EL 18 FREQ 100 Hz (2) S
EM 19 FREQ 100 Hz (4) T
EN 20 FREQ 100 Hz (8) U
EO 21 FREQ 1 kHz (1) V
EP 22 FREQ 1 kHz (2) W
EQ 23 FREQ 1 kHz (4) X
ER 24 FREQ 1 kHz (8) Y
ES 25 FREQ 10 kHz (1) J
ET 26 FREQ 10 kHz (2) K
EU 27 FREQ 10 kHz (4) L
EV 28 FREQ 10 kHz (8) M
EW 29 FREQ 100 kHz (1) N
EX 30 FREQ 100 kHz (2) O
EY 31 FREQ 100 kHz (4) P
EZ 32 FREQ 100 kHz (8) Q
FA 33 FREQ 1 MHz (1) B
FB 34 FREQ 1 MHz (2) C
FC 35 FREQ 1 MHz (4) D
FD 36 FREQ 1 MHz (8) E
FE 37 FREQ 10 MHz (1) F
FF 38 FREQ 10 MHz (2) G
LED STATUS DISPLAY A2A1
635-0825-008
P/O J3
P/O P5
1 ISB ENBL HI
2 CW ENBL HH
3 FM ENBL HG
4 AM ENBL HF
5 SSB ENBL HO
7 PRESEL FAULT IND HD
13 RT FAULT IND HB
14 RF OVLD IND HE
15 AFC LOCK IND HA
17 FL2 (LSB) ENBL DW
18 FL1 (USB) ENBL DV
19 FL5 (C) ENBL DU
20 FL6 (D) ENBL DT
21 FL4 (B) ENBL DS
22 FL3 (A) ENBL DR
23 FL7 (E) ENBL DQ
24 FL 8 (16 kHz) ENBL DP
FREQUENCY DISPLAY A2A5
637-1781-XXX
P/O J5
P/O P8
32 FREQ 10 MHz (2) FF
31 FREQ 10 MHz (1) FE
30 FREQ 1 MHz (8) FD
29 FREQ 1 MHz (4) FC
28 FREQ 1 MHz (2) FB
27 FREQ 1 MHz (1) FA
26 FREQ 100 kHz (8) EZ
25 FREQ 100 kHz (4) EY
24 FREQ 100 kHz (2) EX
23 FREQ 100 kHz (1) EW
22 FREQ 10 kHz (8) EV
21 FREQ 10 kHz (4) EU
20 FREQ 10 kHz (2) ET
19 FREQ 10 kHz (1) ES
18 FREQ 1 kHz (8) ER
17 FREQ 1 kHz (4) EQ
16 FREQ 1 kHz (2) EP
15 FREQ 1 kHz (1) EO
SWITCH MOUNTING BOARD A2A2
638-6060-001
P/O P4
P/O J1
HO SSB ENBL 6
HF AM ENBL 7
HG FM ENBL 8
HI ISB ENBL 10
HD PRESEL FAULT IND 4
EB LOC FREQ ENBL 21
HM MON 22
HN LOC ENBL 23
HH CW ENBL 9
HJ VBFO PAR ENBL 18
HK FINE TUNE 19
HL RESERVED 20
HC VBFO TUNE 26
P/O J1
6 MODE SWITCH
7
8
10
(NOT USED)
21 CONT SWITCH
22
23
(NOT USED)
19 DIAL SWITCH
26
P3
P/O J2
DA DIAL LOCK 2
DX VBFO ENBL 28
DH VBFO 1 kHz (8) 3
DI VBFO 1 kHz (4) 4
DJ VBFO 1 kHz (2) 5
DK VBFO 1 kHz (1) 6
DL CH A AGC OFF 7
DM CH B AGC OFF 8
DN CH A AGC FAST 9
DO CH B AGC FAST 12
DP FL8 (16 kHz) ENBL 17
DQ FL7 (E) ENBL 18
DR FL3 (A) ENBL 19
P/O J2
2 VBFO SWITCH
28
3
4
5
6
7 AGC SWITCH
8
9
12
17
18 BAN SWI
19



Remote Control, Block Diagram
Figure 8 (Sheet 3)



NOTES:

1. RESERVED FOR FUTURE USE.
2. STATUS REQUEST, INTERNALLY STRAPPED IN PARALLEL INPUT CARD SO ALL WORDS RECEIVE SAME STATUS REQUEST.
3. USED INTERNALLY IN PARALLEL OUTPUT CARD FOR STATUS REQUEST.
4. RESERVED FOR AUDIO PM, USED ONLY IN PROCESSOR CONTROL UNITS.
5. RESERVED FOR PS FAULT AND SYNTH FAULT INDICATIONS, USED ONLY IN PROCESSOR CONTROL UNITS.
6. SYNTHESIZER SHOWN IS OPTIONAL 10 Hz TUNING, A16 IS NOT INSTALLED AND A17 IS SYNTH END DECADE 635-0657-001. 100 Hz TUNING, A16 AND A17 ARE NOT INSTALLED AND A18 IS SYNTH END DECADE 635-0657-001.
7. NONSTANDARD ABBREVIATION; PM-PERFORMANCE MONITOR, SYNTH-SYNTHESIZER.
8. SHEET 1 USED WITH NON-MICROPROCESSOR BASED REMOTE CONTROL CONFIGURATION. SHEET 1A USED WITH MICROPROCESSOR BASED REMOTE CONTROL CONFIGURATION.

Remote Control, Block Diagram
Figure 8 (Sheet 4)

2.4 Frequency Synthesizer

2.4.1 General (Refer to figure 9.)

The frequency synthesizer used in the 851S-( ) equipments is accuracy controlled by the number of decades used and is adaptable to 10- or 100-Hz control, when used with the associated decades. The frequency synthesizer uses a 9.9-MHz TCXO (temperature compensated crystal oscillator) as a base for generating the required synthesizer frequencies. Using dividers and a multiplier, the synthesizer produces the following fixed frequencies:

a. 9.9-MHz injection frequency
b. 118.8-MHz injection frequency
c. 450-kHz carrier reinsertion frequency
d. 100-kHz synthesizer reference frequency

Using the 100-kHz synthesizer reference frequency and the associated decades, the variable injection frequency for the selected output frequency is generated. The variable injection frequency is 109.350000 to 79.350001 MHz (the higher the selected output frequency, the lower the variable injection frequency). Note that figure 9 shows the synthesizer complement for 10- and 100-Hz tuning.

2.4.2 Synthesizer Reference (Refer to figure 10.)

The synthesizer reference A15 uses a 9.9-MHz TCXO) as a base for generating the required synthesizer frequencies. When used with an external reference, the 9.9-MHz TCXO is supplied with a tracking voltage generated by the 100-kHz reference signal and the external frequency standard. When not used with the external reference, an internal temperature compensation network is used to maintain a constant frequency output from the TCXO.

The 9.9-MHz TCXO output is supplied through an output amplifier and used as 9.9-MHz fixed injection input.

The 9.9-MHz TCXO output is applied to a times-12 circuit which produces a 118.8-MHz fixed injection input.

The 9.9-MHz TCXO output is applied to a divide-by-11 circuit that produces a 900-kHz base frequency. The 900-kHz base frequency is applied to a divide-by-2 circuit that produces a 450-kHz carrier reinsertion input. The 900-kHz base frequency is also applied to a divide-by-9 circuit that produces two 100-kHz reference outputs. The 100-kHz reference frequency outputs are applied to each of the synthesizer decades as a reference for variable injection frequency generation.

2.4.3 Synthesizer End Decade (Refer to figure 10.)

The synthesizer end decade receives bcd inputs and a fixed 100-kHz reference signal and provides a 0.60- to 0.51-MHz variable reference output to the next decade step.

The synthesizer end decade can be used as the 10- or 100-Hz decade to provide the appropriate reference frequency to the next decade in the synthesizer. As implied by its name, it is the end decade; that is, if used as a 10-Hz decade it provides 10-Hz tuning (accuracy) and if used as a 100-Hz decade it provides 100-Hz tuning (accuracy).

The synthesizer and decade contains a phase-lock loop consisting of a phase/frequency discriminator, variable vco, variable divider, and a lock detector. The 100-kHz reference signal is applied to the phase/frequency discriminator where it is compared with the 100-kHz signal from the variable divider. The phase/frequency discriminator develops a tracking voltage output (based on the phase/frequency difference of the 100-kHz signals). The tracking voltage drives the variable vco to the frequency as determined by the bcd input (programmed division ratio of variable divider).

The variable vco signal is divided (division ratio of the variable divider) and applied as 100-kHz variable reference to the phase/frequency discriminator. When the inputs to the phase/frequency discriminator are the same frequency and in phase, a lock signal output is supplied.

The variable vco signal is applied to the fixed divide-by-10 output circuit and the 0.60- to 0.51-MHz end decade output signal is supplied to the next decade step.

2.4.4 Synthesizer Decades (Refer to figure 10.)

The synthesizer decade receives bcd inputs, a fixed 100-kHz reference signal, and a variable high reference signal, and provides a variable reference signal to the next decade step. Refer to table 2 for the input/output difference of the synthesizer decades.

The synthesizer decades differ only in strapping and vco coils. These differences result in the different input and output frequencies, as shown in table 2.

These synthesizer decades can be used as the 100-Hz decade and are used as the 1-, 10-, and 100-kHz decades to provide the appropriate reference frequency for the next decade in the synthesizer. For 10-Hz tuning, one 100/10-Hz decade is used as the 100-Hz decade. For 100-Hz tuning, no 100/10-Hz decade is used.

Table 2. Decade Versus Input/Output Frequencies.

DECADE	HI REF INPUT FREQ (MHz)	HI REF OUTPUT FREQ (MHz)
100 kHz	0.85 to 0.750001	1.035 to 0.935001
10 kHz	0.70 to 0.60001	0.85 to 0.750001
1 kHz	0.60 to 0.5001	0.70 to 0.60001
100 Hz	0.60 to 0.501	0.60 to 0.5001
10 Hz	0.60 to 0.51	0.60 to 0.501

The synthesizer decade contains two phase-lock loops. The translator phase-lock loop consists of a phase/frequency discriminator, variable vco, variable divider, and a lock detector. The 100-kHz reference signal is applied to the phase/frequency discriminator where it is compared with the 100-kHz signal from the variable divider. The phase/frequency discriminator develops a tracking voltage output based on the phase/frequency difference of the 100-kHz signals. The tracking voltage drives the variable vco to the frequency, as determined by the bcd input (programmed division ratio of variable divider). The tracking voltage is also applied as a reference voltage to the variable vco in the output phase-lock loop. The variable vco signal output in the translator phase-lock loop is applied to the mixer in the output phase-lock loop.

The variable vco signal output in the translator phase-lock loop is also divided (division ratio of the variable divider) and applied as 100-kHz variable reference to phase/frequency discriminator. When the inputs to the phase/frequency discriminator are the same frequency and in phase, a translator lock signal output is supplied.

The output phase-lock loop consists of a phase/frequency discriminator, variable vco, mixer and squaring amplifier, and a lock detector. A high reference signal (refer to table 2) is applied to the phase/frequency discriminator where it is compared with the difference frequency from the mixer. The phase/frequency discriminator develops a tracking voltage output based on the phase/frequency difference of the high reference signal and the difference frequency from the mixer. The tracking voltage drives the variable vco to the frequency, as determined by the high reference input and the reference voltage supplied by the translator phase-lock loop. The variable vco signal, in the output phase-lock loop, is supplied to a fixed divide-by-10 output circuit, and the output of the divide-by-10 network is supplied to the next decade step.

The variable vco signal, in the output phase-lock loop, is also mixed with the variable vco signal of the translator phase-lock loop, and a difference frequency reference is supplied through a squaring amplifier and applied to the phase/frequency discriminator. When the inputs to the phase/frequency discriminator are the same frequency and in phase, an output lock signal output is supplied.

When lock signals are supplied by both the translator and output phase-lock loops, they are ANDed and supply a decade lock signal output.

2.4.5 Synthesizer Output (Refer to figure 10.)

The synthesizer output A22 receives units/tens MHz bcd inputs, a fixed 100-kHz reference signal, and a variable high reference signal, and provides a 109.35- to 79.350001-MHz variable injection signal output to the unit under control.

The synthesizer output A22 contains two phase-lock loops. The translator phase-lock loop consists of a phase/frequency discriminator, variable vco, variable divider, voltage/gain control, and a lock detector. The 100-kHz reference signal is applied to the phase/frequency discriminator where it is compared with the 100-kHz signal from the variable divider. The phase/frequency discriminator develops a tracking voltage based on the phase/frequency difference of the 100-kHz signals and the operation of the voltage/gain control circuit caused by the 10- and 20-MHz bcd inputs. The tracking voltage drives the variable vco to the frequency as determined by the bcd input (programmed division ratio of variable divider). The tracking voltage is also applied as a reference voltage to the voltage/gain control in the

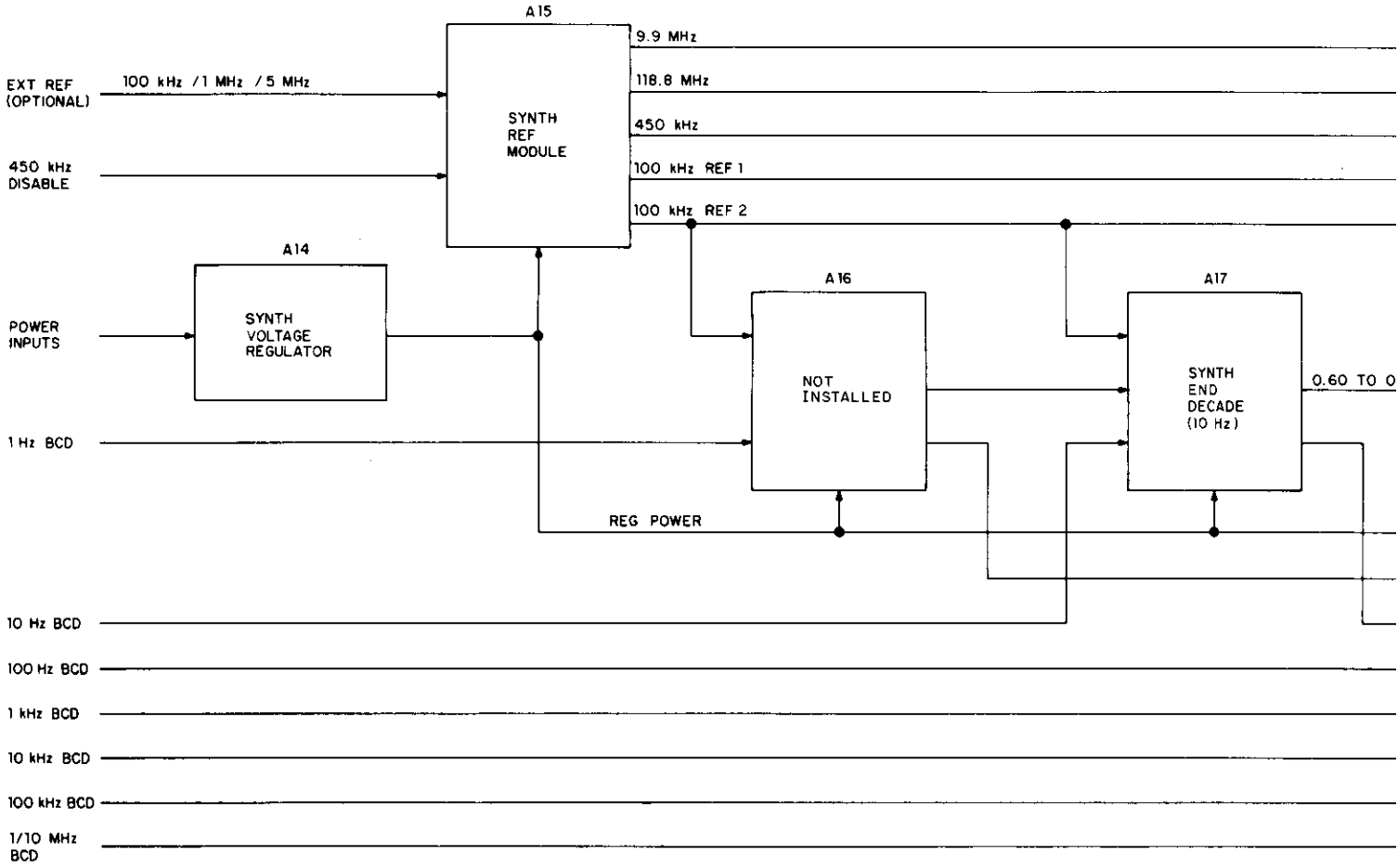
output phase-lock loop. The variable vco signal output in the translator phase-lock loop is applied to the mixer in the output phase-lock loop.

The variable vco signal output in the translator phase-lock loop is also divided (division ratio of the variable divider) and applied as 100-kHz variable reference to the phase/frequency discriminator. When the inputs to the phase/frequency discriminator are the same frequency and in phase, a translator lock signal output is supplied.

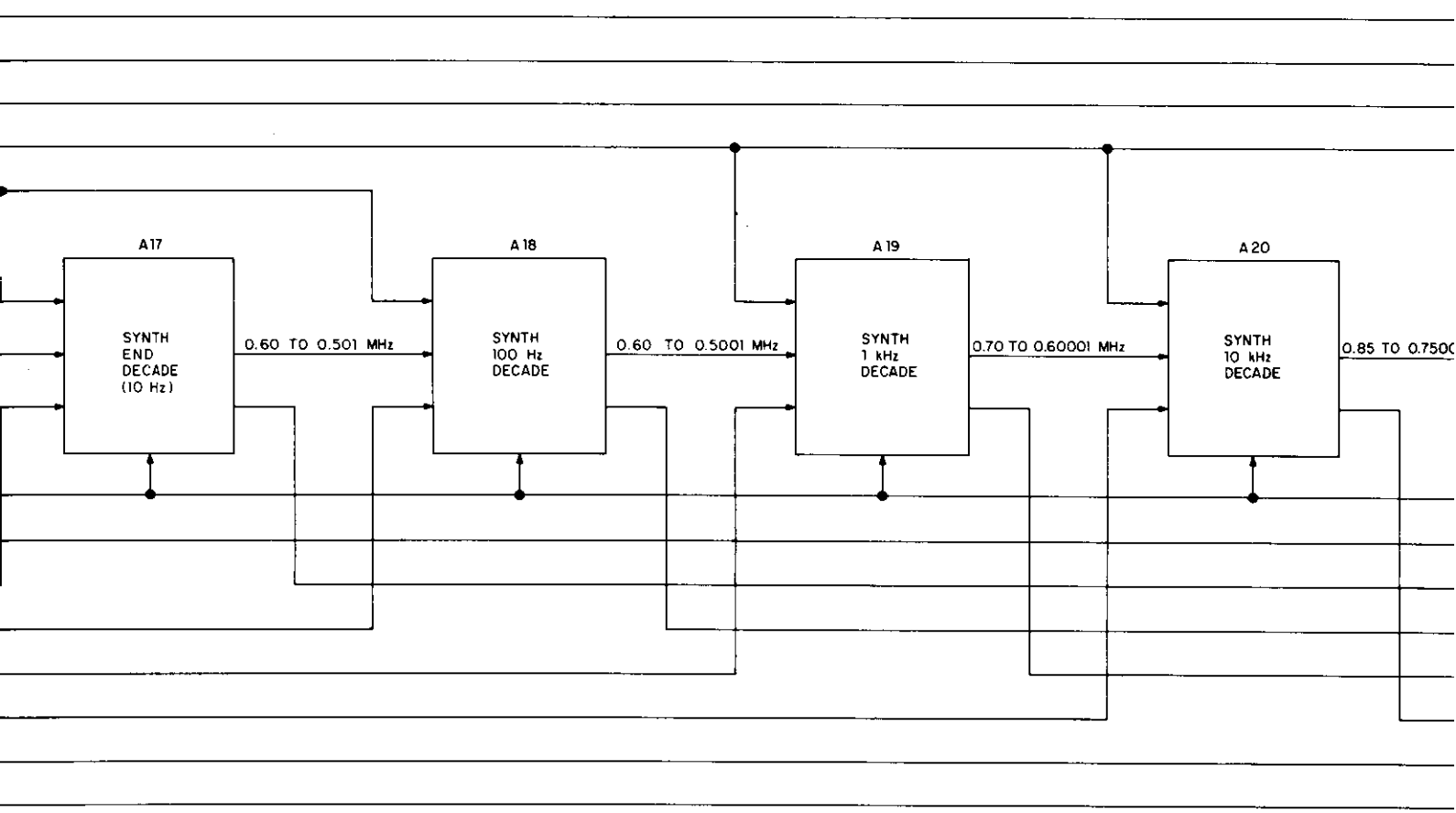
The output phase-lock loop consists of a phase/frequency discriminator, variable vco, mixer and squaring amplifier, voltage/gain control, and a lock detector. A high reference signal is applied to the phase/frequency discriminator where it is compared with the difference frequency from the mixer. The phase/frequency discriminator develops a tracking voltage output based on the phase/frequency difference of the high reference signal and the difference frequency from the mixer, and the operation of the voltage/gain control circuit caused by the translator phase-lock loop tracking voltage. The tracking voltage drives the variable vco to the frequency, as determined by the high reference input, and the reference voltage supplied by the translator phase-lock loop is supplied to the unit under control as the variable injection control signal.

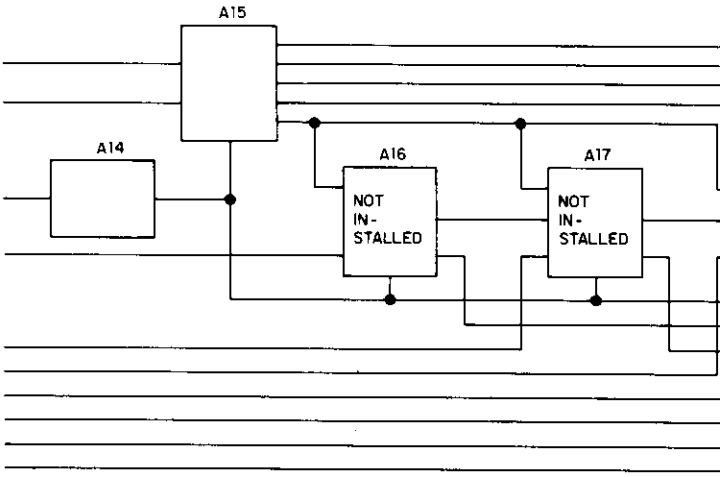
The variable vco signal in the output phase-lock loop is also mixed with the variable vco signal of the translator phase-lock loop, and a difference frequency reference is supplied through a squaring amplifier and applied to the phase/frequency discriminator. When the inputs to the phase/frequency discriminator are the same frequency and in phase, an output lock signal output is supplied.

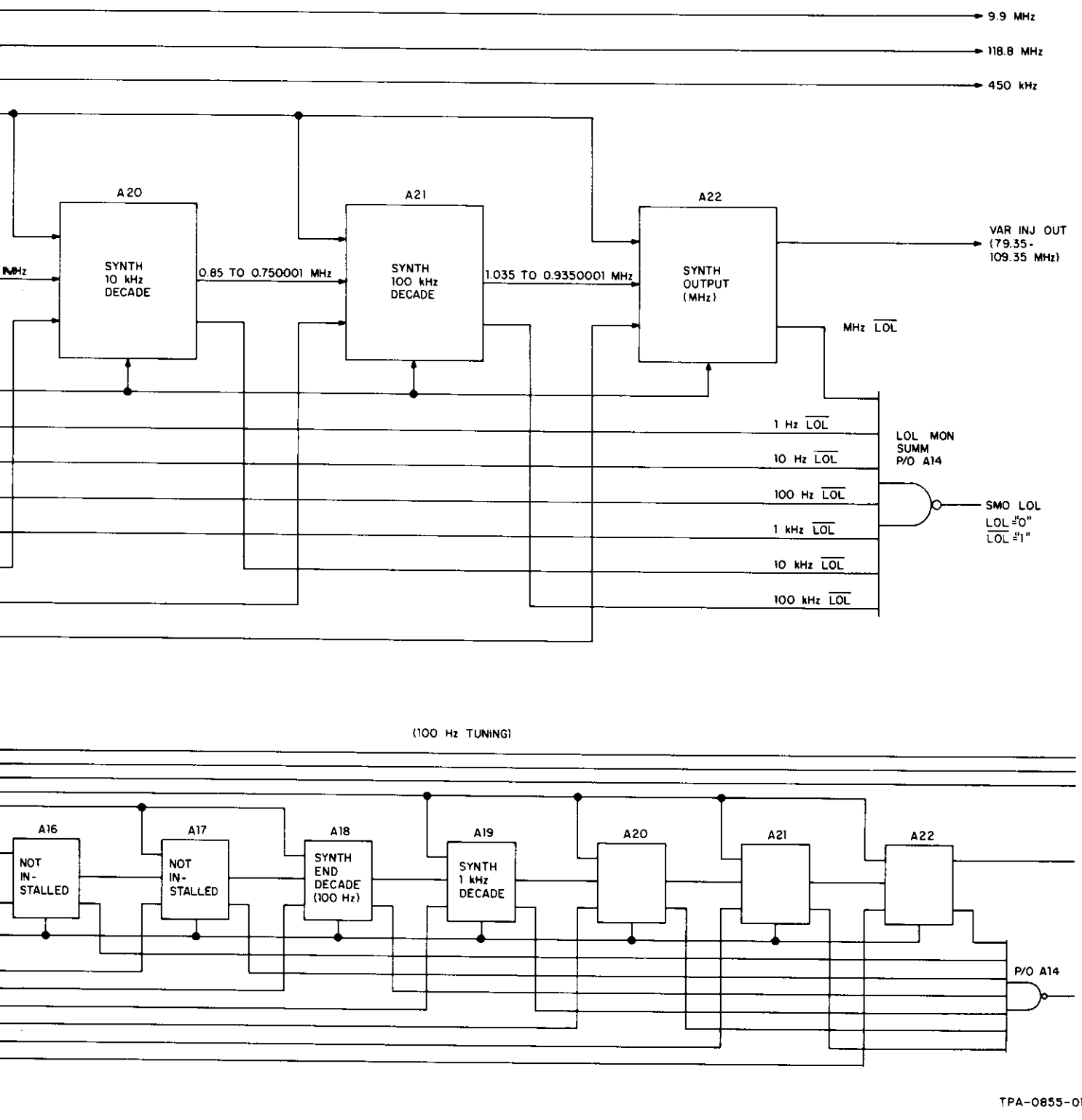
When lock signals are supplied by both the translator and output phase-lock loops, they are ANDed and supply a MHz decade lock signal output.


A15
SYNTH
REF
MODULE
EXT REF
(OPTIONAL)
100 kHz / 1 MHz / 5 MHz
450 kHz
DISABLE
9.9 MHz
118.8 MHz
450 kHz
100 kHz REF 1
100 kHz REF 2
A14
SYNTH
VOLTAGE
REGULATOR
POWER
INPUTS
A16
NOT
INSTALLED
A17
SYNTH
END
DECADE
(10 Hz)
0.60 TO 0
1 Hz BCD
REG POWER
10 Hz BCD
100 Hz BCD
1 kHz BCD
10 kHz BCD
100 kHz BCD
1/10 MHz
BCD

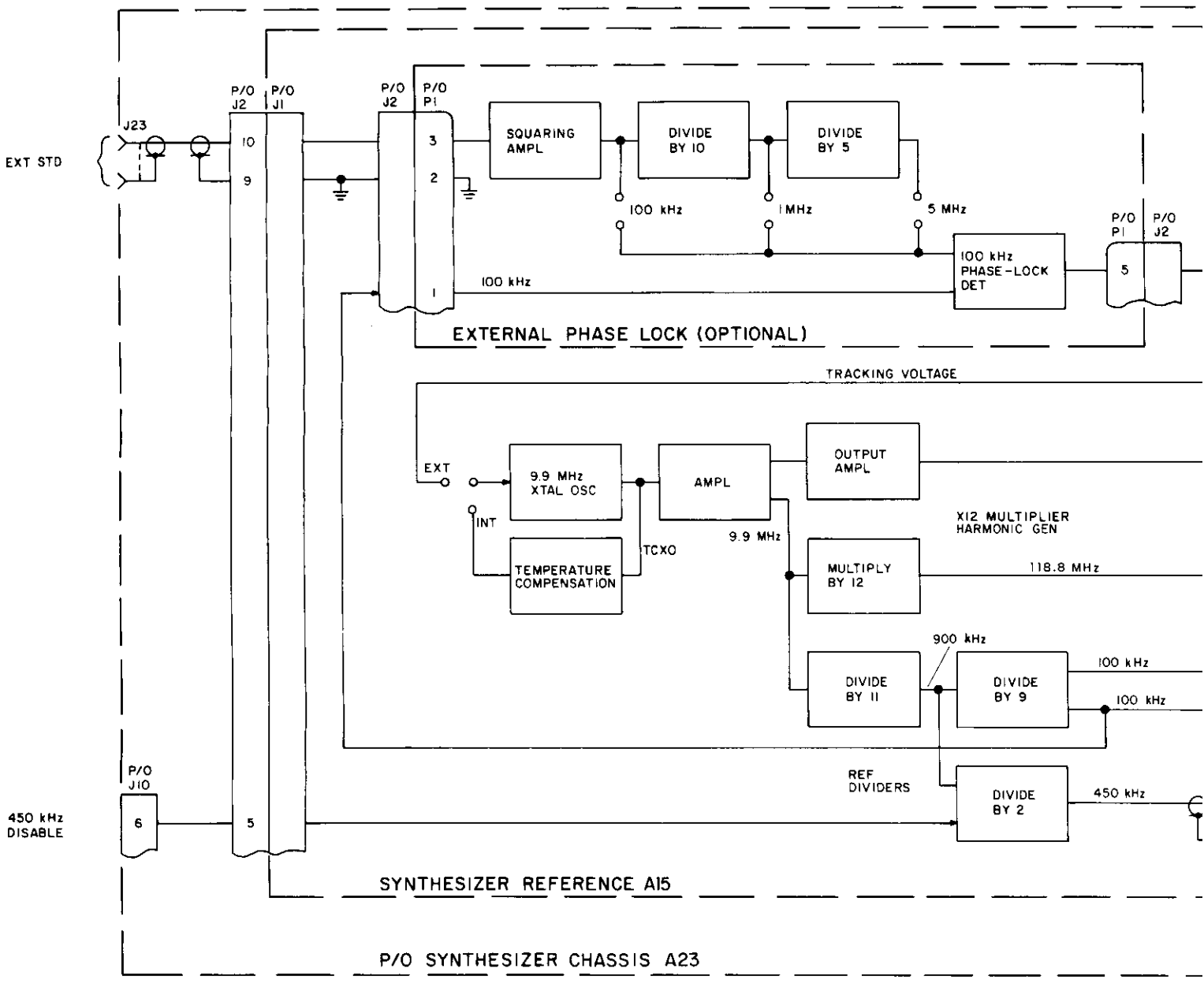
(10 Hz TUNING)

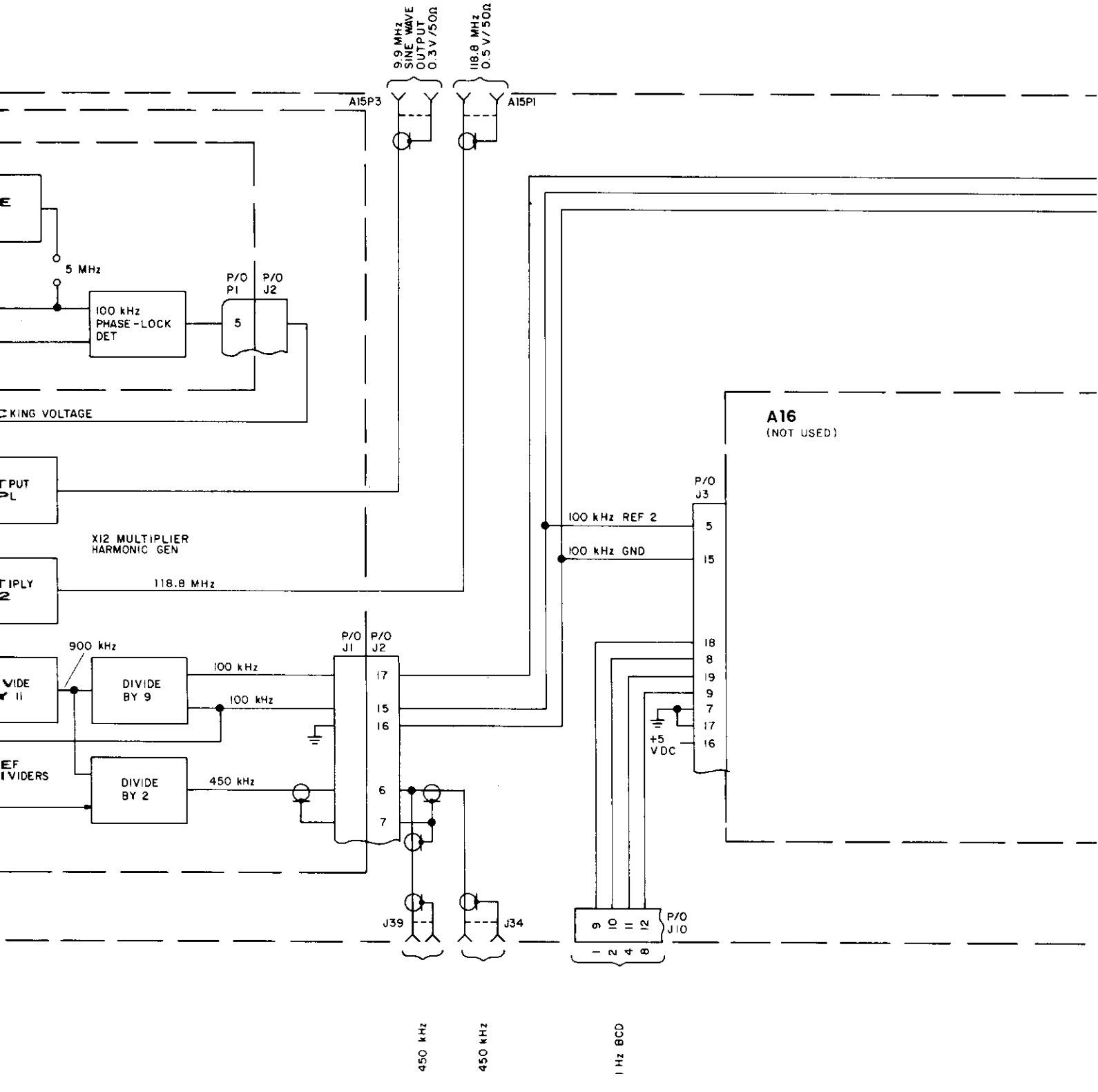

A17
SYNTH
END
DECADE
(10 Hz)
0.60 TO 0.501 MHz
A18
SYNTH
100 Hz
DECADE
0.60 TO 0.5001 MHz
A19
SYNTH
1 kHz
DECADE
0.70 TO 0.60001 MHz
A20
SYNTH
10 kHz
DECADE
0.85 TO 0.7500

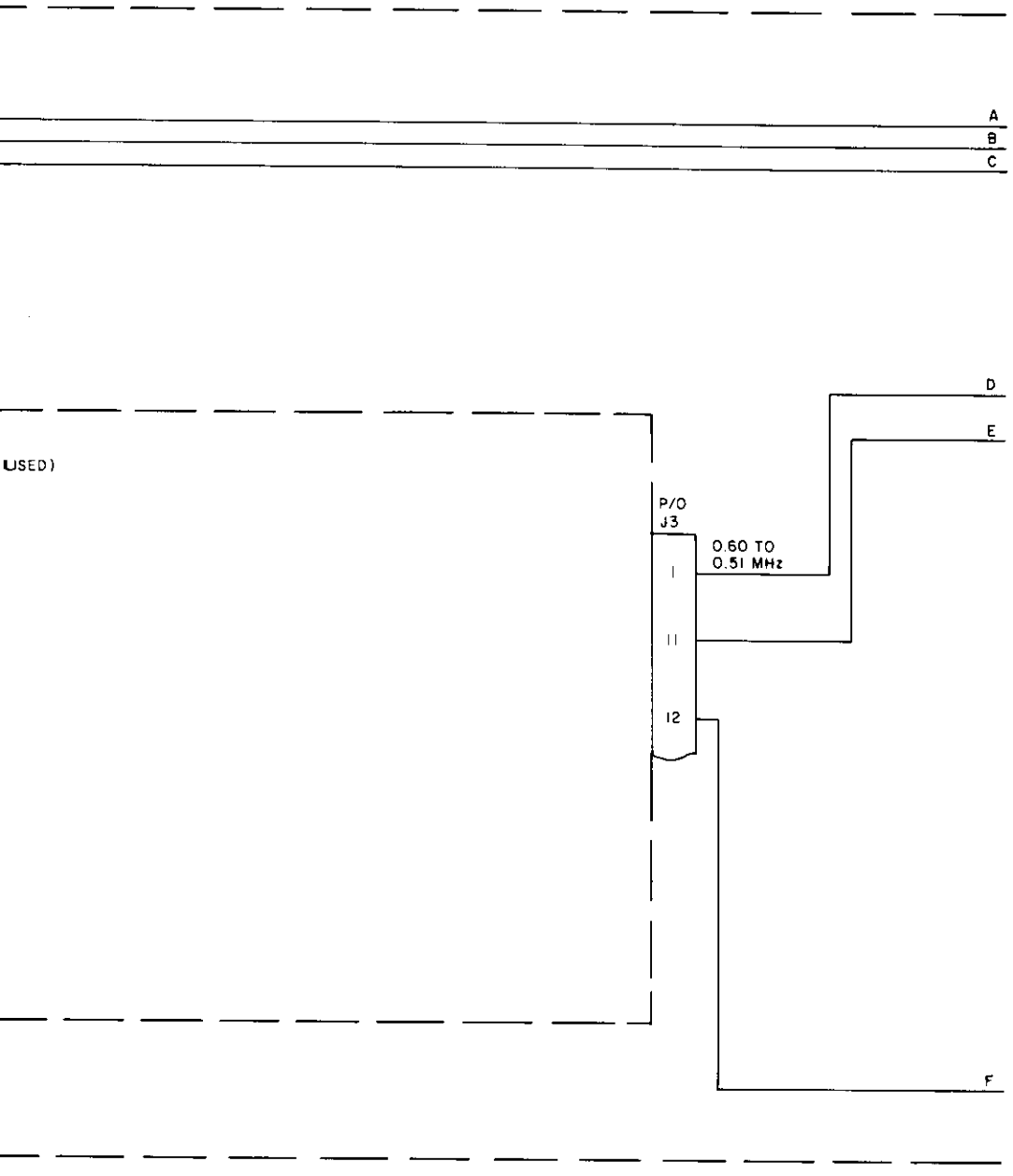

A15
A14
A16
NOT
IN-
STALLED
A17
NOT
IN-
STALLED



Frequency Synthesizer, Simplified Block Diagram
Figure 9


EXT STD
J23
P/O J2
P/O J1
10
9
P/O J2
P/O P1
3
2
1
SQUARING AMPL
DIVIDE BY 10
DIVIDE BY 5
100 kHz
1 MHz
5 MHz
100 kHz PHASE-LOCK DET
P/O P1
P/O J2
5
100 kHz
EXTERNAL PHASE LOCK (OPTIONAL)
TRACKING VOLTAGE
EXT
INT
9.9 MHz XTAL OSC
TEMPERATURE COMPENSATION
TCXO
AMPL
9.9 MHz
OUTPUT AMPL
X12 MULTIPLIER HARMONIC GEN
MULTIPLY BY 12
118.8 MHz
900 kHz
DIVIDE BY 11
DIVIDE BY 9
100 kHz
100 kHz
REF DIVIDERS
DIVIDE BY 2
450 kHz
P/O J10
6
5
450 kHz DISABLE
SYNTHESIZER REFERENCE A15
P/O SYNTHESIZER CHASSIS A23


9.9 MHz SINE WAVE OUTPUT 0.3 V/50Ω
118.8 MHz 0.5 V/50Ω
A15P3
A15P1
5 MHz
100 kHz PHASE-LOCK DET
P/O P1
P/O J2
5
KING VOLTAGE
X12 MULTIPLIER HARMONIC GEN
118.8 MHz
900 kHz
DIVIDE BY 9
DIVIDE BY 2
100 kHz
100 kHz
450 kHz
P/O J1
P/O J2
17
15
16
6
7
A16
(NOT USED)
P/O J3
100 kHz REF 2
100 kHz GND
5
15
18
8
19
9
7
17
16
+5 VDC
J39
J34
P/O J10
9
10
11
12
1
2
4
8
450 kHz
450 kHz
1 Hz BCD



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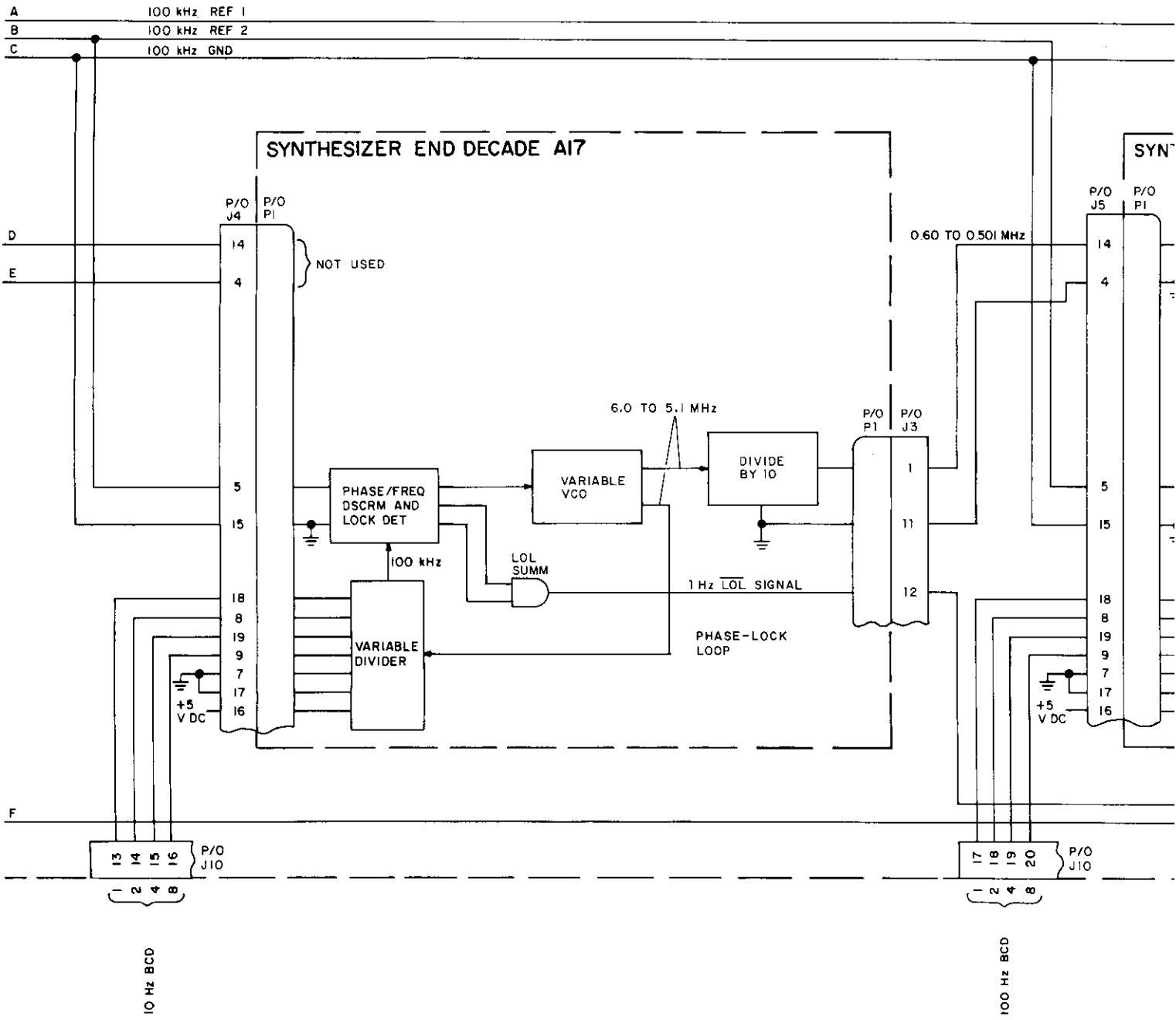
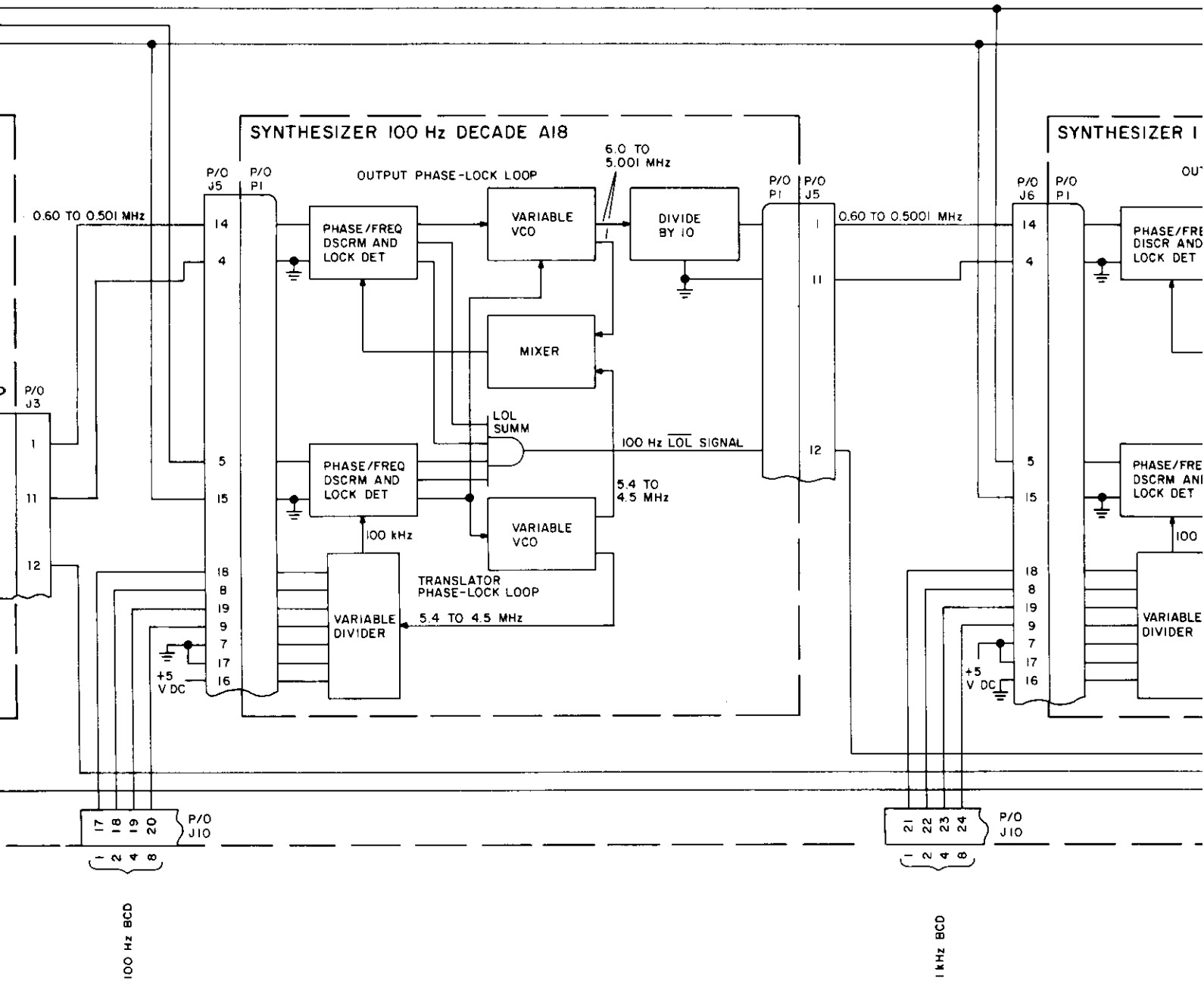
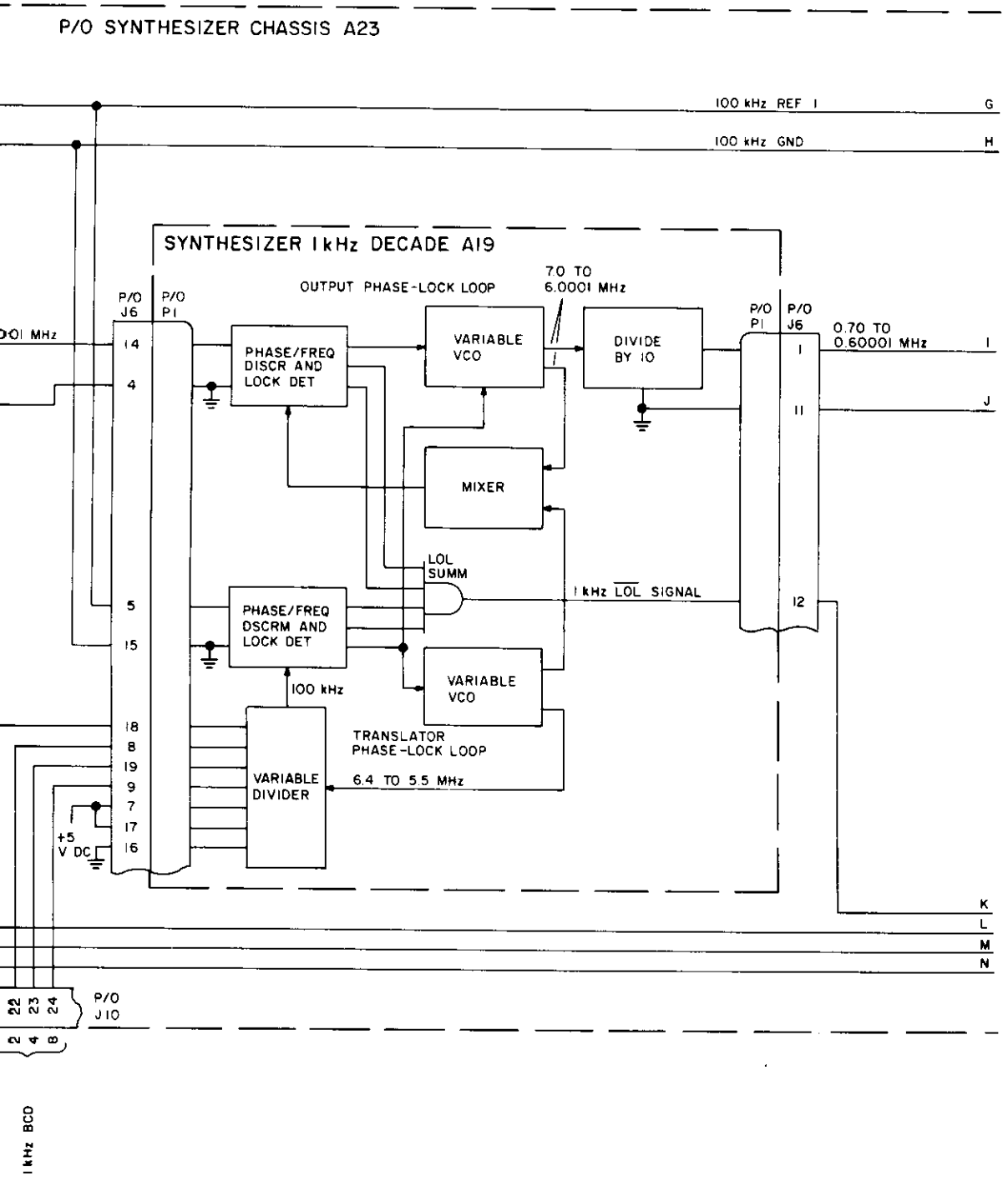
Frequency Synthesizer, Block Diagram
Figure 10 (Sheet 1 of 3)


A
100 kHz REF 1
B
100 kHz REF 2
C
100 kHz GND
SYNTHESIZER END DECADE A17
P/O J4
P/O P1
D
E
14
4
NOT USED
5
15
18
8
19
9
7
17
16
+5 V DC
PHASE/FREQ DSCRM AND LOCK DET
100 kHz
VARIABLE VCO
6.0 TO 5.1 MHz
DIVIDE BY 10
LOL SUMM
1 Hz LOL SIGNAL
VARIABLE DIVIDER
PHASE-LOCK LOOP
P/O P1
P/O J3
1
11
12
0.60 TO 0.501 MHz
P/O J5
P/O P1
F
13 14 15 16
P/O J10
1 2 4 8
10 Hz BCD
17 18 19 20
P/O J10
1 2 4 8
100 Hz BCD


SYNTHESIZER 100 Hz DECADE A18
SYNTHESIZER I
OUTPUT PHASE-LOCK LOOP
6.0 TO 5.001 MHz
0.60 TO 0.501 MHz
0.60 TO 0.5001 MHz
P/O J5
P/O P1
P/O J6
P/O J3
PHASE/FREQ DSCRM AND LOCK DET
VARIABLE VCO
DIVIDE BY 10
MIXER
LOL SUMM
100 Hz LOL SIGNAL
5.4 TO 4.5 MHz
100 kHz
TRANSLATOR PHASE-LOCK LOOP
VARIABLE DIVIDER
+5 V DC
P/O J10
100 Hz BCD
1 kHz BCD



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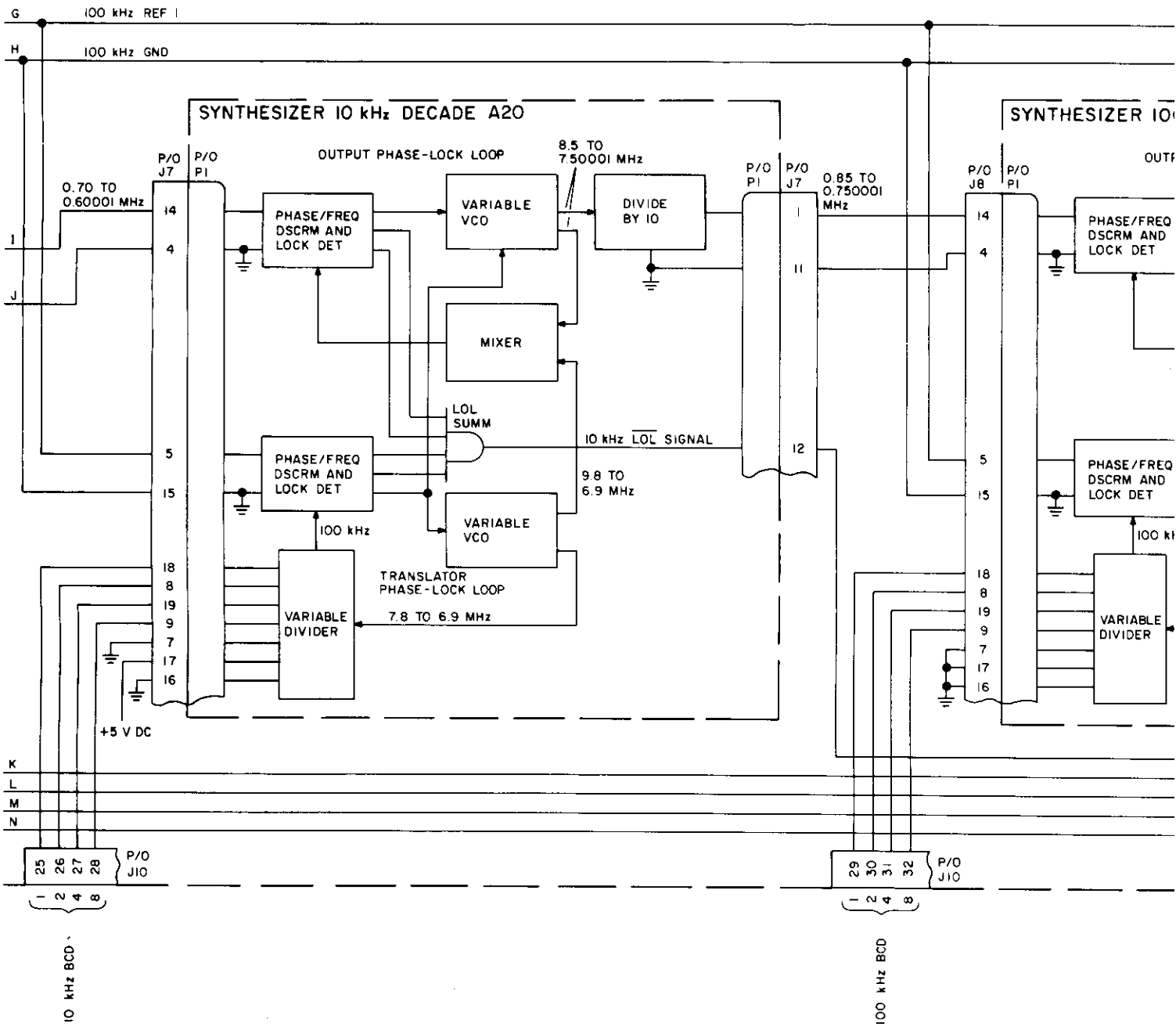
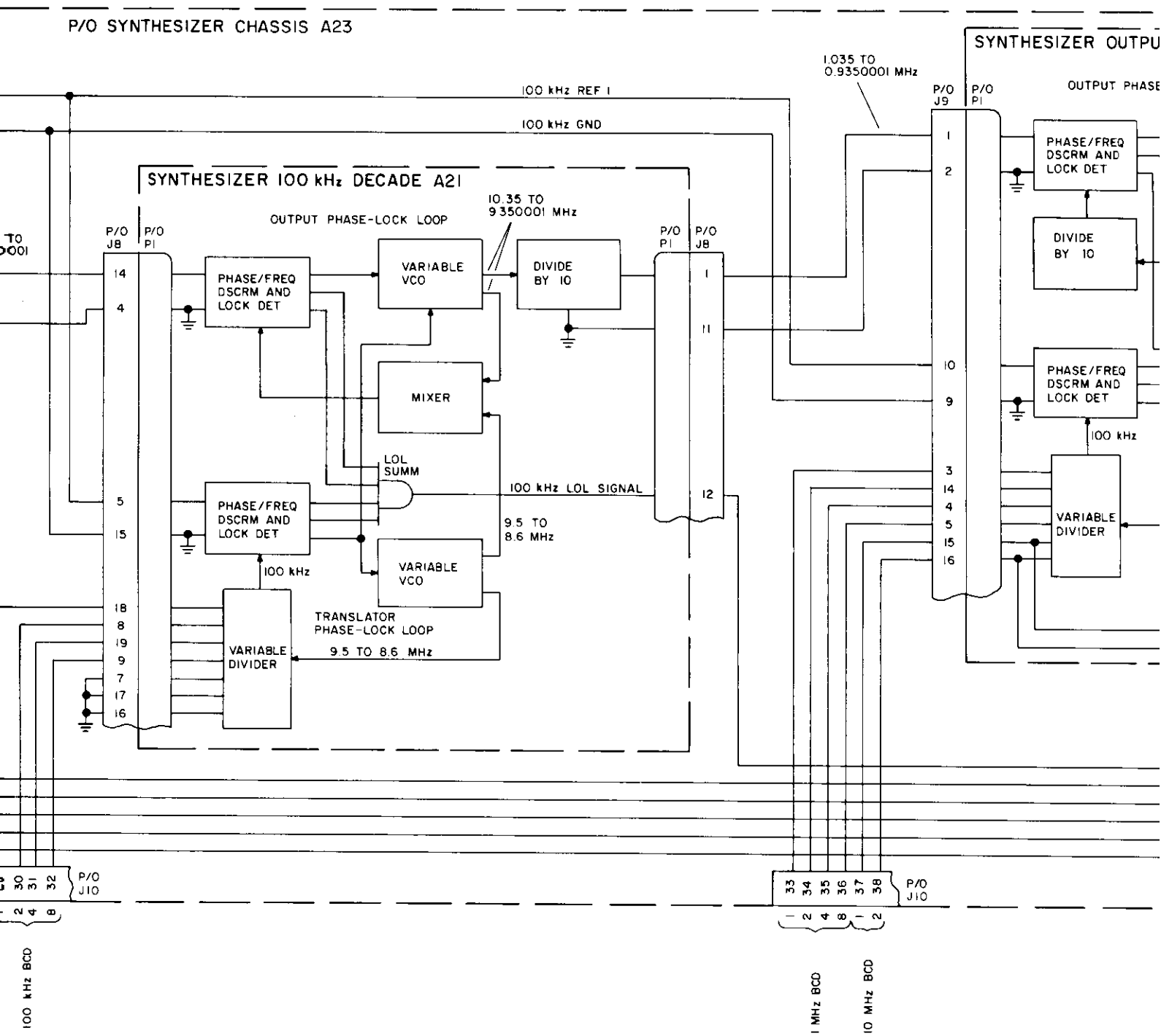
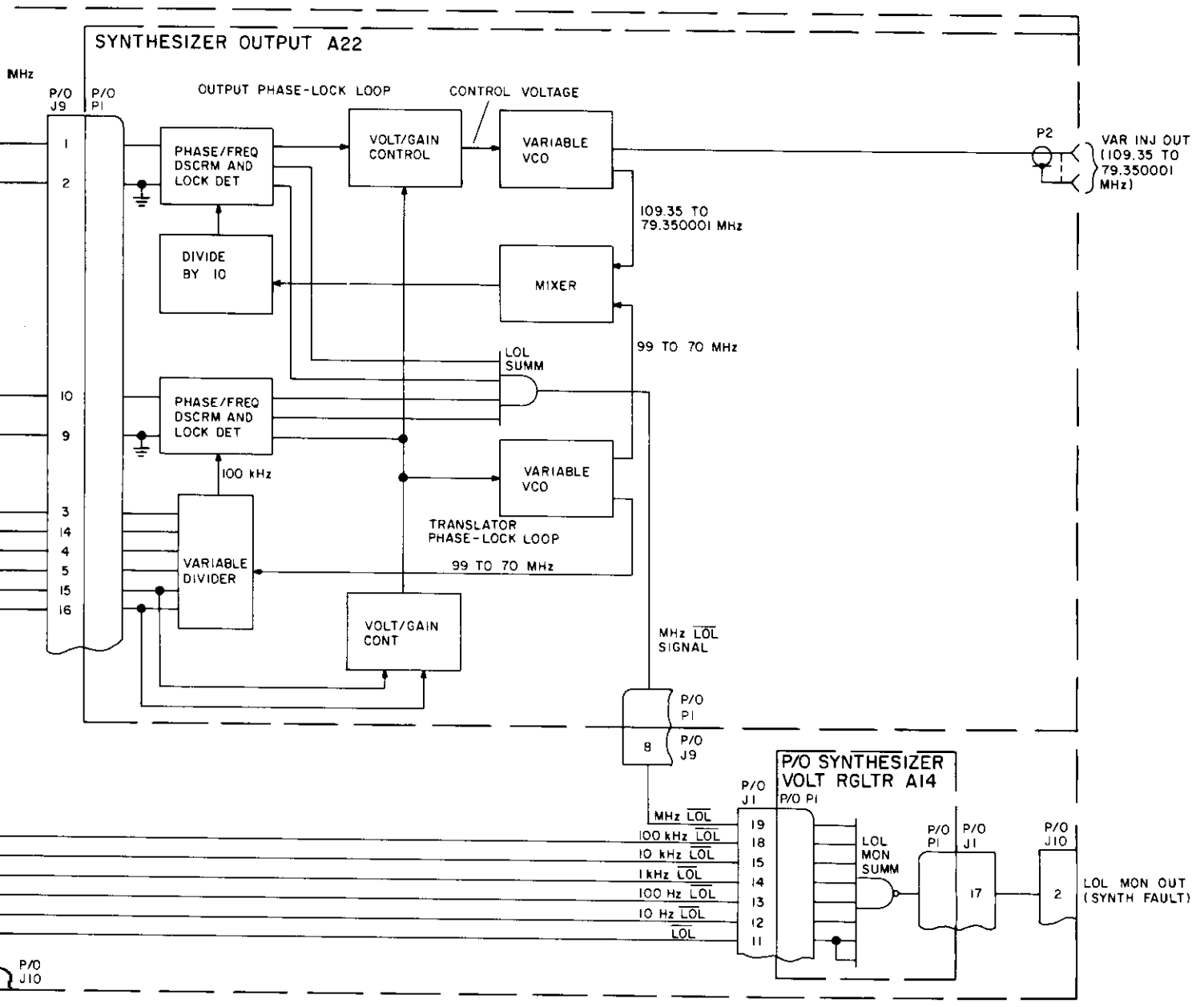
Frequency Synthesizer, Block Diagram
Figure 10 (Sheet 2)


G
100 kHz REF I
H
100 kHz GND
SYNTHESIZER 10 kHz DECADE A20
SYNTHESIZER 10
P/O J7
P/O P1
OUTPUT PHASE-LOCK LOOP
8.5 TO 7.50001 MHz
0.70 TO 0.60001 MHz
PHASE/FREQ DSCRM AND LOCK DET
VARIABLE VCO
DIVIDE BY 10
P/O P1
P/O J7
0.85 TO 0.750001 MHz
P/O J8
P/O P1
MIXER
LOL SUMM
10 kHz LOL SIGNAL
9.8 TO 6.9 MHz
100 kHz
VARIABLE VCO
TRANSLATOR PHASE-LOCK LOOP
7.8 TO 6.9 MHz
VARIABLE DIVIDER
+5 V DC
I
J
K
L
M
N
14
4
5
15
18
8
19
9
7
17
16
1
11
12
P/O J10
25
26
27
28
29
30
31
32
1
2
4
8
10 kHz BCD
100 kHz BCD


P/O SYNTHESIZER CHASSIS A23
SYNTHESIZER OUTPU
1.035 TO 0.9350001 MHz
100 kHz REF I
100 kHz GND
SYNTHESIZER 100 kHz DECADE A21
10.35 TO 9.350001 MHz
OUTPUT PHASE-LOCK LOOP
P/O J8
P/O P1
P/O J9
P/O P1
PHASE/FREQ DSCRM AND LOCK DET
VARIABLE VCO
DIVIDE BY 10
MIXER
LOL SUMM
100 kHz LOL SIGNAL
9.5 TO 8.6 MHz
100 kHz
VARIABLE DIVIDER
TRANSLATOR PHASE-LOCK LOOP
9.5 TO 8.6 MHz
P/O J10
100 kHz BCD
1 MHz BCD
10 MHz BCD



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Frequency Synthesizer, Block Diagram
Figure 10 (Sheet 3)

2.5 Monitor Functions (Refer to figure 11.)

Local monitors in the receiver consist of LEDs on LED status display A2A1 and frequency display A2A3, and the front panel meter indications. All front panel monitor information and some additional monitor information is contained in the monitor data supplied by the remote controlled receiver to a control/display station. Likewise, some control information is supplied to the remote controlled receiver from a control station. Using the 8-bit character word format or 7-bit ASCII word format, monitor information supplied to the parallel input is transmitted to a control/display station and control information supplied from the parallel output is received from a control station. Refer to table 3 for location of signals in control/monitor word format.)

2.5.1 Fault and Status Indicators

All fault and status indicators are lit by a logic 1 signal to LED status display A2A1. Refer to the LED status display section of this instruction book for detailed information.

a. RCV FAULT (DS5) is lit by a receive fault signal at A2J3-13. The logic 1 receive fault signal is supplied by control A10. In the remote controlled receiver, the receive fault signal is also supplied to the parallel input A11. The receive fault signal from control A10 is a summary of a power supply fault signal, a synthesizer fault signal (smo lol), and a vbfo synthesizer fault signal.

   A logic 0 power supply fault signal is supplied by power supply A1. In the remote controlled receiver, the power supply fault signal is also supplied to the parallel input A11. The power supply fault signal from the power supply A1 is a summary fault signal resulting from the loss of +8-, +15-, +18-, +24-, or -15-V dc power supply outputs. The power supply fault signal will produce a receive fault signal from control A10. A receive fault, when caused by a power supply fault, is cleared only by changing frequency.

   A logic 1 synthesizer fault signal (smo lol) is supplied by synthesizer voltage regulator A14 in the frequency synthesizer. The synthesizer fault signal from the synthesizer subassembly is a summary fault signal resulting from loss of lock on any of the synthesizer decades (1-, 10-, or 100-Hz end decade, 10-Hz decade, 100-Hz decade, 1-kHz decade, 10-kHz decade, 100-kHz decade, and 1/10-MHz output module). The synthesizer fault signal will produce a receive fault signal from control A10. A receive fault signal, when caused by a synthesizer fault signal, is cleared when the cause of the fault is removed.

   A logic 1 vbfo synthesizer fault signal is supplied by vbfo A4. In the remote controlled receiver, the vbfo synthesizer fault signal is also supplied to the parallel input A11. The vbfo synthesizer fault signal from the vbfo A4 is a vbfo synthesizer loss-of-lock signal. The vbfo synthesizer fault signal will produce a receive fault signal from control A10. A receive fault signal, when caused by a vbfo synthesizer fault signal, is cleared when the cause of the fault is removed.

A logic 1 vbfo synthesizer fault signal is supplied by vbfo A4. In the remote controlled receiver, the vbfo synthesizer fault signal is also supplied to the parallel input A11. The vbfo synthesizer fault signal from the vbfo A4 is a vbfo synthesizer loss-of-lock signal. The vbfo synthesizer fault signal will produce a receive fault signal from control A10. A receive fault signal, when caused by a vbfo synthesizer fault signal, is cleared when the cause of the fault is removed.

b. RCV OVERLOAD (DS6) is lit by a receive overload signal at A2J3-14. The logic 1 receive overload signal is supplied by control A10. In the remote controlled receiver, the receive overload signal is also supplied to parallel input A11. The receive overload signal from control A10 is a summary of preselector rf overload signal from an associated preselector and a receive rf overload from rf translator A9.
c. AFC LOCK (DS7) is lit by an AFC lock signal A2J3-15. The logic 1 AFC lock signal is supplied by AFC A3. In the remote controlled receiver, the AFC lock is also supplied to the parallel input A11. The AFC lock signal indicates that the AFC is locked on the received carrier frequency.
d. PRESEL FAULT (DS23) is lit by a preselector fault signal at A2J3-7. The logic 1 preselector fault signal is supplied by control A10. In the remote controlled receiver, the preselector fault signal is also supplied to the parallel input A11. The preselector fault signal from control A10 is supplied as a logic 1 by the associated preselector and through a driver in control A10.

2.5.2 Mode Indicators

All mode indicators are lit by a logic 1 signal to LED status display A2A1. Refer to LED status display section of this instruction book for detailed information.

a. AM mode (DS9) is lit by an AM enable signal at A2J3-4. The logic 1 is supplied by MODE control switch on switch mounting board A2A2. In the remote controlled receiver, the AM enable signal may also be supplied by the parallel output A12 and is supplied to the parallel input A11.
b. SSB/CW mode (DS10) is lit by an SSB enable signal at A2J3-5. The logic 1 is supplied by MODE control switch on switch mounting board A2A2. In the remote controlled receiver, the SSB enable signal may also be supplied by the parallel output A12 and is supplied to the parallel input A11.
c. ISB mode (DS12) is lit by an ISB enable signal at A2J3-1. The logic 1 is supplied by MODE control switch on switch mounting board A2A2. In the remote controlled receiver, the ISB enable signal may also be supplied by the parallel output A12 and is supplied to the parallel input A11.

2.5.3 BANDWIDTH Indicators

All BANDWIDTH indicators are lit by a logic 1 signal to LED status display A2A1. Refer to LED status display section of this instruction book for detailed information. BANDWIDTH indicators will light only in AM, SSB/CW, or FM modes as the enabling logic 1 pullup is removed in all other settings of the MODE switch.

a. 16 (DS14) is lit by an FL8 (16-kHz) enable signal at A2J3-24. The logic 1 is supplied by BANDWIDTH control switch on switch mounting board A2A2. In the remote controlled receiver, the FL8 (16-kHz) enable signal may also be supplied by the parallel output A12 and is supplied to the parallel input A11.
b. A (DS15) is lit by an FL3 (A) enable signal at A2J3-22. The logic 1 is supplied by BANDWIDTH control switch on switch mounting board A2A2. In the remote controlled receiver, the FL3 (A) enable signal may also be supplied by the parallel output A12 and is supplied to the parallel input A11.
c. B (DS16) is lit by an FL4 (B) enable signal at A2J3-21. The logic 1 is supplied by BANDWIDTH control switch on switch mounting board A2A2. In the remote controlled receiver, the FL4 (B) enable signal may also be supplied by the parallel output A12 and is supplied to the parallel input A11.
d. U (DS17) is lit by an FL1 (USB) enable signal at A2J3-18. The logic 1 is supplied by BANDWIDTH control switch on switch mounting board A2A2. In the remote controlled receiver, the FL1 (USB) enable signal may also be supplied by the parallel output A12 and is supplied to the parallel input A11.
e. L (DS18) is lit by an FL2 (LSB) enable signal at A2J3-17. The logic 1 is supplied by BANDWIDTH control switch on switch mounting board A2A2. In the remote controlled receiver, the FL2 (LSB) enable signal may also be supplied by the parallel output A12 and is supplied to the parallel input A11.
f. C (DS19) is lit by an FL5 (C) enable signal at A2J3-19. The logic 1 is supplied by BANDWIDTH control switch on switch mounting board A2A2. In the remote controlled receiver, the FL5 (C) enable signal may also be supplied by the parallel output A12 and is supplied to the parallel input A11.
g. D (DS20) is lit by an FL6 (D) enable signal at A2J3-20. The logic 1 is supplied by BANDWIDTH control switch on switch mounting board A2A2. In the remote controlled receiver, the FL6 (D) enable signal may also be supplied by the parallel output A12 and is supplied to the parallel input A11.
h. E (DS21) is lit by an FL7 (E) enable signal at A2J3-23. The logic 1 is supplied by BANDWIDTH control switch on switch mounting board A2A2. In the remote controlled receiver, the FL7 (E) enable signal may also be supplied by the parallel output A12 and is supplied to the parallel input A11.

2.5.4 FREQUENCY KHZ and VBFO OFFSET HZ Displays (Refer to figure 7.)

All FREQUENCY KHZ and VBFO OFFSET HZ displays are lit by the BCD code supplied as the frequency control signals to the frequency synthesizer and/or the vbfo card. These BCD codes are supplied from the control A10 and vbfo A4, to the associated control circuits and the frequency display A2A5. In the remote controlled receiver, the frequency control signals may also be supplied by the parallel output A12 and are supplied to the parallel input A11.

2.5.5 Metering

The front panel meter is controlled by the METER switch. METER switch A2S1 in the 851S-1 Receiver has five positions: CH B AF (+13 FS), CH B AF (+3 FS), CH A AF (+3 FS), CH A AF (+13 FS), and RCV SIG.

a. In the CH B AF (+13 FS) and CH B AF (+3 FS) positions, a dc signal proportional to the B receive audio is supplied from receive audio A6 through J4-52, J12-42, P3-42, and METER switch A2A2S1 to meter M1. In both positions, A2A2R1 is in parallel with meter to ground to provide a calibrated full-scale reading of +3-dB mW full-scale deflection. In the CH B AF (+13 FS) position,

A2A2R2 is added in parallel with meter to ground to cause an effective reading of +13-dB mW full-scale deflection.

b. In the CH A AF (+3 FS) and CH A AF (+13 FS) positions, a dc signal proportional to the A receive audio is supplied from receive audio A6 through J4-3, J12-46, P3-46, and METER switch A2A2S1 to meter M1. In both positions, A2A2R1 is in parallel with meter to ground to provide a calibrated full-scale reading of +3-dB mW full-scale deflection. In the CH A AF (+13 FS) position, A2A2R2 is added in parallel with meter to ground to cause an effective reading of +13-dB mW full-scale deflection.

c. In the RCV SIG position, an rf AGC sample is supplied from channel A if A8 and channel B if A7. The AGC sample is supplied from channel A if A8 through J6-12 or from channel B if A7 through J5-12, through J12-41, P3-41, and METER switch A2A2S1 to meter M1. In the RCV SIG position, the meter is zeroed at 0 dB with up to 1-μV signal input and calibrated in dB above 1 μV with full-scale deflection of 100 dB above 1-μV rf signal input.

Table 3. Location of Signals in Control/Monitor Words.

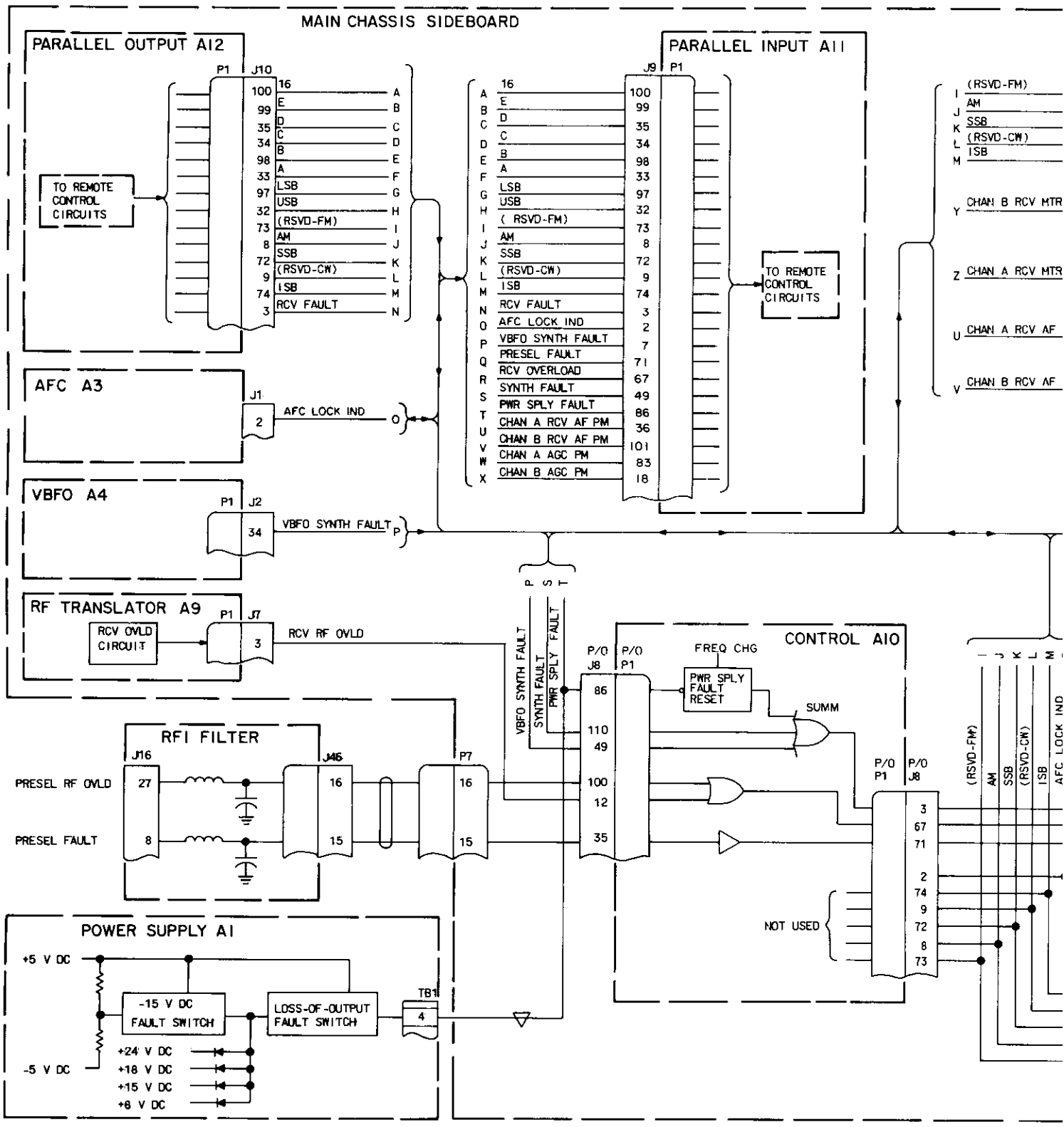
SIGNAL	8-BIT CHARACTER			7-BIT ASCII		
	WORD	CHARACTER	BIT	WORD	FUNCTIONAL CHARACTER	WT
Fault and Status Indicators						
AFC lock	4	3	8	4	6	8
Receive fault	4	4	1	4	9	1
Power supply fault	4	4	2	4	9	2
Synth fault (smo lol)	4	4	3	4	9	4
Vbfo synth fault	4	5	6	4	10	2
Receive overload	4	4	4	4	9	8
Preselector fault	4	5	4	4	11	8
Mode Indicators						
AM	2	5	7	2	10	4
SSB	2	5	6	2	10	2
CW	2	5	5	2	10	1
ISB	2	5	4	2	11	8
BANDWIDTH Indicators						
16	2	4	8	2	8	8
A	2	4	3	2	9	4
B	2	4	4	2	9	8
C	2	4	5	2	8	1
D	2	4	6	2	8	2
E	2	4	7	2	8	4
LSB	2	4	2	2	9	2
USB	2	4	1	2	9	1

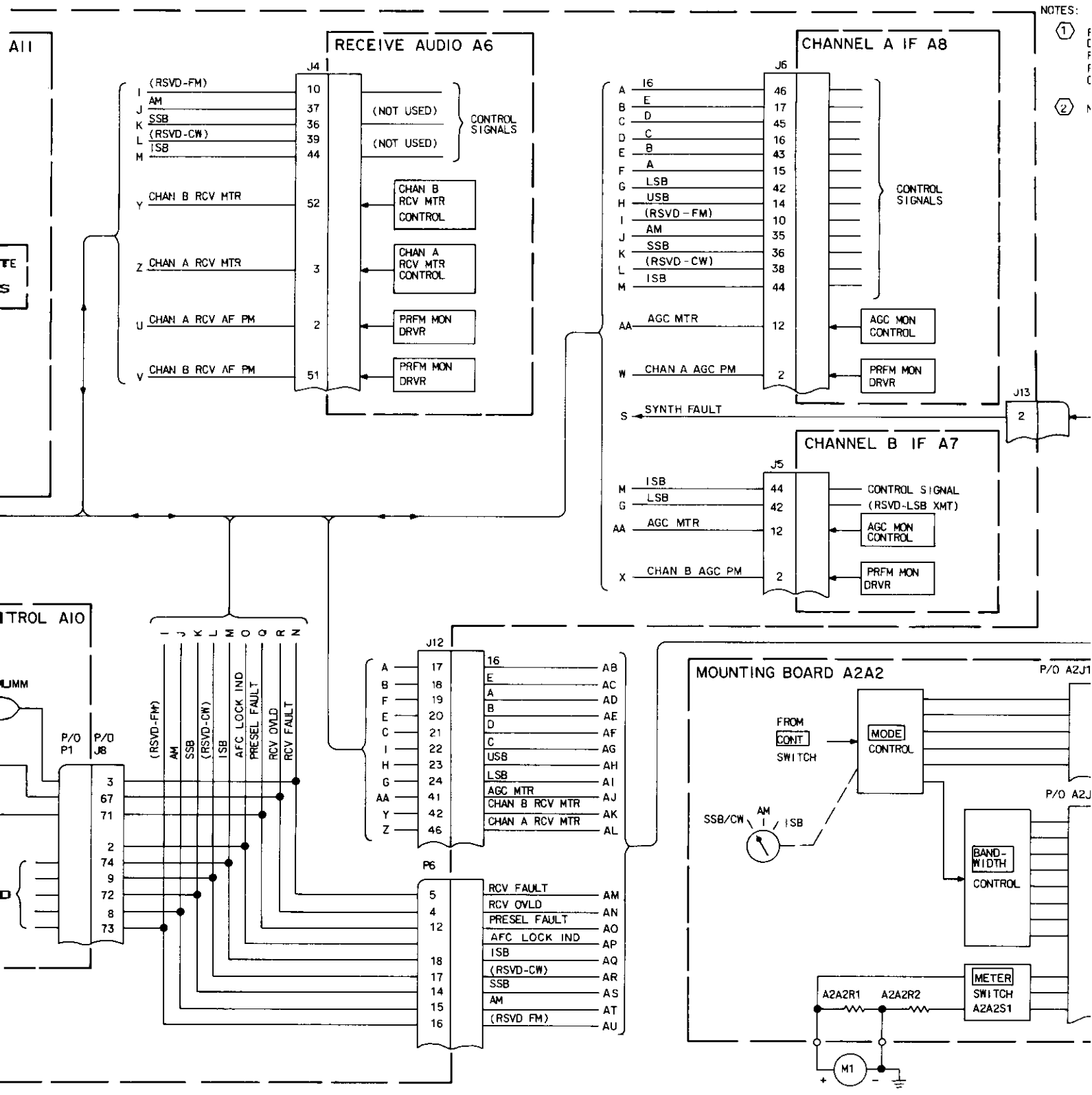
Table 3. Location of Signals in Control/Monitor Words (Cont).

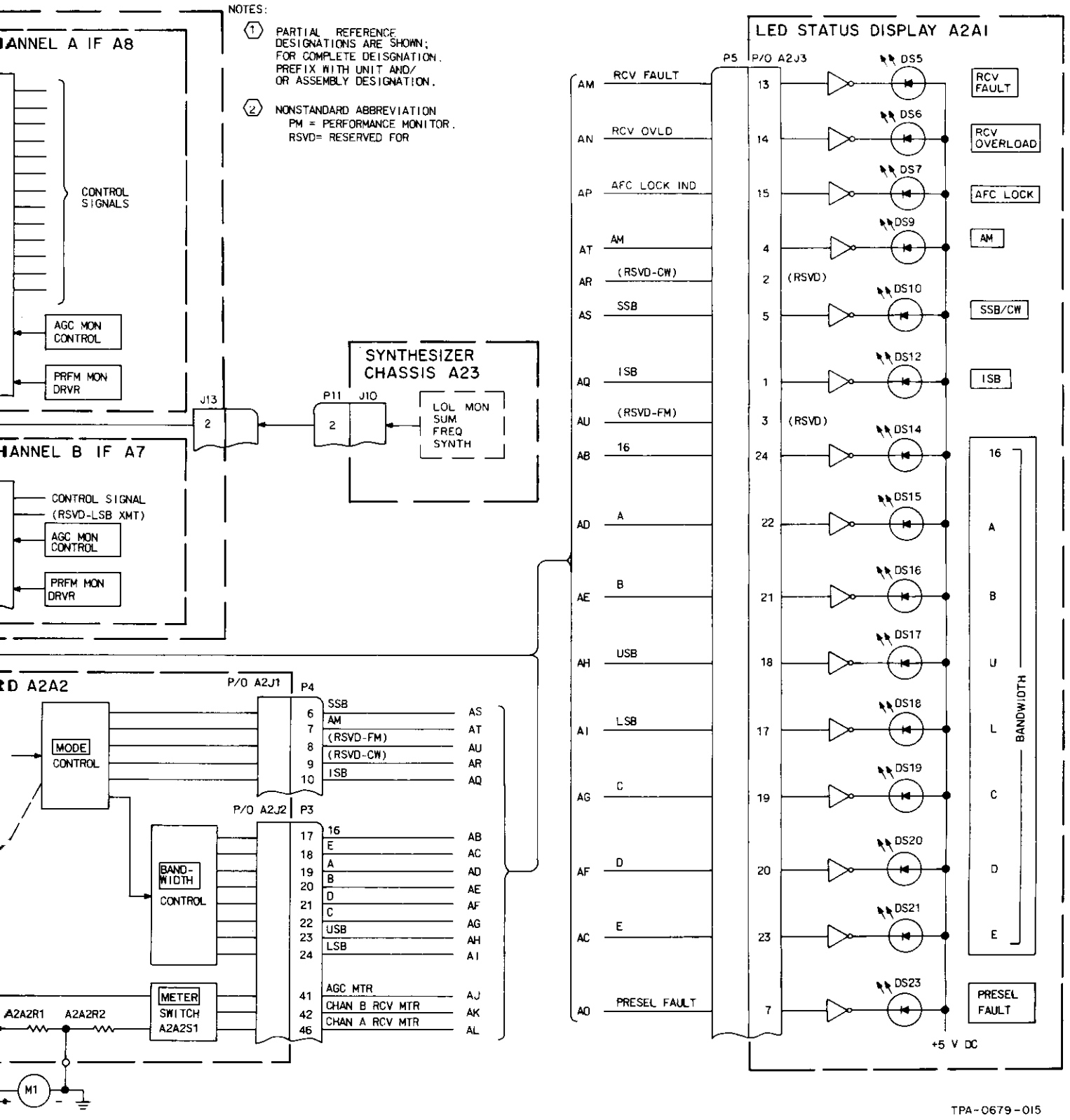
SIGNAL	8-BIT CHARACTER			7-BIT ASCII		
	WORD	CHARACTER	BIT	WORD	FUNCTIONAL CHARACTER	WT
FREQUENCY KHZ BCD Signals						
1 Hz (1)	1	5	1	1	11	1
1 Hz (2)	1	5	2	1	11	2
1 Hz (4)	1	5	3	1	11	4
1 Hz (8)	1	5	4	1	11	8
10 Hz (1)	1	5	5	1	10	1
10 Hz (2)	1	5	6	1	10	2
10 Hz (4)	1	5	7	1	10	4
10 Hz (8)	1	5	8	1	10	8
100 Hz (1)	1	4	1	1	9	1
100 Hz (2)	1	4	2	1	9	2
100 Hz (4)	1	4	3	1	9	4
100 Hz (8)	1	4	4	1	9	8
1 kHz (1)	1	4	5	1	8	1
1 kHz (2)	1	4	6	1	8	2
1 kHz (4)	1	4	7	1	8	4
1 kHz (8)	1	4	8	1	8	8
10 kHz (1)	1	3	1	1	7	1
10 kHz (2)	1	3	2	1	7	2
10 kHz (4)	1	3	3	1	7	4
10 kHz (8)	1	3	4	1	7	8
100 kHz (1)	1	3	5	1	6	1
100 kHz (2)	1	3	6	1	6	2
100 kHz (4)	1	3	7	1	6	4
100 kHz (8)	1	3	8	1	6	8
1 MHz (1)	1	2	1	1	5	1
1 MHz (2)	1	2	2	1	5	2
1 MHz (4)	1	2	3	1	5	4
1 MHz (8)	1	2	4	1	5	8
10 MHz (1)	1	2	5	1	4	1

Table 3. Location of Signals in Control/Monitor Words (Cont).

SIGNAL	8-BIT CHARACTER			7-BIT ASCII		
	WORD	CHARACTER	BIT	WORD	FUNCTIONAL CHARACTER	WT
VBFO OFFSET KHZ BCD Signals						
10 MHz (2)	1	2	6	1	4	2
10 Hz (1)	3	3	1	3	7	1
10 Hz (2)	3	3	2	3	7	2
10 Hz (4)	3	3	3	3	7	4
10 Hz (8)	3	3	4	3	7	8
100 Hz (1)	3	3	5	3	6	1
100 Hz (2)	3	3	6	3	6	2
100 Hz (4)	3	3	7	3	6	4
100 Hz (8)	3	3	8	3	6	8
1 kHz (1)	3	2	1	3	5	1
1 kHz (2)	3	2	2	3	5	2
1 kHz (4)	3	2	3	3	5	4
1 kHz (8)	3	2	4	3	5	8
SIGN	3	2	5	3	4	1


MAIN CHASSIS SIDEBOARD
PARALLEL OUTPUT A12
P1
J10
TO REMOTE CONTROL CIRCUITS
100 16 A
99 E B
35 D C
34 C D
98 B E
33 A F
97 LSB G
32 USB H
73 (RSVD-FM) I
8 AM J
72 SSB K
9 (RSVD-CW) L
74 ISB M
3 RCV FAULT N
PARALLEL INPUT A11
J9
P1
TO REMOTE CONTROL CIRCUITS
A 16 100
B E 99
C D 35
D C 34
E B 98
F A 33
G LSB 97
H USB 32
I (RSVD-FM) 73
J AM 8
K SSB 72
L (RSVD-CW) 9
M ISB 74
N RCV FAULT 3
O AFC LOCK IND 2
P VBFO SYNTH FAULT 7
Q PRESEL FAULT 71
R RCV OVERLOAD 67
S SYNTH FAULT 49
T PWR SPLY FAULT 86
U CHAN A RCV AF PM 36
V CHAN B RCV AF PM 101
W CHAN A AGC PM 83
X CHAN B AGC PM 18
I (RSVD-FM)
J AM
K SSB
L (RSVD-CW)
M ISB
Y CHAN B RCV MTR
Z CHAN A RCV MTR
U CHAN A RCV AF
V CHAN B RCV AF
AFC A3
J1
2
AFC LOCK IND
O
VBFO A4
P1
J2
34
VBFO SYNTH FAULT
P
RF TRANSLATOR A9
RCV OVLD CIRCUIT
P1
J7
3
RCV RF OVLD
P
S
T
VBFO SYNTH FAULT
SYNTH FAULT
PWR SPLY FAULT
CONTROL A10
P/O J8
P/O P1
FREQ CHG
PWR SPLY FAULT RESET
SUMM
86
110
49
100
12
35
P/O P1
P/O J8
3
67
71
2
74
9
72
8
73
NOT USED
(RSVD-FM)
AM
SSB
(RSVD-CW)
ISB
AFC LOCK IND
RFI FILTER
J16
J45
P7
PRESEL RF OVLD
PRESEL FAULT
27
8
16
15
16
15
POWER SUPPLY A1
+5 V DC
-5 V DC
-15 V DC FAULT SWITCH
LOSS-OF-OUTPUT FAULT SWITCH
TB1
4
+24 V DC
+18 V DC
+15 V DC
+8 V DC


NOTES:
A11
RECEIVE AUDIO A6
J4
I (RSVD-FM) 10
J AM 37
K SSB 36
L (RSVD-CW) 39
M ISB 44
(NOT USED)
(NOT USED)
CONTROL SIGNALS
Y CHAN B RCV MTR 52
CHAN B RCV MTR CONTROL
Z CHAN A RCV MTR 3
CHAN A RCV MTR CONTROL
U CHAN A RCV AF PM 2
PRFM MON DRVR
V CHAN B RCV AF PM 51
PRFM MON DRVR
CHANNEL A IF A8
J6
A I6 46
B E 17
C D 45
D C 16
E B 43
F A 15
G LSB 42
H USB 14
I (RSVD-FM) 10
J AM 35
K SSB 36
L (RSVD-CW) 38
M ISB 44
CONTROL SIGNALS
AA AGC MTR 12
AGC MON CONTROL
W CHAN A AGC PM 2
PRFM MON DRVR
J13
S SYNTH FAULT 2
CHANNEL B IF A7
J5
M ISB 44
G LSB 42
CONTROL SIGNAL (RSVD-LSB XMT)
AA AGC MTR 12
AGC MON CONTROL
X CHAN B AGC PM 2
PRFM MON DRVR
ITROL A10
P/O P1
P/O J8
(RSVD-FM)
AM
SSB
(RSVD-CW)
ISB
AFC LOCK IND
PRESEL FAULT
RCV OVLD
RCV FAULT
3
67
71
2
74
9
72
8
73
J12
A 17
B 18
F 19
E 20
C 21
I 22
H 23
G 24
AA 41
Y 42
Z 46
16 AB
E AC
A AD
B AE
D AF
C AG
USB AH
LSB AI
AGC MTR AJ
CHAN B RCV MTR AK
CHAN A RCV MTR AL
P6
5 RCV FAULT AM
4 RCV OVLD AN
12 PRESEL FAULT AO
AFC LOCK IND AP
18 ISB AQ
17 (RSVD-CW) AR
14 SSB AS
15 AM AT
16 (RSVD FM) AU
MOUNTING BOARD A2A2
P/O A2J1
FROM CONT SWITCH
MODE CONTROL
SSB/CW
AM
ISB
BAND-WIDTH CONTROL
P/O A2J
METER SWITCH A2A2S1
A2A2R1
A2A2R2
M1



Monitor Functions, Block Diagram
Figure 11

2.6 Power Distribution (Refer to figure 12.)

Primary power distribution in the 851S-( ) equipments is controlled by power supply A1. Input power to the power supply is connected to A1J1 on the 851S-1 rear panel, supplied through A1F1 (rear panel), A2S15 (front panel), and A1S1 (rear panel) to the input power transformer (P/O A1). Power supply A1 uses rectifiers and regulators to produce the following base output voltages: +5, +8, +15, +18, +24, and -15 V dc.

These voltages are supplied to cards and modules in the 851S-1 and are the only voltages used, except for the following special applications.

In receive audio A6, the -15 V dc input is used with a 5.1-V dc regulator to produce -5.1 V dc for a squelch reference voltage.

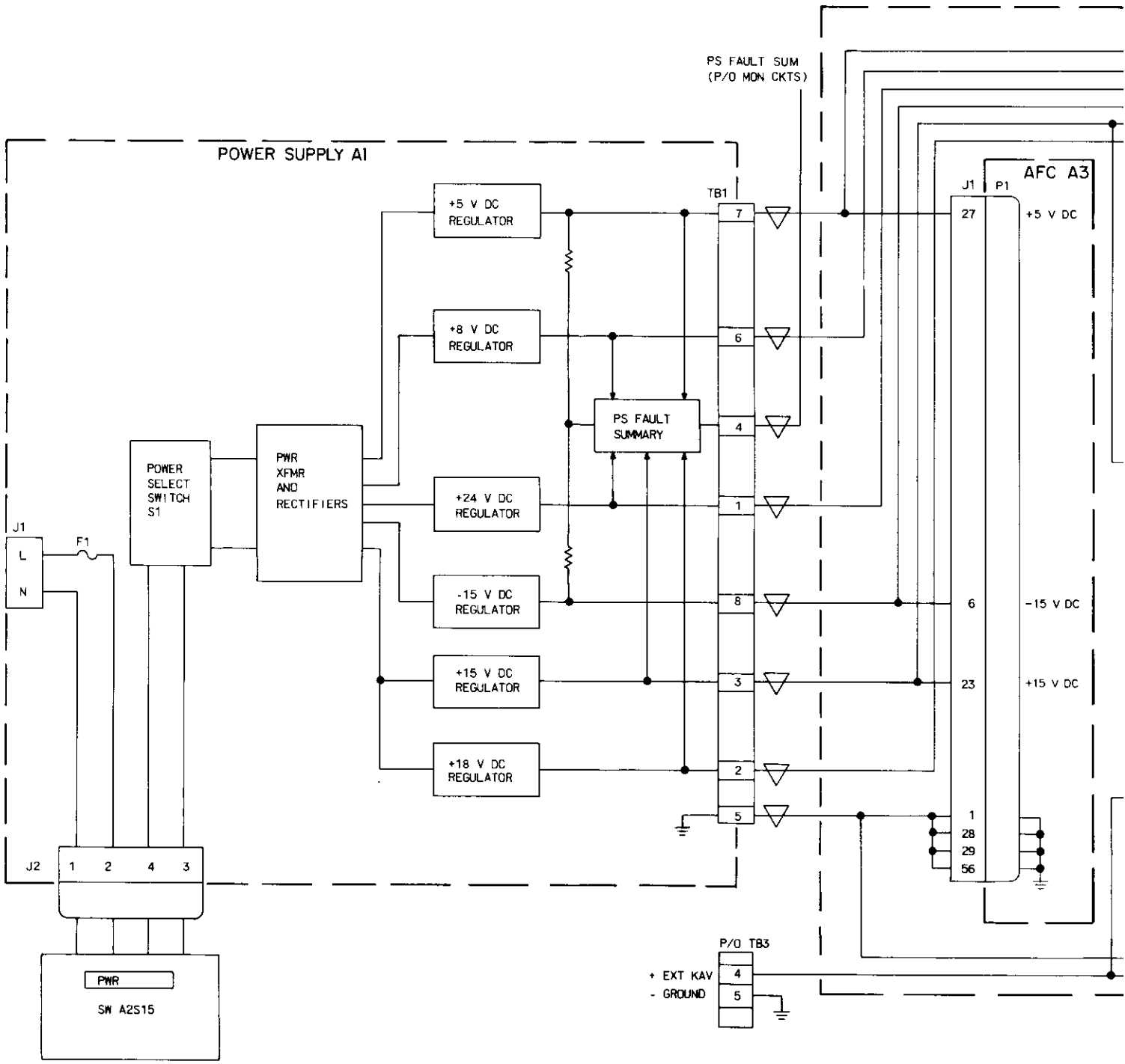
In channel A if A8 and channel B if A7, the following voltages are produced:

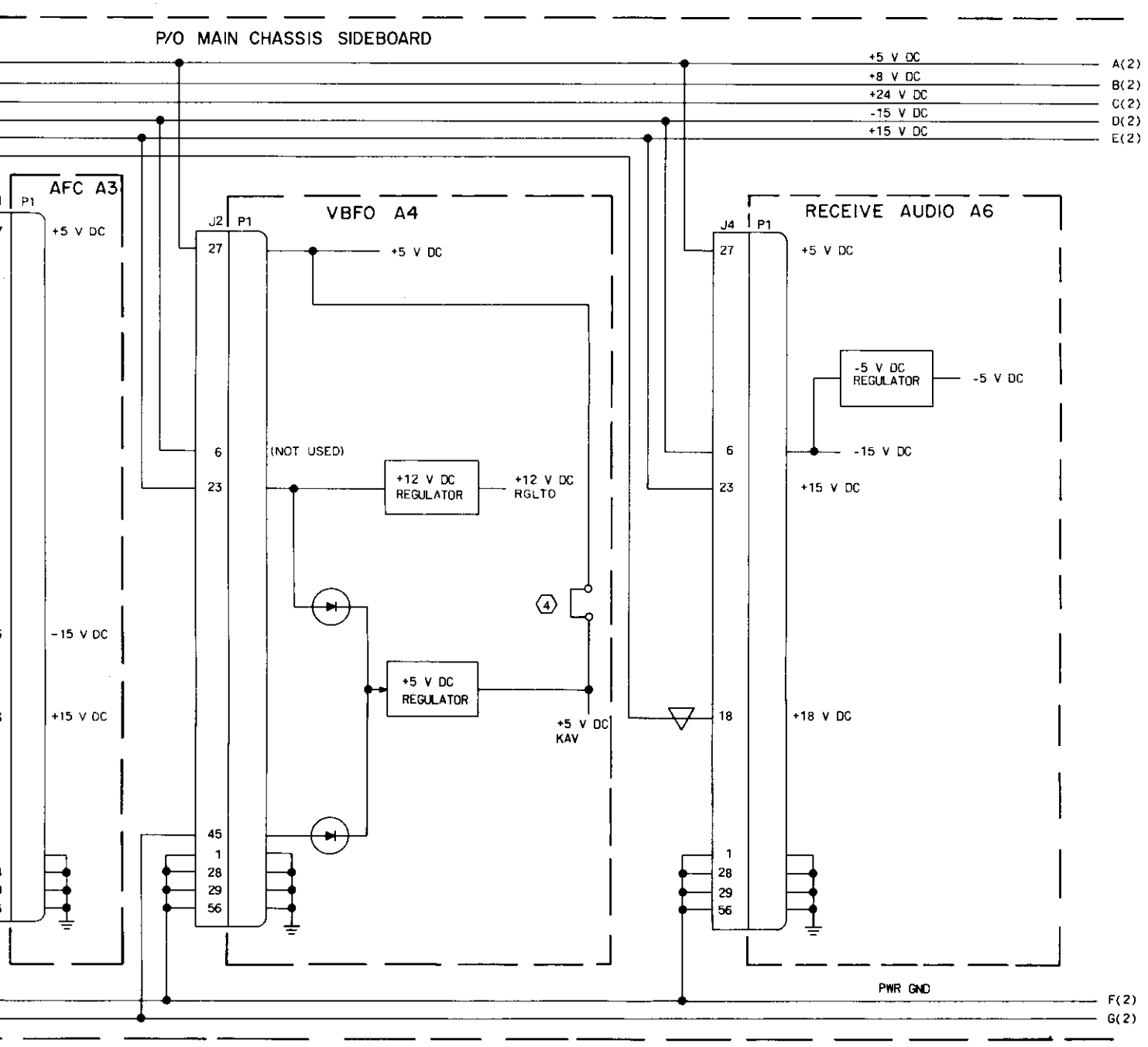
a. The -15-V dc input is used with a 10-V dc regulator to produce -10 V dc B- for the filter switches.
b. The -15-V dc input is used with a 6.8-V dc regulator to produce -6.8 V dc B- for the transmit 9.45-MHz output amplifier.
c. The +15-V dc input is used with a 6.8-V dc regulator to produce +6.8 V dc B+ for the transmit 9.45-MHz output amplifier.
d. The +15-V dc input is used with a voltage divider to produce +2-V dc reference voltage for filter switches.

In parallel output A12, the +15-V dc input is used with a 5.6-V dc regulator to produce +5.6 V dc B+ for output storage registers.

In synthesizer voltage regulator A14, the +24-, and +8-V dc inputs are used with series regulators to produce regulated +20- and regulated +5.2-V dc outputs for synthesizer control and B+ voltages.

An optional external keep-alive voltage (+5 to +15 V dc) may be supplied to the vbfo A4 and control A10 to save frequency and offset information during a power interrupt.


PS FAULT SUM
(P/O MON CKTS)
POWER SUPPLY AI
AFC A3
J1
P1
TB1
+5 V DC
REGULATOR
+8 V DC
REGULATOR
PS FAULT
SUMMARY
+24 V DC
REGULATOR
-15 V DC
REGULATOR
+15 V DC
REGULATOR
+18 V DC
REGULATOR
POWER
SELECT
SWITCH
S1
PWR
XFMR
AND
RECTIFIERS
J1
L
N
F1
J2
1
2
4
3
PWR
SW A2S15
7
6
4
1
8
3
2
5
27
+5 V DC
6
-15 V DC
23
+15 V DC
1
28
29
56
P/O TB3
+ EXT KAV
- GROUND
4
5



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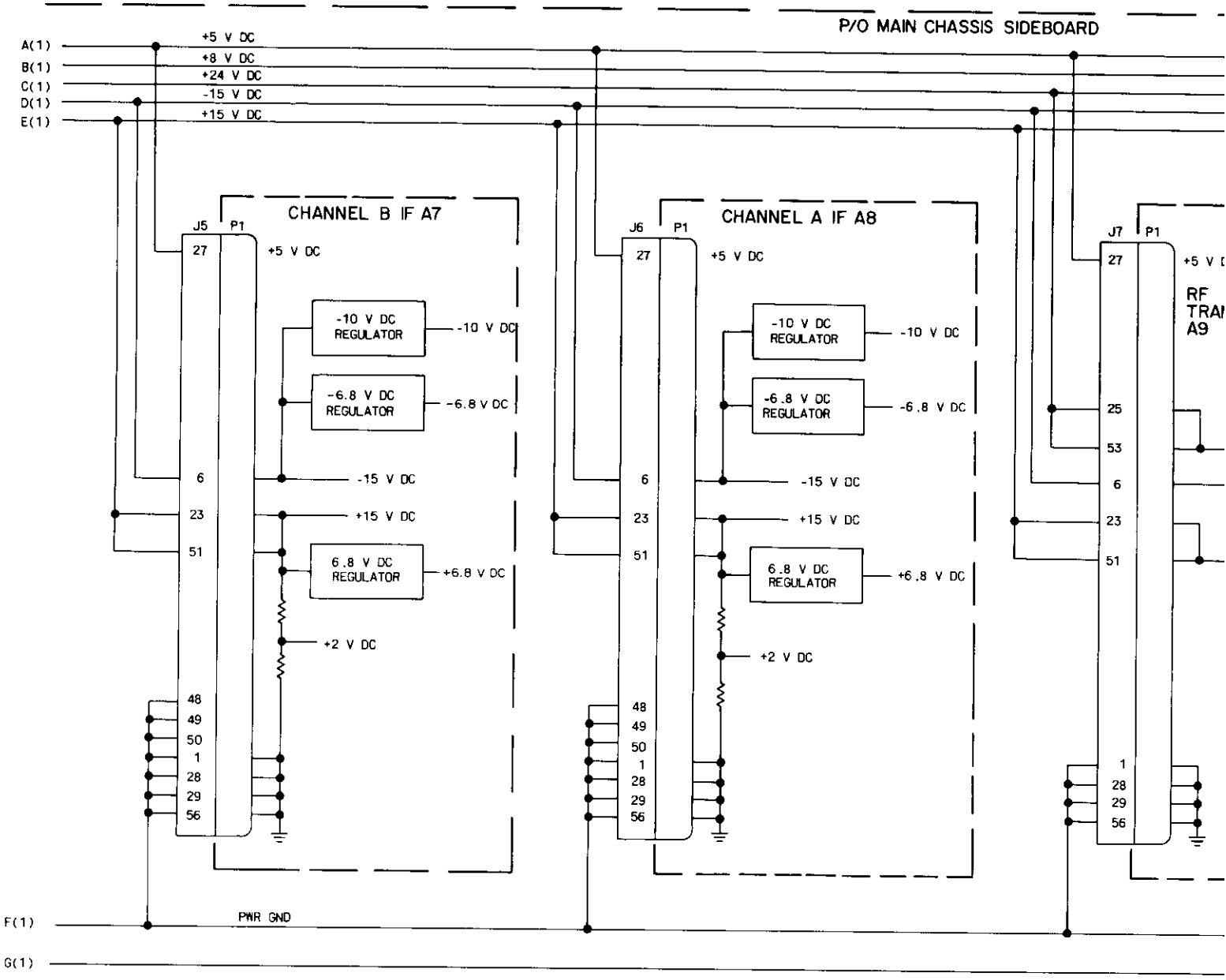
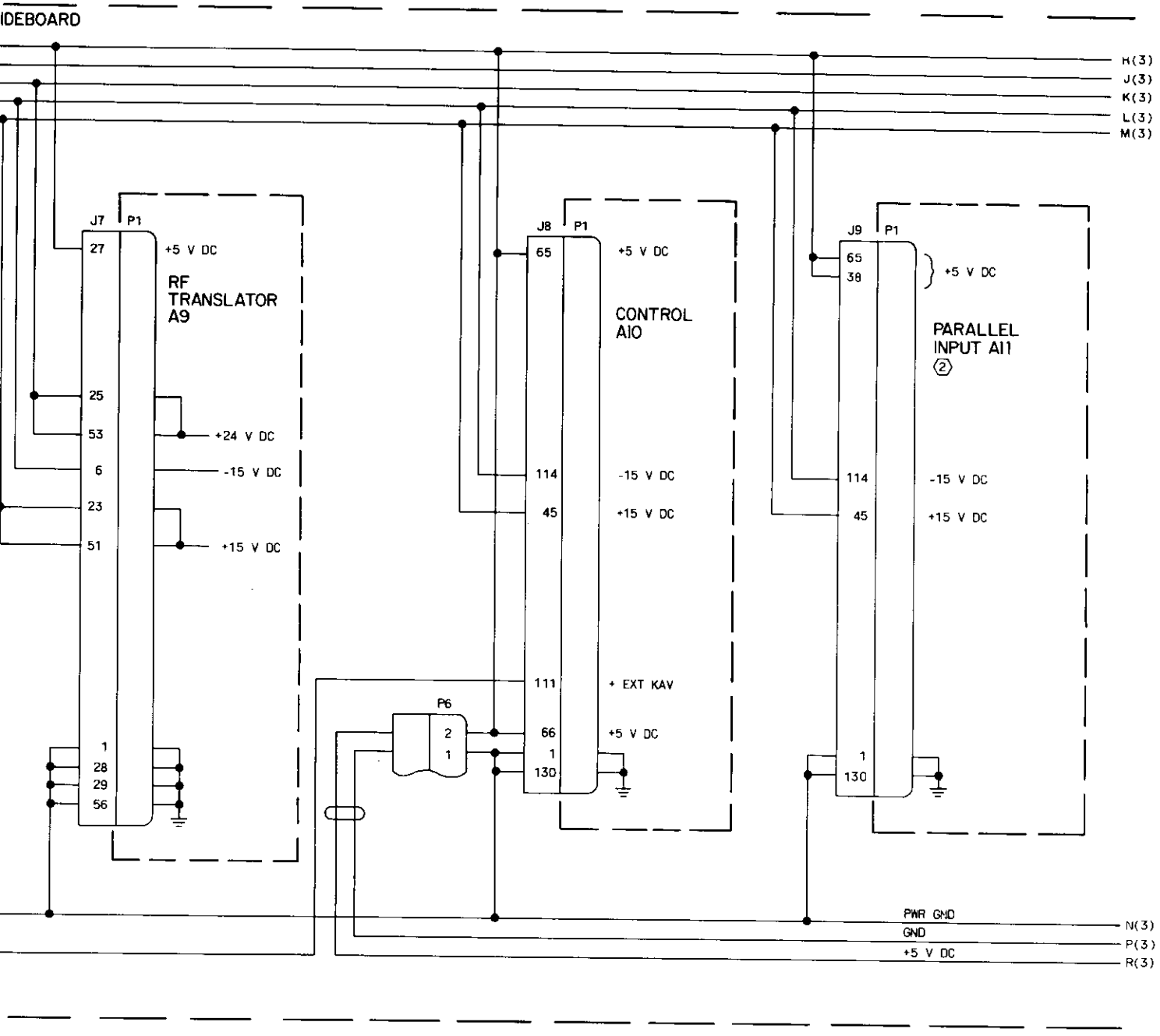
Power Distribution, Block Diagram
Figure 12 (Sheet 1 of 4)


P/O MAIN CHASSIS SIDEBOARD
A(1)
B(1)
C(1)
D(1)
E(1)
+5 V DC
+8 V DC
+24 V DC
-15 V DC
+15 V DC
CHANNEL B IF A7
J5
P1
27
+5 V DC
-10 V DC REGULATOR
-10 V DC
-6.8 V DC REGULATOR
-6.8 V DC
6
-15 V DC
23
+15 V DC
51
6.8 V DC REGULATOR
+6.8 V DC
+2 V DC
48
49
50
1
28
29
56
CHANNEL A IF A8
J6
P1
27
+5 V DC
-10 V DC REGULATOR
-10 V DC
-6.8 V DC REGULATOR
-6.8 V DC
6
-15 V DC
23
+15 V DC
51
6.8 V DC REGULATOR
+6.8 V DC
+2 V DC
48
49
50
1
28
29
56
J7
P1
27
+5 V
RF
TRA
A9
25
53
6
23
51
1
28
29
56
F(1)
PWR GND
G(1)



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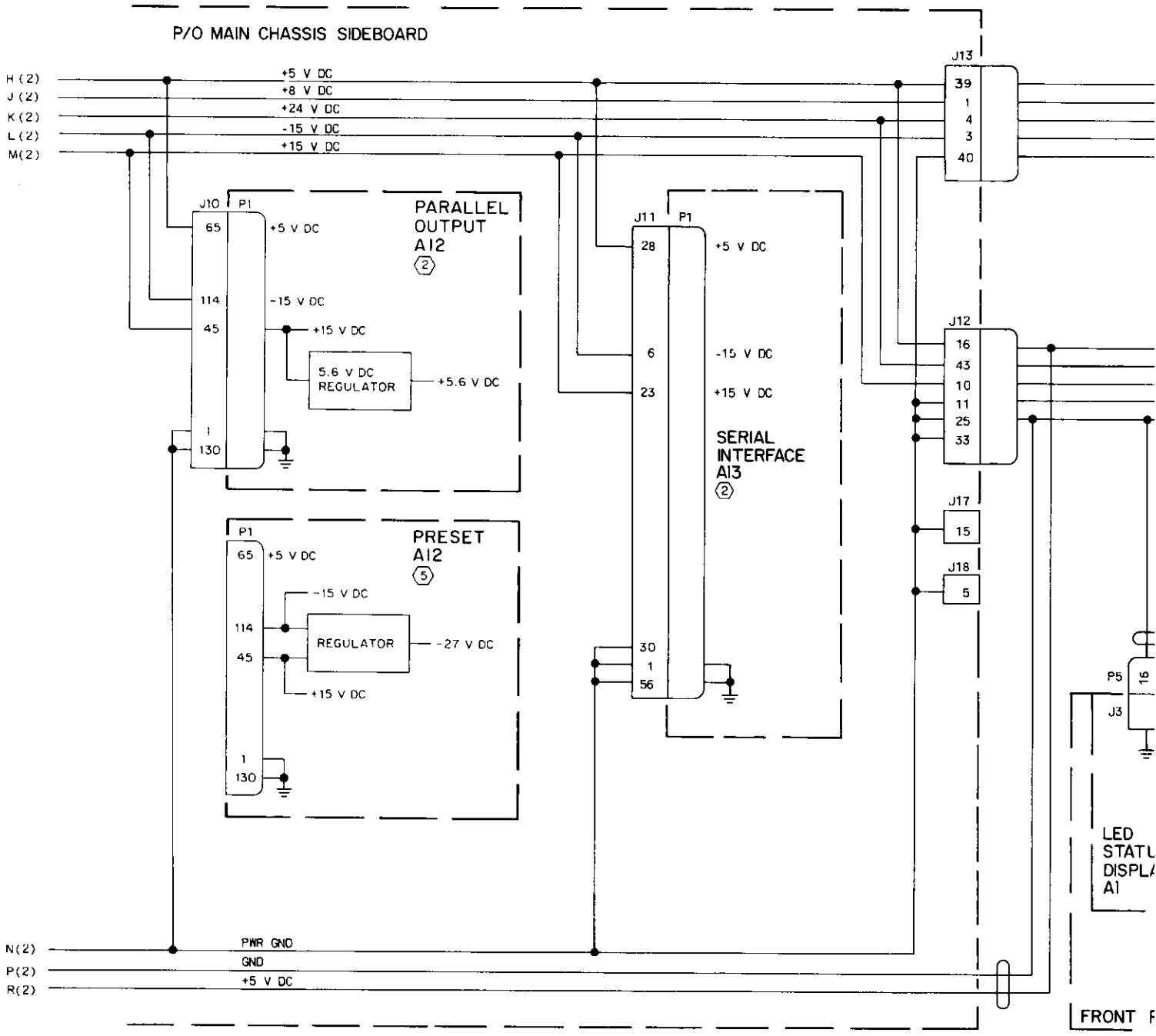
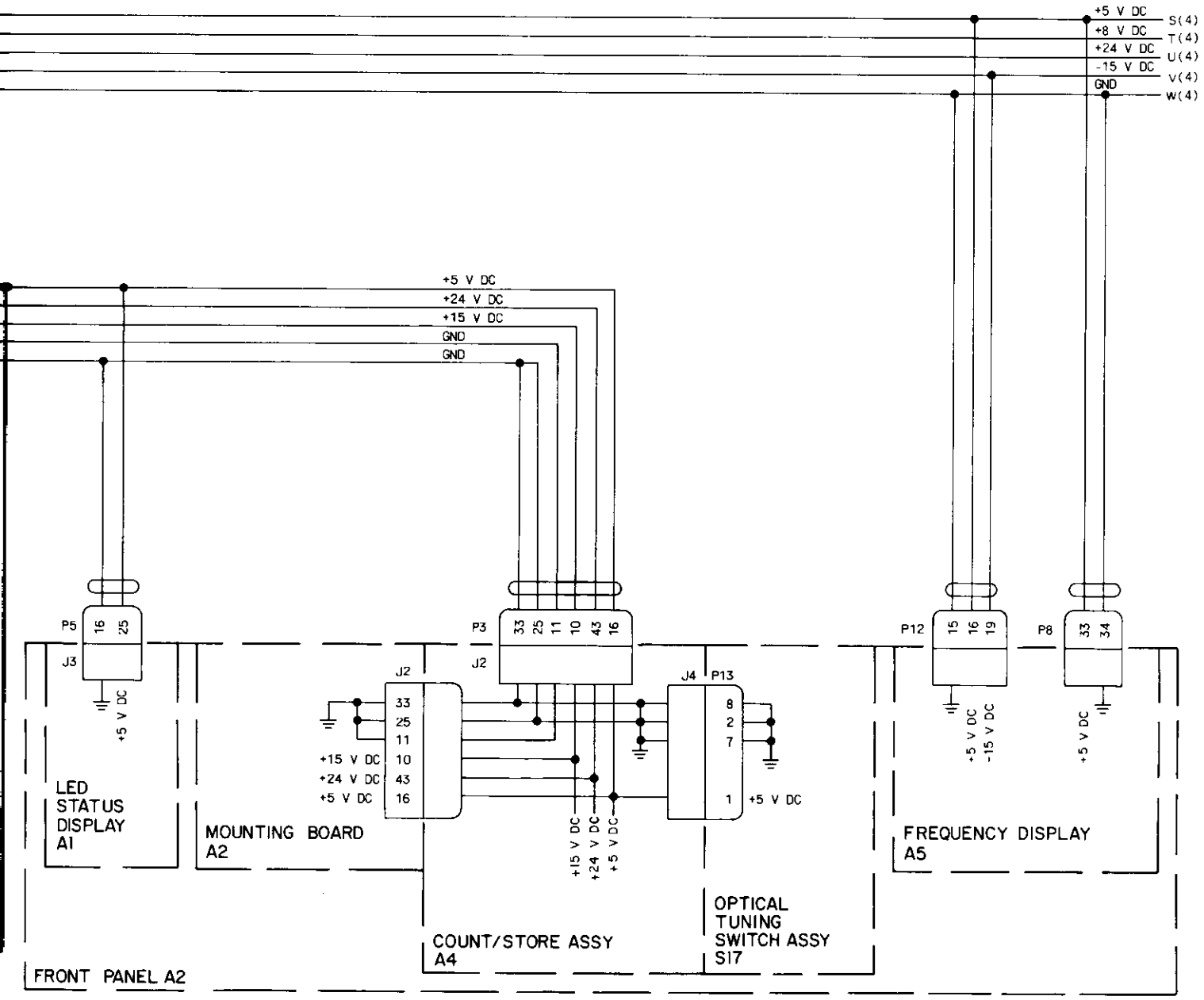
Power Distribution, Block Diagram
Figure 12 (Sheet 2)


P/O MAIN CHASSIS SIDEBOARD
H(2)
J(2)
K(2)
L(2)
M(2)
+5 V DC
+8 V DC
+24 V DC
-15 V DC
+15 V DC
J13
39
1
4
3
40
J10
P1
65
114
45
1
130
+5 V DC
-15 V DC
+15 V DC
5.6 V DC REGULATOR
+5.6 V DC
PARALLEL OUTPUT A12
2
J11
P1
28
6
23
30
1
56
+5 V DC
-15 V DC
+15 V DC
SERIAL INTERFACE A13
2
J12
16
43
10
11
25
33
J17
15
J18
5
P1
65
114
45
1
130
+5 V DC
-15 V DC
+15 V DC
REGULATOR
-27 V DC
PRESET A12
5
P5
16
J3
LED STATU DISPLA A1
FRONT
N(2)
P(2)
R(2)
PWR GND
GND
+5 V DC



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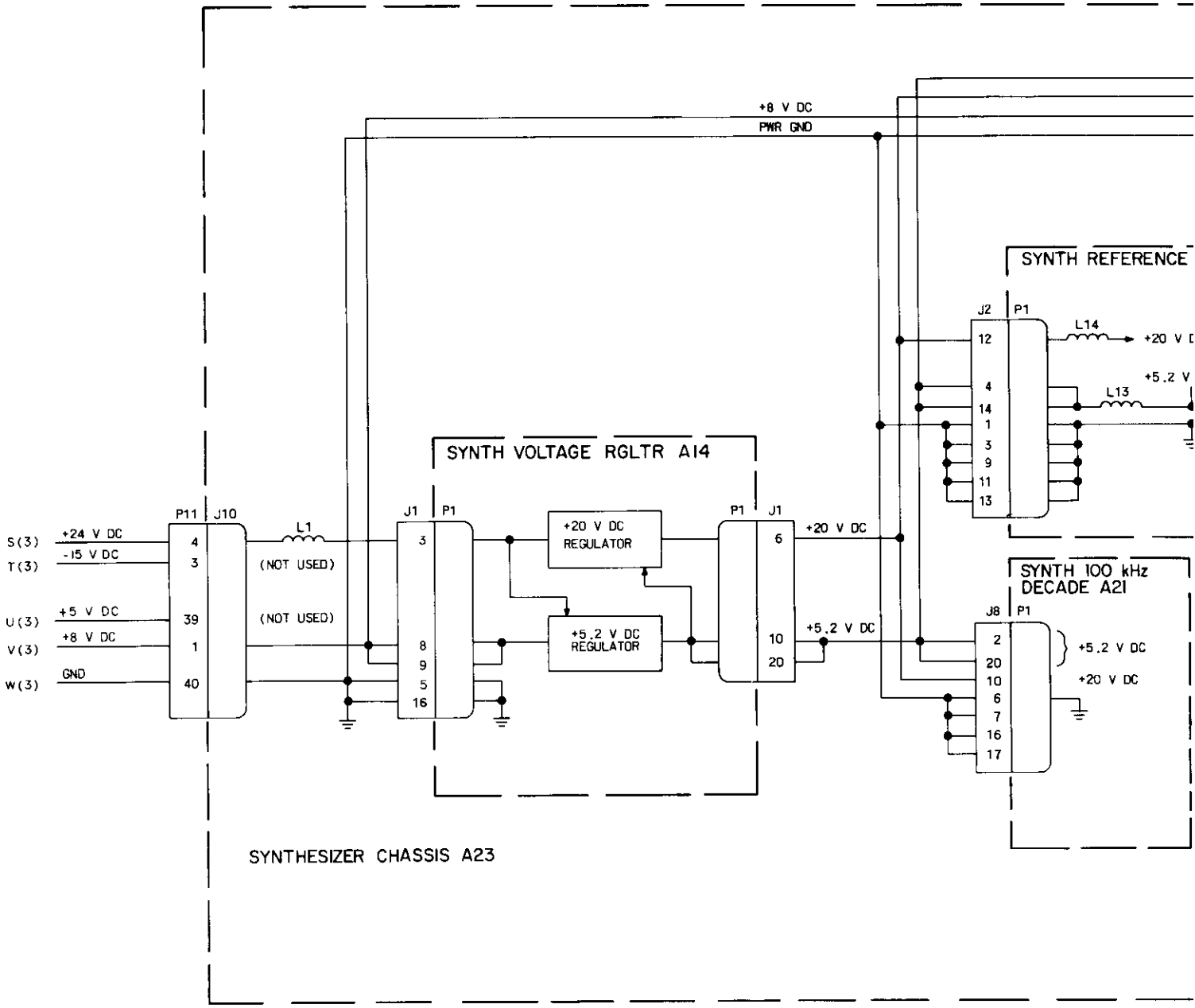
Power Distribution, Block Diagram
Figure 12 (Sheet 3)



NOTES:

NONSTANDARD SYMBOLS

(1) INDICATES HARD WIRED

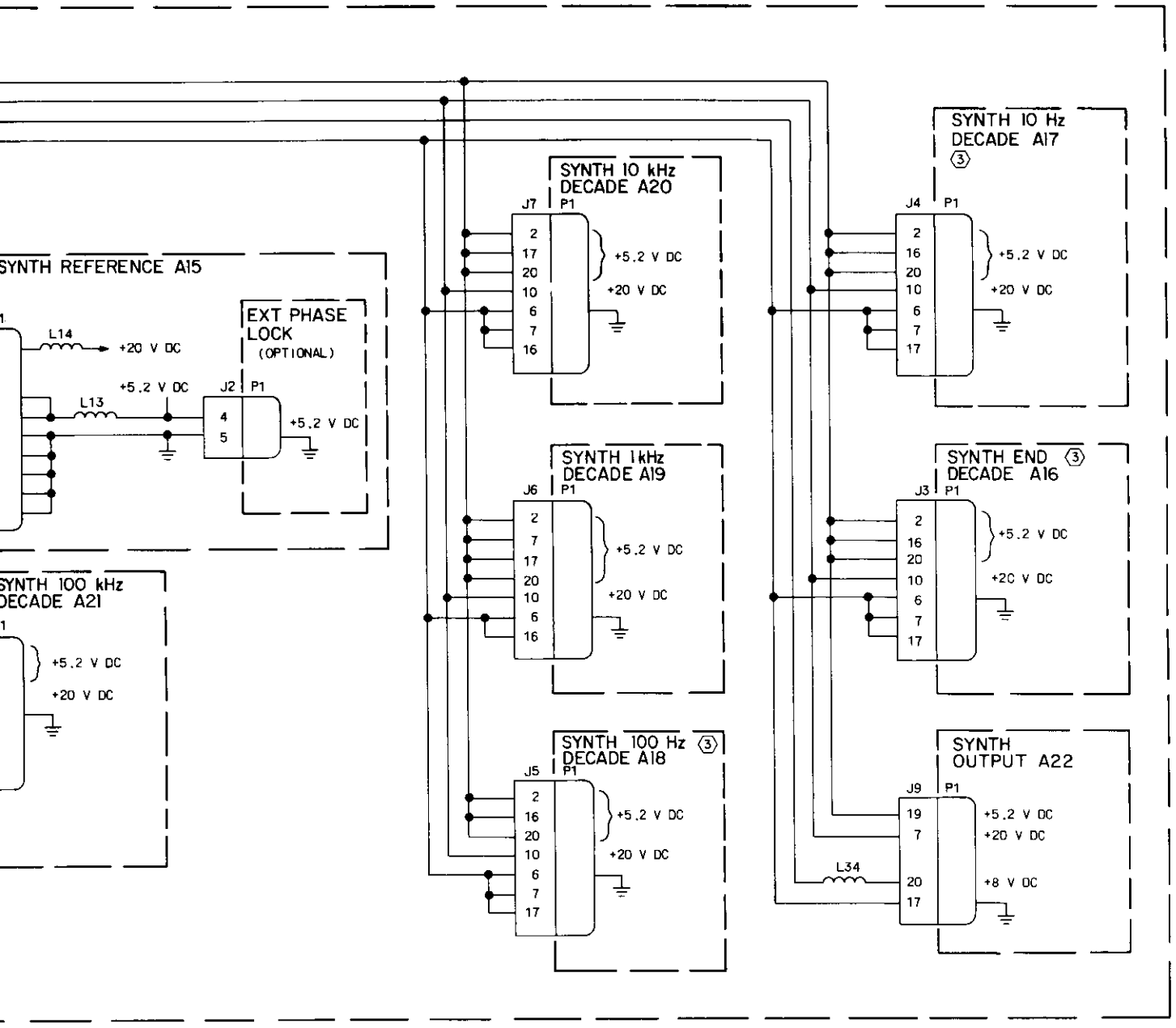
INDICATES RIBBON CABLE

(2) INCLUDED ONLY IN REMOTE UNITS.

(3) SYNTHESIZER END DECADE IS:
A18 FOR 100 Hz TUNING (A16 AND A17
A17 FOR 10 Hz TUNING (A16 NOT USED)
A16 FOR 1 Hz TUNING.

(4) JUMPERED IF + EXT KAV (+5 V DC)
IS NOT USED.

(5) INCLUDED ONLY IN UNITS WITH PRESE



END DECADE IS:
Hz TUNING (A16 AND A17 NOT USED).
z TUNING (A16 NOT USED).
z TUNING.

EXT KAV (+5 V DC)

LY IN UNITS WITH PRESET CONTROL.

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Power Distribution, Block Diagram
Figure 12 (Sheet 4)