Serial Interface (635-0742-001)

Rockwell International

instructions

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1. DESCRIPTION

Serial Interface 635-0742-001, shown in figure 1, is a 2-layer planar card with a 56-pin edge-on connector (2 layers, 28 pins each).

The serial interface card consists of two primary circuits, a serial data receive circuit and a serial data transmit circuit.

In the serial data receive circuit are a receiver, an FSK decoder, a data UAR/T (universal asynchronous receiver/transmitter), an error detector, a word subaddress latch, an output parallel-to-serial shift register, a strobe decoder, and a bit/baud rate and clock generator.

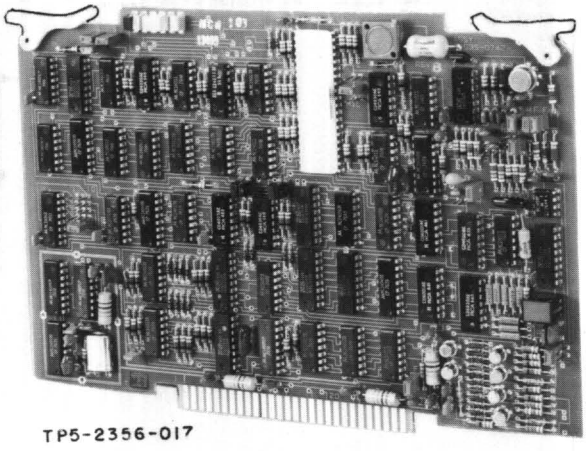
In the serial data transmit circuit are a data multiplexer, a data strobe generator, a bit/baud rate and clock generator, a data UAR/T, an FSK keyer, and an RS-232C driver.

2. PRINCIPLES OF OPERATION

2.1 General (Refer to figure 2.)

As a serial data receiver, the serial interface card receives FSK, RS-232C or MIL-STD-188C serial data control signals and checks for address, command status, and data errors. It then provides error, clock, word subaddress, strobe, and serial data outputs for decoding by a parallel output card.

As a serial data transmitter, the serial interface card receives parallel data inputs and a transmit word initiate and provides FSK, RS-232C, or MIL-STD-188C serial data monitor signals. The serial data monitor signals are supplied to the associated unit/control.

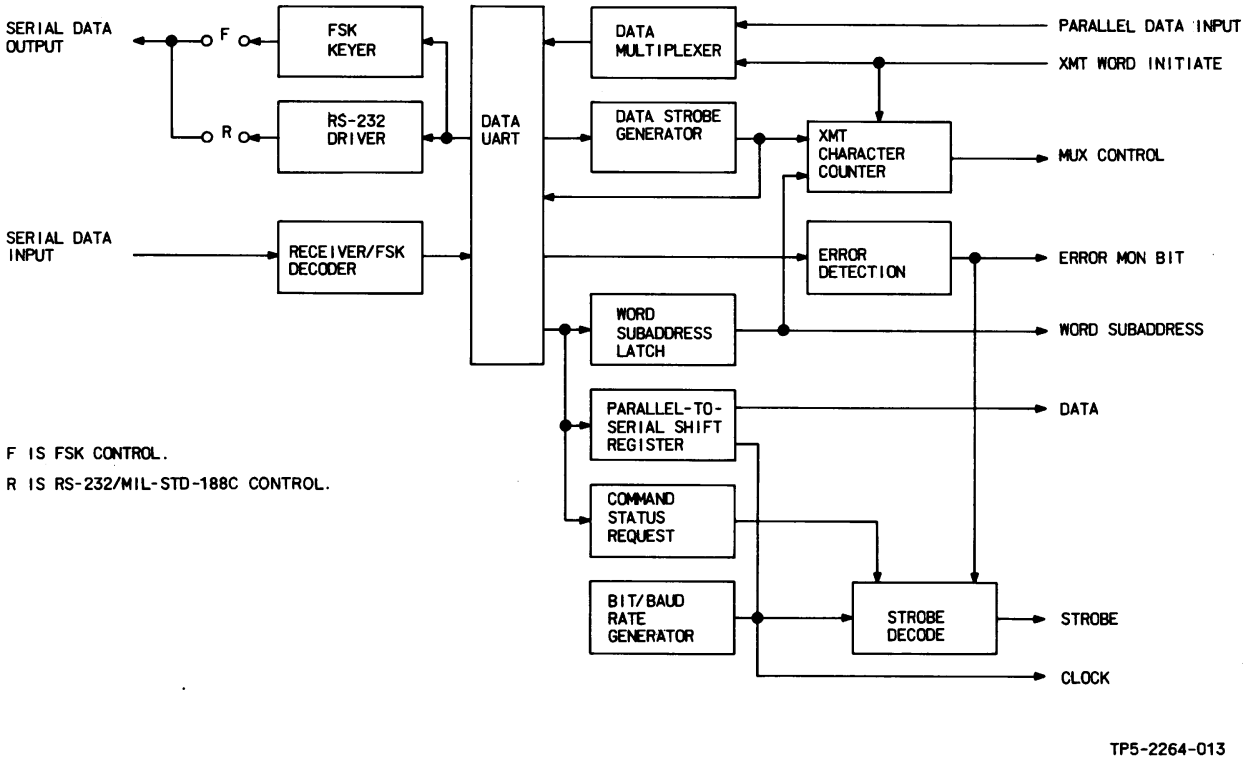


Serial Interface
Figure 1

2.2 Serial Data Inputs and Outputs

When strapped accordingly, the serial interface card receives and transmits any of the following types of control techniques.

a. FSK (mark = 1280 Hz, space = 2133 Hz) with mark equivalent to logic 1 data and space equivalent to logic 0 data. Data supplied at 75, 150, 300, or 600 bauds.
b. EIA RS-232C (mark = -6 ±1 V dc, space = +6 ±1 V dc) with mark equivalent to logic 1 data and space equivalent to logic 0 data. Using an EIA RS-232C processor, data supplied at 1200, 2400, 4800, 9600, or 19,200 bauds.
c. MIL-STD-188C (mark = +6 ±1 V dc, space = -6 ±1 V dc) with mark equivalent to logic 1 data and space equivalent to logic 0 data. Using a MIL-STD-188C control, data supplied at 75, 150, 300, 600, or



Simplified Block Diagram
Figure 2

1200 bauds. Using a MIL-STD-188C processor, data supplied at 1200, 2400, 4800, 9600, or 19,200 bauds.

Each control word is composed of five 11-bit characters. The last two bits of each character group are stop and parity bits. The first bit is a start bit. The first character of each control word is reserved for equipment address, word identification (subaddress), and word sync information. Bits seven and eight of the second character in each word are reserved for command and status request. The remaining characters of each word carry frequency, control, and monitor information.

Refer to figure 3. Control (and monitor) word timing is accomplished by a crystal-controlled oscillator on the serial interface card. A divider reduces the frequency to the desired values. Strapping permits selection of the baud rate for clock inputs to the various circuits. Selection is from 75, 150, 300, 600, 1200, 2400, 4800, 9600, and 19,200 bauds.

Refer to figure 4. Monitor data (serial data input) is applied to a serial data processor on the serial interface card. Word and status information is decoded from the monitor data and is used to determine strobe address information. The monitor data is then

applied to the data input of four word serial-to-parallel converters on the associated parallel output card. Each serial-to-parallel converter is enabled before it accepts and processes the monitor data. This occurs when the strobe address input is decoded and an enable signal is generated by the word enable circuit.

Refer to figure 4. Control information (serial data output) is stored in the multiplexers on the associated parallel input card. Word gate outputs are applied to the mux (multiplexer) address generator, located on the serial interface card. This generator uses the word gate information that is applied back to the multiplexers on the associated parallel input card. The mux address information enables the applicable multiplexer, which shifts the stored parallel information to the serial interface card that shifts the serial data through the FSK keyer or RS-232C driver circuit to the control bus.

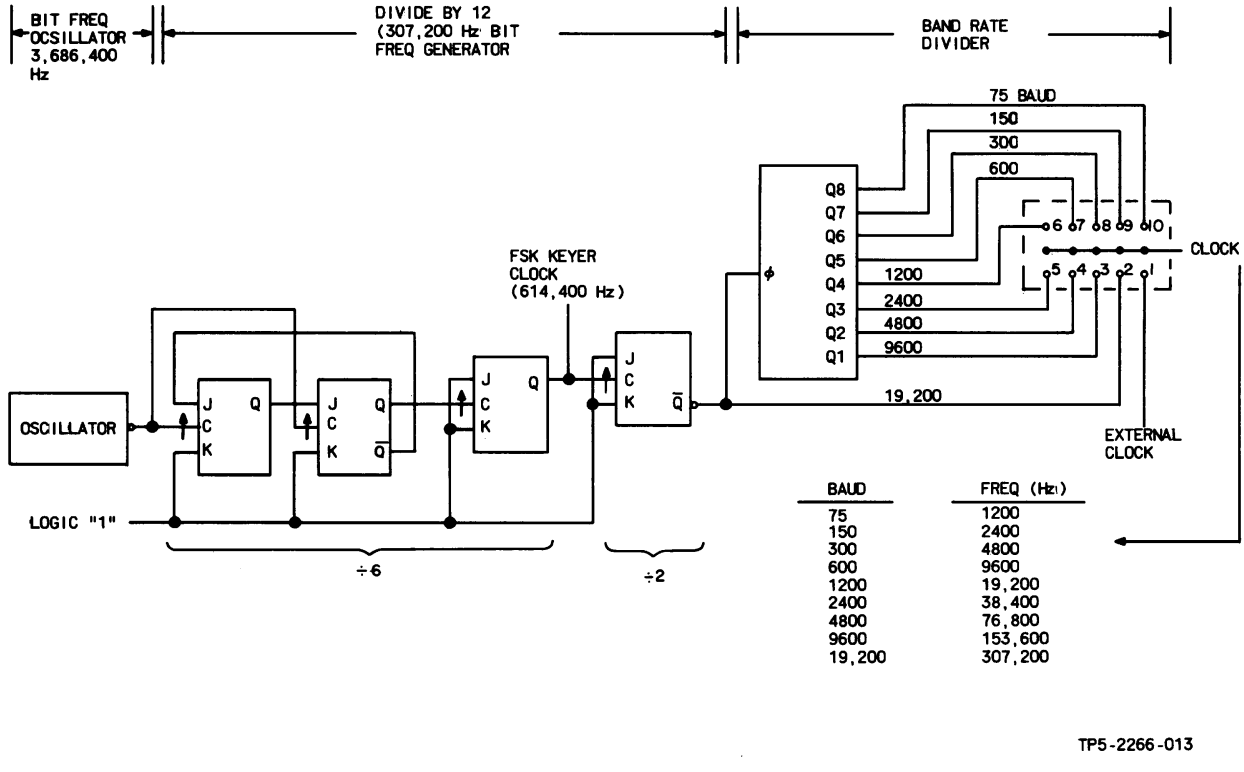
2.3 Monitor Data (Refer to figure 4.)

Monitor data (serial data input) is received by a line receiver and applied, through the FSK demodulator (if FSK strapped), to the UAR/T).

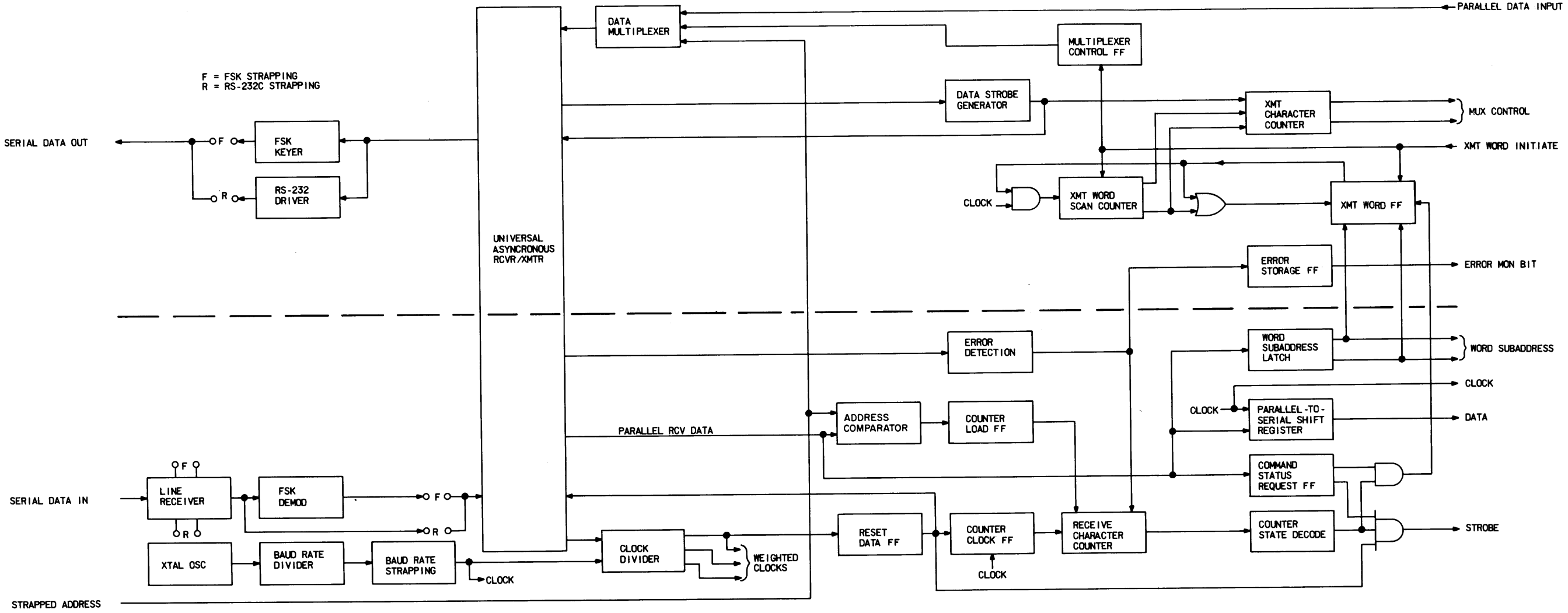
In FSK, the line receiver applies the received FSK signal to the FSK demodulator where a 1280-Hz signal is converted to a logic 1 output and a 2133-Hz signal is converted to a logic 0 output.

In RS-232C or MIL-STD-188C operation, the line receiver converts a +6-V dc input to a logic 0 (ground) output and converts a -6-V dc input to a logic 1 (+4.7-V dc) output.

The UAR/T receives the monitor data input, converts the data word to receive data outputs (RD1 through RD8), and clocks the serial data into the appropriate storage registers on the parallel output card. From the UAR/T, parallel receive data is supplied to the address comparator for comparison to the strapped address. The output of the address comparator enables/disables the receive character counter. The command status is controlled also by the received parallel data. If the command status is enabled, it provides an enable signal to the strobe. With the command status, receive character, and reset data signals applied, a strobe is supplied and data is accepted into the appropriate storage register in the associated parallel output card as determined by the word subaddress.



Bit and Baud Rate Generator
Figure 3



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Block Diagram
Figure 4

2.4 Control Data (Refer to figure 4.)

Control data (serial data output) is transmitted by an FSK keyer (for FSK operation) or by a line driver (for RS-232C or MIL-STD-188C operation).

In FSK, the FSK keyer is strapped and converts logic 0 outputs from the UAR/T to 1280-Hz FSK signal and logic 1 outputs from the UAR/T to 2133 Hz.

In RS-232C or MIL-STD-188C operation, the line driver converts logic 0 inputs to the line driver to +6 V dc and logic 1 inputs to the line driver to -6 V dc.

Parallel input data are address selected and applied to the UAR/T, and supplied as serial output (so) data to the line driver or FSK keyer. The serial data is converted to the appropriate signal data and supplied to the associated remote unit/control.

2.5 Purpose of Strapping

2.5.1 FSK Control (F Straps)

All straps marked "F" are in place. All straps marked "R" or "MIL" are removed. Baud rate is strapped for 75, 150, 300, or 600 bauds (same as associated unit control).

a. Strap between J1-54 and resistor R7 provides a 600-ohm load between J1-54 and J1-55.
b. Strap between C2 and R3 completes circuit to noninverting input of U34A to allow balanced ac (FSK) operation.
c. Strap between R1 and R2 paralleling these resistors makes inverting input load approximately equal to the noninverting input load.
d. Strap between U34A-2 to R6 provides degenerative feedback to U34A opamp.
e. Strap between CR1-anode to R78 provides a positive clipper for the FSK signal.
f. Strap between U12-7 and U20B-5 connects the FSK demodulator output to the UAR/T input.
g. Strap between J1-26 and C48 connects the FSK keyer output to the control data line.

2.5.2 RS-232C Control (R Straps)

All straps marked "R" are in place. All straps marked "F" or "MIL" are removed. Baud rate is strapped at any rate (same as associated unit/control).

a. Strap between J1-54 and R2 provides direct dc connection to opamp U34A.
b. Strap between J1-55 and ground provides reference for monitor data return.
c. Strap between U34A-3 and R4 provides reference for U34A noninverting input.
d. Strap between U34A-3 and R6 provides degenerative feedback to U34A opamp.
e. Strap between U20B-5 and R78 connects line receiver output to UAR/T input for RS-232C or MIL-STD-188C operation.
f. Strap between J1-26 and CR14-anode connects RS-232C driver output to control data line.
g. Strap between J1-27 and ground provides reference for control data return.

2.5.3 MIL-STD-188C Control (MIL Strap and R Straps)

All straps marked "R" are in place (see paragraph 2.5.5) and one strap marked "MIL" is in place. All straps marked "F" are removed. Baud rate is strapped at any rate (same as associated unit/control).

a. Strap between U9D-13 and ground inverts serial inputs to and serial outputs from UAR/T allowing application of MIL-STD-188C signals.

2.5.4 Parity

2.5.4.1 Odd Parity (O Strap)

Strapped between CR3-cathode and ground to recognize odd parity inputs.

2.5.4.2 Even Parity (E Strap)

Strapped between CR3-anode and ground to recognize even parity inputs.

2.5.4.3 No Parity

O and E straps are removed when input parity is insignificant.

2.5.5 Test Strap (Y Strap)

Strap between U20C-9 and U52B-6 removed for test purposes. Strap in place for normal operation.

2.5.6 Address Recognition (A Strap)

Strap between U5B-4 and U1A-8 provides address recognition. Serial interface card recognizes data inputs only if address input matches the address strapping provided by the unit/control in which the serial interface card is installed.

2.5.7 Baud Rate

Strap for applicable baud rate as follows:

a. 75 bauds — strap between baud pin 10 and center pin.
b. 150 bauds — strap between baud pin 9 and center pin.
c. 300 bauds — strap between baud pin 8 and center pin.
d. 600 bauds — strap between baud pin 7 and center pin.
e. 1200 bauds — strap between baud pin 6 and center pin.
f. 2400 bauds — strap between baud pin 5 and center pin.
g. 4800 bauds — strap between baud pin 4 and center pin.
h. 9600 bauds — strap between baud pin 3 and center pin.
i. 19,200 bauds — strap between baud pin 2 and center pin.
j. External bauds — strap between baud pin 1 and center pin. External baud may be any between 75 and 19,200 bauds (baud is 1/16 of applied frequency).

2.5.8 Spares (S Straps)

S straps have no associated electrical circuits. They are used only for storing unused straps.

2.6 Presettable Up/Down Counter CD4029A (Refer to figure 5.)

The CD4029A consists of a 4-stage binary or bcd decade presettable up/down counter with provisions for look-ahead carry in both counting modes.

A high preset enable signal allows information on the jam inputs to preset the counter to any state asynchronously with the clock. A low on each jam line, when the preset enable is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the carry-in and preset enable signals are low. Advancement is inhibited when the carry-in or preset enable signals are high. The carry-out signal is normally high and goes low when the counter reaches its maximum count in the up mode or the minimum count in the down mode, provided the carry-in signal is low. The carry-in signal in the low state can thus be considered a clock-enable. The carry-in terminal must be connected to V_{SS} when not in use.

Binary counting is accomplished when the binary/decade input is high; the counter counts in the decade mode when the binary/decade input is low. The counter counts up when the up/down input is high, and down when the up/down input is low.

2.7 Exclusive OR Gate CD4030A (Refer to figure 6.)

Exclusive OR gate CD4030A consists of four 2-input exclusive OR gates in a package. The exclusive OR gate is commonly used as a pulse generator similar to that shown in figure 6.

2.8 8-Stage Shift Register CD4021A (Refer to figure 7.)

The CD4021A is an 8-stage parallel or serial-input/serial-output shift register having common clock and parallel/serial control inputs, a single serial data input, and individual parallel jam inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. Q outputs are available from the sixth, seventh, and eighth stages.

When the parallel/serial control input is low, data is serially shifted into the 8-stage register synchronously with the positive-going transition of the clock pulse.

When the parallel/serial control input is high, data is jammed into the 8-stage register via the parallel input lines asynchronously with the clock line.

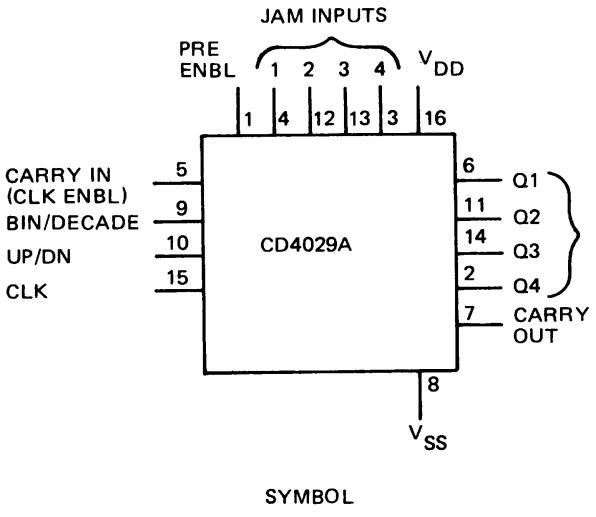
2.9 Dual D-Type Flip-Flop CD4013A (Refer to figure 8.)

The CD4013A consists of two identical, independent, data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset input, respectively.

2.10 UAR/T AY-5-1013

2.10.1 General (Refer to figure 9 and to table 1.)

The UAR/T is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, five to eight data bits,



SYMBOL

CHARACTERISTICS

V_{DD}: +3 TO +15 V DC
V_{SS}: 0 V

OUTPUT VOLTAGE:
LOW LEVEL: V_{SS} +0.05 V DC MAX.
HIGH LEVEL: V_{DD} −0.05 V DC MIN.

CLK FREQ: 2.5 MHz TYP (WITH V_{DD} AT +5 V DC)
5.0 MHz TYP (WITH V_{DD} AT +10 V DC)

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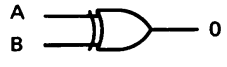
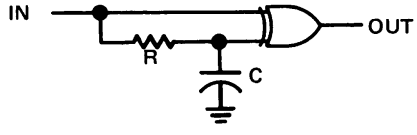
Presettable Up/Down Counter CD4029A
Figure 5

2–INPUT
EXCLUSIVE OR GATE



INPUTS		OUTPUT
A	B	0
0	0	0
1	0	1
0	1	1
1	1	0

PULSE GENERATOR



INPUT	OUTPUT	
0	0	
1	0	
0 → 1	⎍	NOTE 1
1 → 0	⎍	NOTE 1

NOTE:
1. PULSE WIDTH DEPENDANT ON VALUE OF R AND C.

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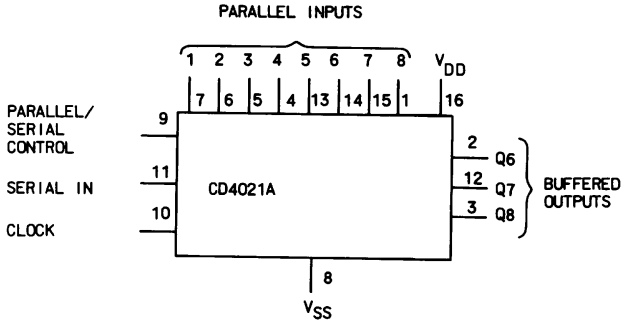
Exclusive OR Gate CD4030A
Figure 6



CHARACTERISTICS

V_{DD}: +3 TO +15 V DC

V_{SS}: 0 V

OUTPUT VOLTAGE:

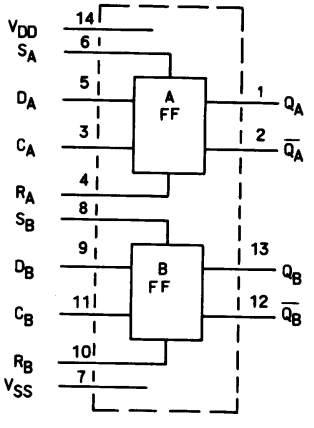
LOW LEVEL: V_{SS} +0.05 V DC MAX.

HIGH LEVEL: V_{DD} -0.05 V DC MIN.

CLOCK FREQ: 2.5 MHz TYP (WITH V_{DD} AT +5 V DC)
5.0 MHz TYP (WITH V_{DD} AT +10 V DC)

TP5-2269-014

8-Stage Static Shift Register CD4021A
Figure 7



TRUTH TABLE

C	D	R	S	Q	$\overline{Q}$	
0→1	0	0	0	0	1	
0→1	1	0	0	1	0	
1→0	X	0	0	Q	$\overline{Q}$	NO CHANGE
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

X = EITHER 1 OR 0

CHARACTERISTICS

V_{DD} : +3 TO +15 V DC

V_{SS} : 0 V

OUTPUT VOLTAGE:
LOW LEVEL: V_{SS} +0.05 V DC MAX.
HIGH LEVEL: V_{DD} -0.05 V DC MIN.
CLOCK FREQ: 4 MHz TYP (WITH V_{DD} AT +5 V DC)
10 MHz TYP (WITH V_{DD} AT +10 V DC)

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Dual D-Type Flip-Flop CD4013A
Figure 8

one or two stop bits, and either odd/even parity or no parity. In order to make the UAR/T universal, the baud, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip. All inputs and outputs are directly compatible with MTOS/MTNS logic, and also with TTL/DTL/CMOS logic without the need for interfacing components. All strobed outputs are 3-state logic.

2.10.2 Receiver Operation (Refer to figure 10.)

Power is applied, external reset is enabled, and clock pulse having a frequency of 16 times the desired baud is applied. The previous conditions will set data available (DAV) to a logic 0.

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter, making individual control bit setting unnecessary. Data reception starts when serial input signal changes from marking (logic 1) to spacing (logic 0), which initiates the start bit. The start bit is valid if, after transition from logic 1 to logic 0, the S1 line continues to be at logic 0 when center sampled, 8 clock pulses later. If, however, line is at a logic 1 when center sampling occurs, the start bit verification process will be reset. If the serial input line transitions from a logic 1 to a logic 0 (marking to spacing) when the 16X clock is in a logic 1 state, the bit time for center sampling will begin when the clock line transitions from a logic 1 to a logic 0 state. After verification of a genuine start bit, data bit reception, parity bit reception, and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s), the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip-flop and/or the framing error flip-flop to a logic 1. It should be noted that, if the no parity mode is selected, the PE (parity error) will be set unconditionally to a logic 0.

Once a full character is received, internal logic looks at the data available (DAV) signal to determine if data has been read out. If the DAV signal is at a logic 1, the receiver will assume data has not been read out and the overrun flip-flop of the status word holding register will be set to a logic 1. If the DAV signal is at a logic 0, the receiver will assume that data has been read out. After DAV goes to a logic 1, the receiver shift register is ready to accept the next character and has one full character time to remove the received character.

2.10.3 Transmitter Operation (Refer to figure 11.)

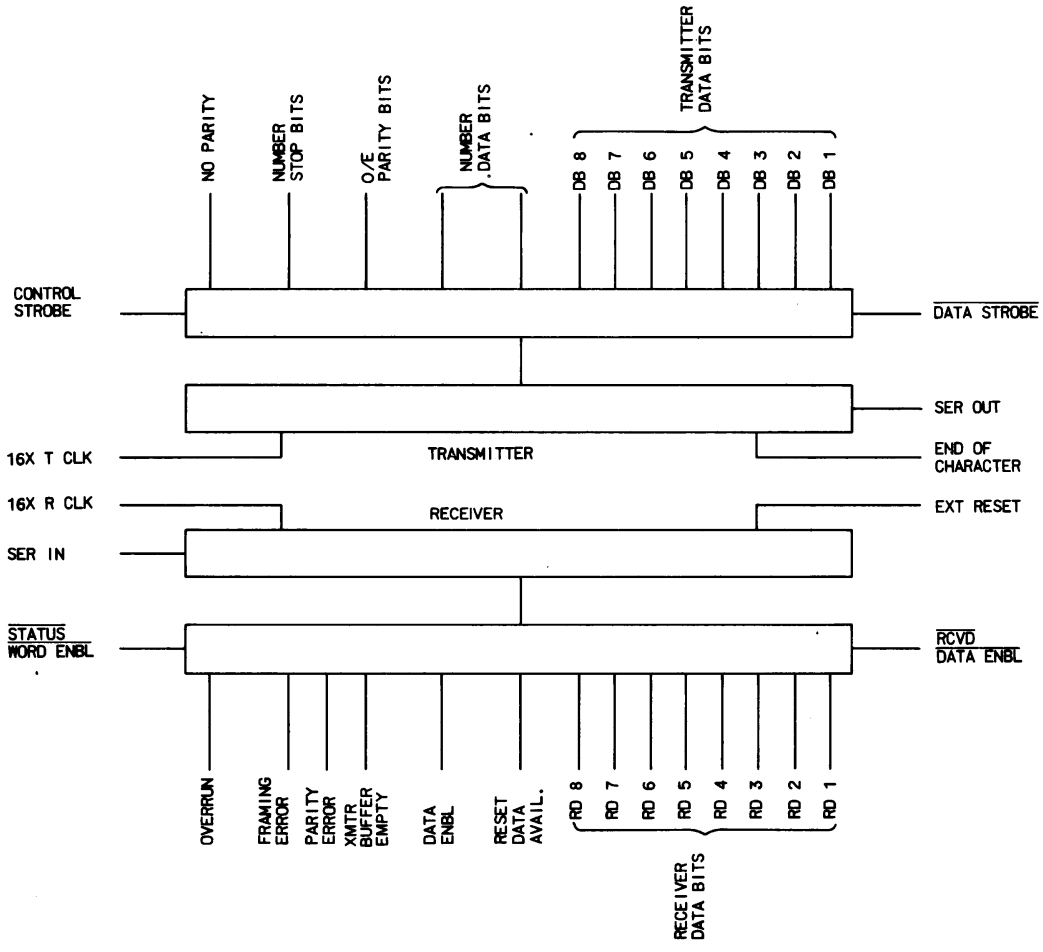
Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud. The above conditions will set TBMT, EOC, and SO to logic 1 (line is marking).

After initializing is completed, user may set control bits and data bits, with control bits selection normally occurring before data bits selection. However, one may set both DS and CS simultaneously if minimum pulse width specifications are followed. Once data strobe (DS) is pulsed, the TBMT signal will change from a logic 1 to a logic 0 indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and that the transmitter shift register is transmitting previously loaded data. TBMT will return to a logic 1. When the transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic 0, and EOC going to a logic 0, indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed, due to double buffering (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired), and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic 1, indicating that a new character is ready for transmission. This new character will be transmitted only if TBMT is a logic 0 as was previously discussed.

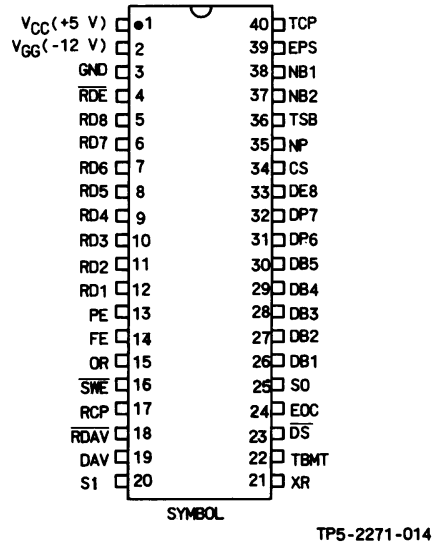
2.11 Phase-Locked Loop NE565A (Refer to figure 12.)

The NE565A phase-locked loop is a self-contained, adaptable filter and demodulator for the frequency range from 0.001 Hz to 500 kHz. The circuit is comprised of a vco, a phase detector, an amplifier, and a low-pass filter. The center frequency of the phase-locked loop is determined by the free-running frequency of the vco. The vco frequency is adjusted externally with a resistor or a capacitor. The low-pass filter that determines the capture characteristics of the loop is formed by an internal resistor and an external capacitor.



CHARACTERISTICS

V_{GG}: -12 V DC ±5%
V_{CC}° +5 V DC ±5%
INPUT LOGIC LEVELS: LOGIC 0, 0 TO +0.8 V DC;
LOGIC 1, V_{CC} -1.5 V DC TO V_{CC} +0.3 V DC
OUTPUT LOGIC LEVELS: LOGIC 0, NMT +0.4 V DC;
LOGIC 1, NLT V_{CC} -1.0 V DC
CLOCK FREQUENCY: DC TO 480 kHz
BAUD: 0 TO 30 k BAUD
CLOCK PULSE: 1.0 uS MIN.
CONTROL STROBE: 300 nS MIN.
EXTERNAL RESET: 500 nS MIN.
STATUS WORD ENABLE: 500 nS MIN.
RESET DATA ENABLE: 250 nS MIN.
RECEIVED DATA ENABLE: 500 nS MIN.
DATA STROBE: 190 nS MIN.



SYMBOL

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UAR/T AY-5-1013
Figure 9

Table 1. UAR/TAY-5-1013, Pin Functions.

PIN NO.	NAME (SYMBOL)	FUNCTION
1	V_{cc} power supply (V_{cc})	+5-V supply.
2	V_{GG} power supply (V_{GG})	-12-V supply.
3	Ground (V_{GD})	Ground.
4	Received data enable (RDE)	A logic 0 on the receiver enable line places the revised data onto the output lines.
5-12	Received data bits (RD8-RD1)	These are the eight data output lines. Received characters are right justified; the LSB always appears on RD1. These lines have tristate outputs; ie, they have the normal TTL output characteristics when ROE is 0 and a high impedance state when RDE is 1. Thus, the data output lines can be bus structure oriented.
13	Parity error (PE)	This line goes to a logic 1 if the received character parity does not agree with the selected parity. Tristate.
14	Framing error (FE)	This line goes to a logic 1 if the received character has no valid stop bit. Tristate.
15	Overrun (OR)	This line goes to a logic 1 if the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register. Tristate.
16	Status word enable (SWE)	A logic 0 on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. Tristate.
17	Receiver clock (RCP)	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud.
18	Reset data available (RDAV)	A logic 0 will reset the DAV line. The DAV F/F is only thing that is reset.
19	Data available (DAV)	This line goes to a logic 1 when an entire character has been received and transferred to the receiver holding register. Tristate.
20	Serial input (SI)	This line accepts the serial bit input stream. A marking (logic 1) to spacing (logic 0) transition is required for initiation of data reception.
21	External reset (XR)	Resets all registers except the received data register. Sets SO, EOC, and TBMT to a logic 1. Resets DAV, and error flags to 0. Clears input data buffer. Must be tied to logic 0 when not in use.

Table 1. UAR/T AY-5-1013, Pin Functions (Cont).

PIN NO.	NAME (SYMBOL)	FUNCTION
22	Transmitter buffer empty (TBMT)	The transmitter buffer empty flag goes to a logic 1 when the data bits holding register may be loaded with another character. Tristate.
23	Data strobe (DS)	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of DS. Data must be stable during entire strobe.
24	End of character (EOC)	This line goes to a logic 1 each time a full character is transmitted. It remains at this level until the start of transmission of the next character.
25	Serial output (SO)	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic 1 when no data is being transmitted.
26-33	Data bit inputs (DB1-DB8)	There are up to eight data bit input lines available.
34	Control strobe (CS)	A logic 1 on this lead will enter the control bits (EPS, BM1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic 1 level.
35	No parity (NP)	A logic 1 on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic 0.
36	Number of stop bits (TSB)	This lead will select the number of stop bits, one or two, to be appended immediately after the parity bit. A logic 0 will insert one stop bit and a logic 1 will insert two stop bits.
37-38	Number of bits/character (NB2, NB1)	These two leads will be internally decoded to select five, six, seven, or eight data bits/character. NB2 NB1 BITS/CHARACTER 0 0 5 0 1 6 1 0 7 1 1 8

Table 1. UAR/T AY-5-1013, Pin Functions (Cont).

PIN NO.	NAME (SYMBOL)	FUNCTION
39	Odd/even parity select (EPS)	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic 0 will insert odd parity and a logic 1 will insert even parity.
40	Transmitter clock (TCP)	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud.

2.12 Voltage Comparator LM311H (Refer to figure 13.)

The LM311H is a voltage comparator with extremely low input currents from a wide range of supply voltages. Its output is compatible with RTL, DTL, and TTL as well as MOS circuits. It can drive lamps or relays, switching voltages up to 40 volts at currents as high as 50 mA.

2.13 12-Stage Ripple-Carry Binary Counter/ Divider CD4040A (Refer to figure 14.)

The CD4040A consists of an input-pulse-shaping circuit and 12 ripple-carry binary counter stages. Resetting the counter to the all-0's state is accomplished by a high level on the reset line. A master-slave flip-flop configuration is used for each counter stage. The state of the counter is advanced one step in binary order on the negative-going transition of the input pulse. All inputs and outputs are fully buffered.

2.14 7-Stage Binary Counter CD4024A (Refer to figure 15.)

The CD4024A consists of an input-pulse-shaping circuit, reset line driver circuit, and seven binary counter stages. The counter is reset to zero by a high level on the reset input. Each counter stage is a static master-slave flip-flop. The counter stage is advanced one count on the negative going transition of each input pulse.

2.15 Quad AND-OR Select Gate CD4019A (Refer to figure 16.)

The CD4019A consists of four AND-OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is made by control bits Ka and Kb. If Ka and Kb are applied simultaneously, a logical A + B function is accomplished.

2.16 Dual Binary Up Counters CD4520B (Refer to figure 17.)

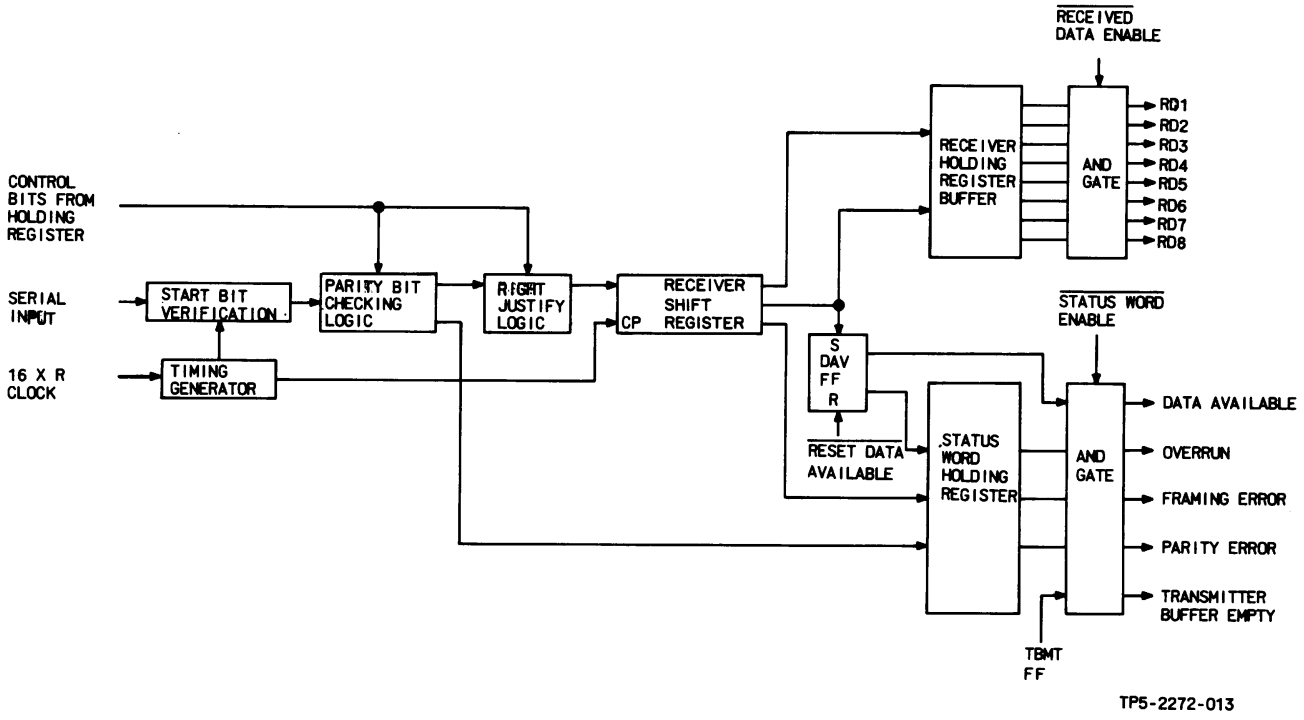
The CD4520B consists of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable clock and enable lines for incrementing on either the positive-going or negative-going transition. For single-unit operation, the enable input is maintained high and the counter advances on each positive-going transition of the clock. The counters are cleared by high levels on their reset lines.

2.17 Dual Operational Amplifier MC1458P1 (Refer to figure 18.)

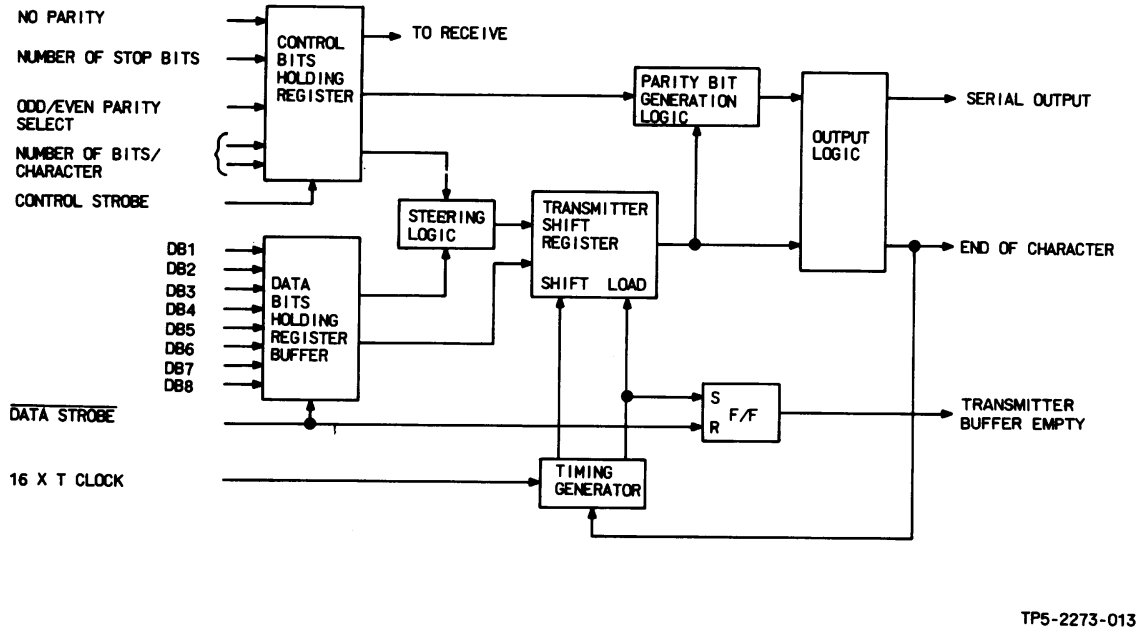
The MC1458P1 consists of two operational amplifiers in one package designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components.

2.18 Dual J-K Master-Slave Flip-Flop CD4027A (Refer to figure 19.)

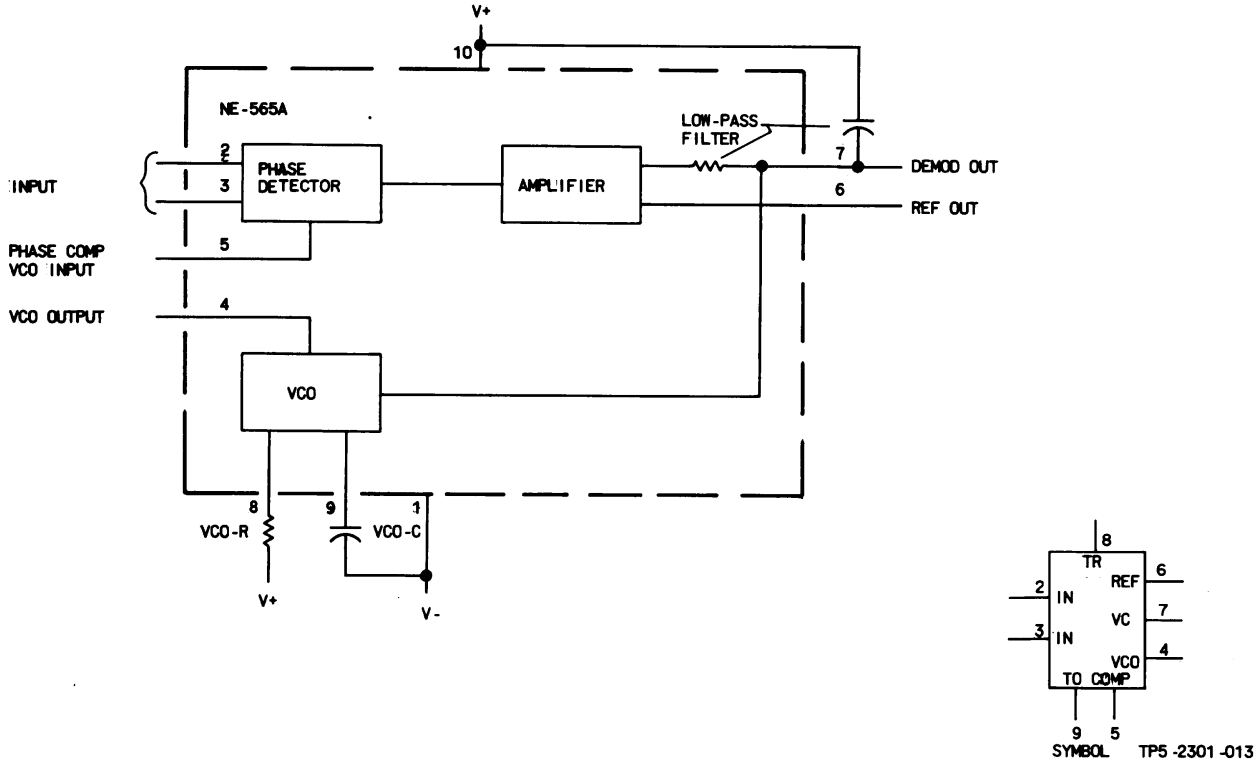
The CD4027A consists of two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has independent J, K, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for control, register, and toggle functions. Logic levels at the J and K inputs, along with internal



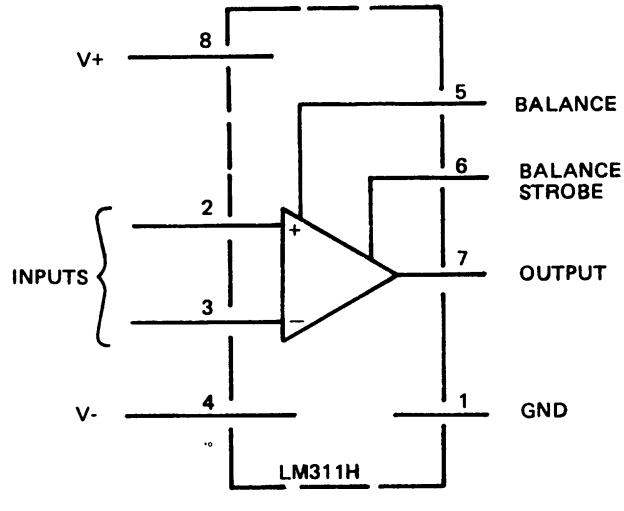
UAR/T Receiver, Block Diagram
Figure 10



UAR/T Transmitter, Block Diagram
Figure 11



Phase-Locked Loop NE565A
Figure 12



CHARACTERISTICS

SUPPLY VOLTAGE: V+ +30 V DC MAX, V− -30 V DC MAX, 40 V MAX BETWEEN V+ AND V−.

INPUT DIFF VOLTAGE: ±30 V MAX

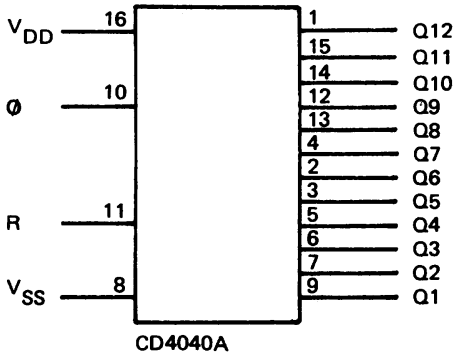
INPUT VOLTAGE: ± 15 V MAX

OUTPUT SHORT CIRCUIT DURATION: 10 s MAX

VOLTAGE GAIN: 200 TYPICAL

TP5-2302-011

Voltage Comparator LM311H
Figure 13



CHARACTERISTICS

V_{DD}: +3 TO +15 V DC

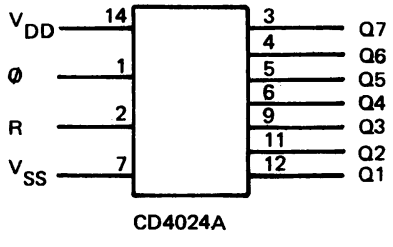
V_{SS}: 0 V

OUTPUT VOLTAGE:
LOW LEVEL: V_{SS} +0.05 V DC MAX.
HIGH LEVEL: V_{DD} −0.05 V DC MIN.

INPUT FREQ (Ø): 1.75 MHz TYPICAL (V_{DD} AT 5 V DC);
5.00 MHz TYPICAL (V_{DD} AT 10 V DC)

TP5-2303-011

12-Stage Ripple-Carry Binary Counter/Divider CD4040A
Figure 14



CHARACTERISTICS

V_{DD}: +3 TO +15 V DC

V_{SS}: 0 V

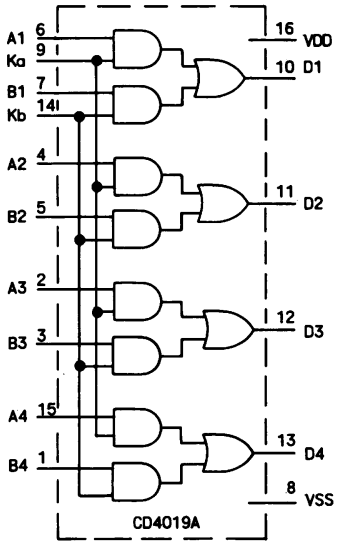
OUTPUT VOLTAGE:
LOW LEVEL: V_{SS} +0.05 V DC MAX.
HIGH LEVEL: V_{DD} −0.05 V DC MIN.

INPUT FREQ (Ø): 2.5 MHz TYPICAL (V_{DD} AT 5 V DC);

7.00 MHz TYPICAL (V_{DD} AT 10 V DC)

TP5-2304-011

7-Stage Binary Counter CD4024A
Figure 15



TRUTH TABLE

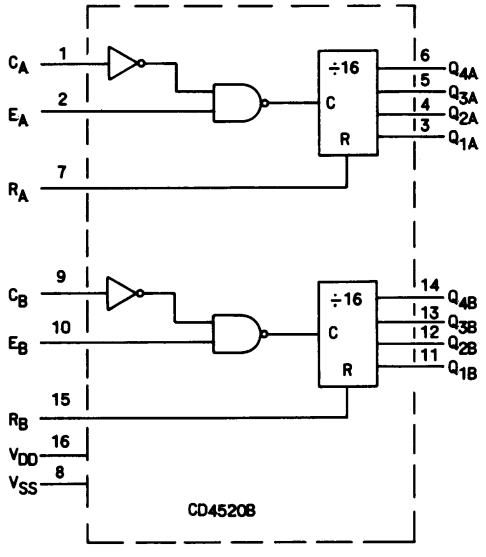
INPUTS				OUTPUT
A	Ka	B	Kb	D
0	0	0	0	0
1	0	0	0	0
0	1	0	0	0
1	1	0	0	1
0	0	1	0	0
1	0	1	0	0
0	1	1	0	0
1	1	1	0	1
0	0	0	1	0
1	0	0	1	0
0	1	0	1	0
1	1	0	1	1
0	0	1	1	1
1	0	1	1	1
0	1	1	1	1
1	1	1	1	1

CHARACTERISTICS

VDD: +3 TO +15 V DC
VSS: 0V
OUTPUT VOLTAGE:
LOW LEVEL: VSS +0.05 V DC MAX.
HIGH LEVEL: VDD - 0.05 V DC MIN.

TP5-2305-013

Quad AND-OR Select Gate CD4019A
Figure 16



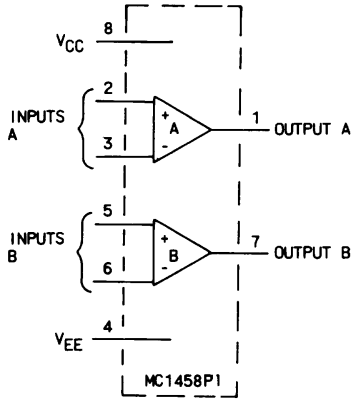
CHARACTERISTICS

V_{DD}: +3 TO +18 V DC
V_{SS}: 0 V
OUTPUT VOLTAGES:
LOW LEVEL: V_{SS} +0.05 V DC MAX.
HIGH LEVEL: V_{DD} -0.05 V DC MIN.

CLOCK FREQ:
1.5 MHz MAX (V_{DD} AT 5 V DC)
3 MHz MAX (V_{DD} AT 10 V DC)
4 MHz MAX (V_{DD} AT 15 V DC)

TP3-2306-013

Dual Binary Up Counters CD4520B
Figure 17

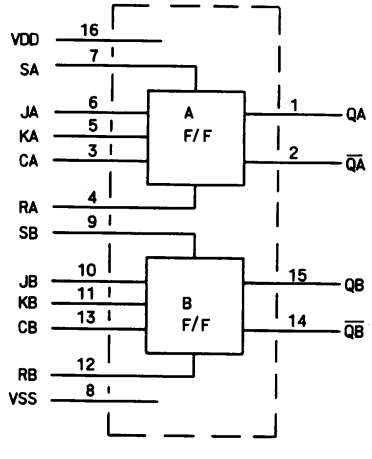


CHARACTERISTICS
SUPPLY VOLTAGE: V_{CC} +18 V DC MAX
V_{EE} -18 V DC MAX
INPUT DIFF VOLTAGE: ±30 V MAX
INPUT COMMON MODE VOLTAGE:
±15 V MAX (1)
OUTPUT SHORT CIRCUIT DURATION:
CONTINUOUS (2)
INPUT RESISTANCE: 300 kΩ MIN, 2.0 MΩ MAX
OUTPUT RESISTANCE: 75Ω TYPICAL
VOLTAGE GAIN: 15 MIN

NOTES:
(1) FOR SUPPLY VOLTAGE LESS THAN ±15.0 V, MAX INPUT VOLTAGE EQUAL TO SUPPLY VOLTAGE.
(2) SUPPLY VOLTAGE EQUAL TO OR LESS THAN 15 V.

TP5-2285-013

Dual Operational Amplifier MC1458P1
Figure 18



CHARACTERISTICS

VDD: +3 TO +15 V DC
VSS: 0V
OUTPUT VOLTAGE
LOW LEVEL: VSS +0.05 V DC MAX
HIGH LEVEL: VDD -0.05 V DC MIN
CLOCK FREQ:
3 MHz TYP (VDD AT +5 V DC)
8 MHz TYP (VDD AT +10 V DC)

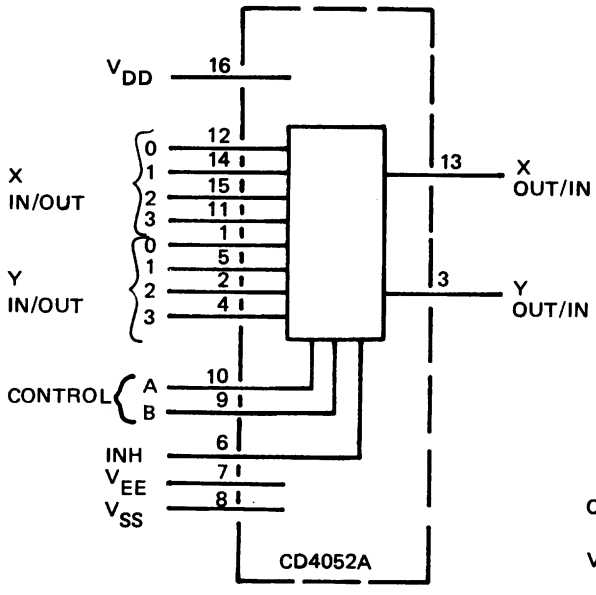
TRUTH TABLE

PRESENT STATE					C	NEXT STATE		
INPUTS				OUTPUTS		OUTPUTS		
J	K	S	R	Q		Q	$\overline{Q}$	
1	X	0	0	0	↑	1	0	
X	0	0	0	1	↑	1	0	
0	X	0	0	0	↑	0	1	
X	1	0	0	1	↑	0	1	
X	X	0	0	X	↓			← NO CHANGE
X	X	1	0	X		1	0	
X	X	0	1	X	X	0	1	
X	X	1	1	X	X	1	1	

X = EITHER 1 OR 0

TP5-2307-013

Dual J-K Master-Slave Flip-Flop CD4027A
Figure 19



TRUTH TABLE

INPUTS			OUTPUT
INHIBIT	A	B	X–Y
0	0	0	0X, 0Y
0	1	0	1X, 1Y
0	0	1	2X, 2Y
0	1	1	3X, 3Y
1	X	X	NONE

X=EITHER 1 OR 0

CHARACTERISTICS

V_{DD}: +3 TO +15 V DC

V_{SS}: 0 V

V_{EE}: −12 TO 0 V DC

ON RESISTANCE:

80 OHM (V_{DD} TO V_{EE} IS 15 V DC)

120 OHM (V_{DD} TO V_{EE} IS 10 V DC)

270 OHM (V_{DD} TO V_{EE} IS 5 V DC)

TP5-2308-011

Differential 4-Channel Multiplexer/Demultiplexer CD4052A
Figure 20

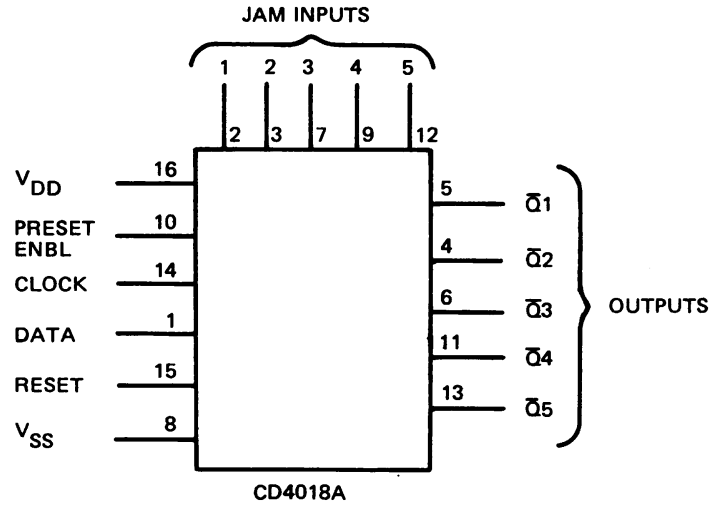
self-steering, control the state of each flip-flop. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset input, respectively.

2.19 Differential 4-Channel Multiplexer/ Demultiplexer CD4052A (Refer to figure 20.)

The CD4052A is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The binary control inputs select one of four pairs of channels to be turned on, and connect the differential analog inputs to the differential outputs.

2.20 Presettable Divide-by-N Counter CD4018A (Refer to figure 21.)

The CD4018A consists of five Johnson-counter stages, buffered $\overline{Q}$ outputs from each stage, and counter preset control gating. Clock, reset, data, preset enable, and five individual jam inputs are provided. A divide-by-10, -8, -6, -4, or -2 counter is implemented by feeding the $\overline{Q}5$, $\overline{Q}4$, $\overline{Q}3$, $\overline{Q}2$, and $\overline{Q}1$ signals, respectively, back to the data input. Divide-by-9, -7, -5, or -3 counter configurations are implemented by using an external gate package to properly gate the feedback connection to the data input. Divide-by functions greater than 10 can be achieved by use of multiple



CHARACTERISTICS

V_{DD}: +3 TO +15 V DC

V_{SS}: 0 V

OUTPUT VOLTAGE:
LOW LEVEL: V_{SS} +0.05 V DC
HIGH LEVEL: V_{DD} −0.05 V DC

CLOCK FREQ: 2.5 MHz TYP (V_{DD} AT +5 V DC)
5 MHz TYP (V_{DD} AT +10 V DC)

TP5-2309-011

Presettable Divide-by-N Counter CD4018A
Figure 21

CD4018A. The counter is advanced one count on a positive clock-signal transition. A high reset signal clears the counter to all zeros. A high preset-enable signal allows information on the jam inputs to preset the counter. Antilock gating is provided to assure the proper counter sequence.

3. TESTING AND TROUBLESHOOTING

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the serial interface card are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 2 check total performance of the serial interface card. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

Table 2. Serial Interface, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	***Note*** These testing and troubleshooting procedures are based on using a control unit and an associated local unit. The most effective method of testing and troubleshooting is obtained by installing the questionable serial interface in the control unit. During these tests when a control unit is referred to it is a receiver-exciter control, an exciter control, or a receiver control. When a local unit is referred to it is a receiver-exciter, an exciter, or a receiver. a. Remove top cover of unit containing the serial interface to be tested. b. Remove serial interface. Install it on an extender card and place it in the control unit. c. Set unit LINE SELECTOR switches to 115 V. d. Connect units to 115-V ac power source and set power on. e. Measure dc voltages between the following pins and ground (TP1, brown): J1-23 J1-28 J1-6 f. Strap local unit for address 0. g. Connect local unit to a control unit.	

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	c. Note audio voltmeter reading. d. Remove U10-2 ground and apply ground to U10-3. e. Note audio voltmeter reading. f. Remove U10-3 ground.	0 ±5 dB mW. Step c reading ±5 dB mW.	Check U34B and associated circuits.
3. Serial data command with status request (Cont)	a. Set local unit front-panel CONT switch to REM. b. Set control unit ADDRESS to 0. ***Note*** Local unit is strapped for address 0 recognition. Address strap A must be installed. c. Set control unit front-panel controls as follows: FREQUENCY KHZ to 29999.9 (0). MODE to SSB/CW or USB. BANDWIDTH to USB (receiver only). RF GAIN to full ccw (receiver and receiver-exciter only). AGC to FAST (receiver and receiver-exciter only). MIC to CH A (exciter and receiver-exciter only). KEY to NORM (exciter and receiver-exciter only). PA PWR to STBY (exciter and receiver exciter only). P CAR to OFF (exciter and receiver-exciter only). CONT to NORM. d. Set control unit ADDRESS to 1. e. Change any and all of controls in step e.		

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	f. Note response signals on the control unit as follows:		
	EQUIPMENT STATUS indicators	No change in indications.	Check U3, U4, U5, and associated address circuits.
	BANDWIDTH indicators (receiver only).	No change in indications.	
	FREQUENCY KHZ indicators.	No change in indications.	
	g. Set control unit ADDRESS to 0.		
	h. Note response signals on the control unit as follows:		
	EQUIPMENT STATUS indicators.	No fault indications, MODE indicates USB (exciter and receiver-exciter), MODE indicates SSB/CW (receiver only).	Check U7, U6, U8, U9, U20, U21, U11, U12, U34, and associated circuits.
	BANDWIDTH indicators (receiver only).	Indicates U (USB).	
	FREQUENCY KHZ indicators.	Indicates 29999.9 (0) kHz.	
	Note Do not connect ground lead to J1-30 until frequency indication is normal (29999.9).		
	i. Connect a storage oscilloscope to TP6 (blue). Sweep time = 10 ms. Trigger = TRIGGER. Vert scale = 1 V per division. Horiz sweep = Normal. Display = STORE.		
	j. Connect a jumper from J1-30 to ground.	R/E FAULT indicator flashes at 0.5-Hz rate (2 s on, 2 s off).	
	k. On control unit, change any FREQUENCY KHZ control.	Oscilloscope display should look similar to command word with status request word 1 (refer to figure 22). Each frequency change changes data pattern.	Check U8, U28, U41, U29, U30, and associated circuits.
(Cont)			

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)		**Note** Without special equipment it is impossible to note exact waveform. Look at spacing and bits of data.	
	l. Erase scope and repeat step k as often as necessary to obtain a good result. **Note** 10-MHz and 1-MHz frequency controls change bit pattern of word 1, character 2. 100-kHz and 10-kHz frequency controls change bit pattern of word 1, character 3. 1-kHz and 100-Hz frequency controls change bit pattern of word 1, character 4. 10-Hz and 1-Hz frequency controls (if applicable) change bit pattern of word 1, character 5.		
	m. Erase scope. On control unit, change RF GAIN control position.	Oscilloscope display should look similar to command word with status request, word 2 (refer to figure 22). Each RF GAIN control changes data pattern. Refer to note of step k.	Same as step k.
(Cont)	n. Erase scope and repeat step m as necessary to obtain a good result. **Note** RF GAIN control changes bit pattern of word 2, character 2. AGC switch changes bit pattern of word 2, character 3. VBFO enable switch (if applicable) changes bit pattern of word 2, character 3. BANDWIDTH control and/or MODE control changes bit pattern of word 2, character 4. MODE control changes bit pattern of word 2, character 5.		

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	o. Erase scope. On control unit, change PA PWR control position.	Oscilloscope display should look similar to command word with status request word 3 (refer to figure 22.) Each PA PWR control change changes data pattern. Refer to note of step k.	Same as step k.
	p. Erase scope and repeat step o as often as necessary to obtain a good result. **Note** VBFO control (if applicable) changes bit pattern of word 3, character 2. DVBFO 1-kHz and sign controls (if applicable) change bit pattern of word 3, character 2. DVBFO 100-Hz and 10-Hz controls (if applicable) change bit pattern of word 3, character 3. PA PWR control changes bit pattern of word 3, character 5. P CAR switch changes bit pattern of word 3, character 5.		
	q. Erase scope. On control unit, change KEY control position.	Oscilloscope display should look similar to command word with status request word 4. (Refer to figure 22.) Each application or removal of a key changes data pattern. Refer to note of step k.	Same as step k.
	r. Erase scope and repeat step q as often as necessary to obtain a good result. s. Remove jumper from J1-30 to ground.		
4. Serial data status only (Cont)	a. Repeat steps 3.a. through 3.i. b. Set local unit front-panel controls as follows: FREQUENCY KHZ to 29999.9 (0). MODE to SSB/CW or USB. BANDWIDTH to USB (receiver only).		Same as test 3.

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	RF GAIN to full ccw (receiver and receiver-exciter only). AGC to FAST (receiver and receiver-exciter only). MIC to CH A (exciter and receiver-exciter only). KEY to NORM (exciter and receiver-exciter only). PA PWR to STBY (exciter and receiver-exciter only). P CAR to OFF (exciter and receiver-exciter only). CONT to LCL.		
	c. Change any or all of the above front-panel controls on the control unit.		
	d. Note response signals on the control unit.	No changes.	
	e. Set control unit ADDRESS to 0.		
	f. Note response signals on the control unit as follows:		
	EQUIPMENT STATUS indicators.	No fault indications, mode indicates USB (exciter and receiver-exciter), mode indicates SSB/CW (receiver only), BUSY indicator is lit.	
	BANDWIDTH indicators (receiver only).	Indicates U (USB).	
	FREQUENCY KHZ indicators.	Indicates 29999.9 (0) kHz.	
	g. Connect a storage oscilloscope to TP6 (blue). Sweep time = 20 ms. Trigger = INTERNAL. Vert scale = 1 V per division. Horiz sweep = SINGLE SWEEP. Display = STORE.		
(Cont)	h. Note oscilloscope waveform.	Should look similar to status request only words (refer to figure 22).	

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	i. Repeat steps g and h as often as necessary to obtain a good result.	***Note*** Without special equipment it will be impossible to note exact waveform. Look at spacing and bits of data.	
5. Serial data status only (Cont)	a. Repeat steps 3.a through 3.i. b. Set local unit front-panel controls as follows: FREQUENCY KHZ to 29999.9 (0). MODE to SSB/CW or USB. BANDWIDTH to USB (receiver only). RF GAIN to full ccw (receiver and receiver-exciter only). AGC to FAST (receiver and receiver-exciter only). MIC to CH A (exciter and receiver-exciter only). KEY to NORM (exciter and receiver-exciter only). PA PWR to STBY (exciter and receiver-exciter only). P CAR to OFF (exciter and receiver-exciter only). CONT to LCL. c. Change any or all of the above front-panel controls on the control unit. d. Note response signals on the control unit. e. Set control unit ADDRESS to 0. f. Note response signals on the control unit as follows:	No changes.	Same as test 3.

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	EQUIPMENT STATUS indicators.	No fault indications mode indicates USB (exciter and receiver-exciter), mode indicates SSB/CW (receiver only), BUSY indicator is lit.	
	BANDWIDTH indicators (receiver only).	Indicate U (USB).	
	FREQUENCY KHZ indicators.	Indicates 29999.9 (0) kHz.	
	g. Connect a storage oscilloscope to TP5 (green). Sweep time = 20 ms. Trigger = INTERNAL. Vert scale = 1 V per division. Horiz sweep = SINGLE SWEEP. Display = STORE.		
	h. Note oscilloscope waveform.	Should look similar to monitor word(s)/ command word(s) with no status request, (refer to figure 22). ***Note*** Without special equipment it will be impossible to note exact waveform. Look at spacing and bits of data.	
	i. Repeat steps g and h as often as necessary to obtain a good result.		
6. FSK receiver sensitivity	a. Connect local unit to a control unit through a 40-dB attenuator in both the monitor and data lines. b. Repeat test 3.	Results should be same as test 3 results.	Check U34A and associated circuits.
7. Address recognition (Cont)	a. Set local unit CONT switch to REM. b. Set control unit ADDRESS to 0. c. Set control unit front-panel controls as follows: FREQUENCY KHZ to 29999.9(9).		

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
7. (Cont)	MODE to SSB/CW or USB.		
	BANDWIDTH to USB (receiver only).		
	RF GAIN to full ccw (receiver and receiver-exciter only).		
	AGC to FAST (receiver and receiver-exciter only).		
	MIC to CH A (exciter and receiver-exciter only).		
	KEY to NORM (exciter and receiver-exciter only).		
	PA PWR to STBY (exciter and receiver-exciter only).		
	P CAR to OFF (exciter and receiver-exciter only).		
	CONT to NORM.		
	d. Note response signals on the control unit as follows:		
	EQUIPMENT STATUS indicators.	No fault indications mode indicates USB (exciter, receiver-exciter) or SSB/CW (receiver), PA READY might be lit (exciter, receiver-exciter only).	Check U7, U6, U8, U9, U20, U21, U11, U12, U34, and associated circuits.
	BANDWIDTH indicators (receiver only).	Indicates U (USB).	
	FREQUENCY KHZ indicators.	Indicates 29999.9(9) kHz.	
	e. Set control unit ADDRESS to 1.		
	f. Note response signals on the control unit as follows:		
	EQUIPMENT STATUS indicators.	EXCTR FAULT, RCV FAULT, or R/E FAULT indicator flashes at a 0.25-Hz rate (on 2 seconds, off 2 seconds). All other indications should remain the same.	Check U3, U4, U5, U27, U28, U29, U30, U8, and associated circuits. Check also busy circuit on parallel output.
(Cont)	BANDWIDTH indicators (receiver only).	No change from step d.	

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

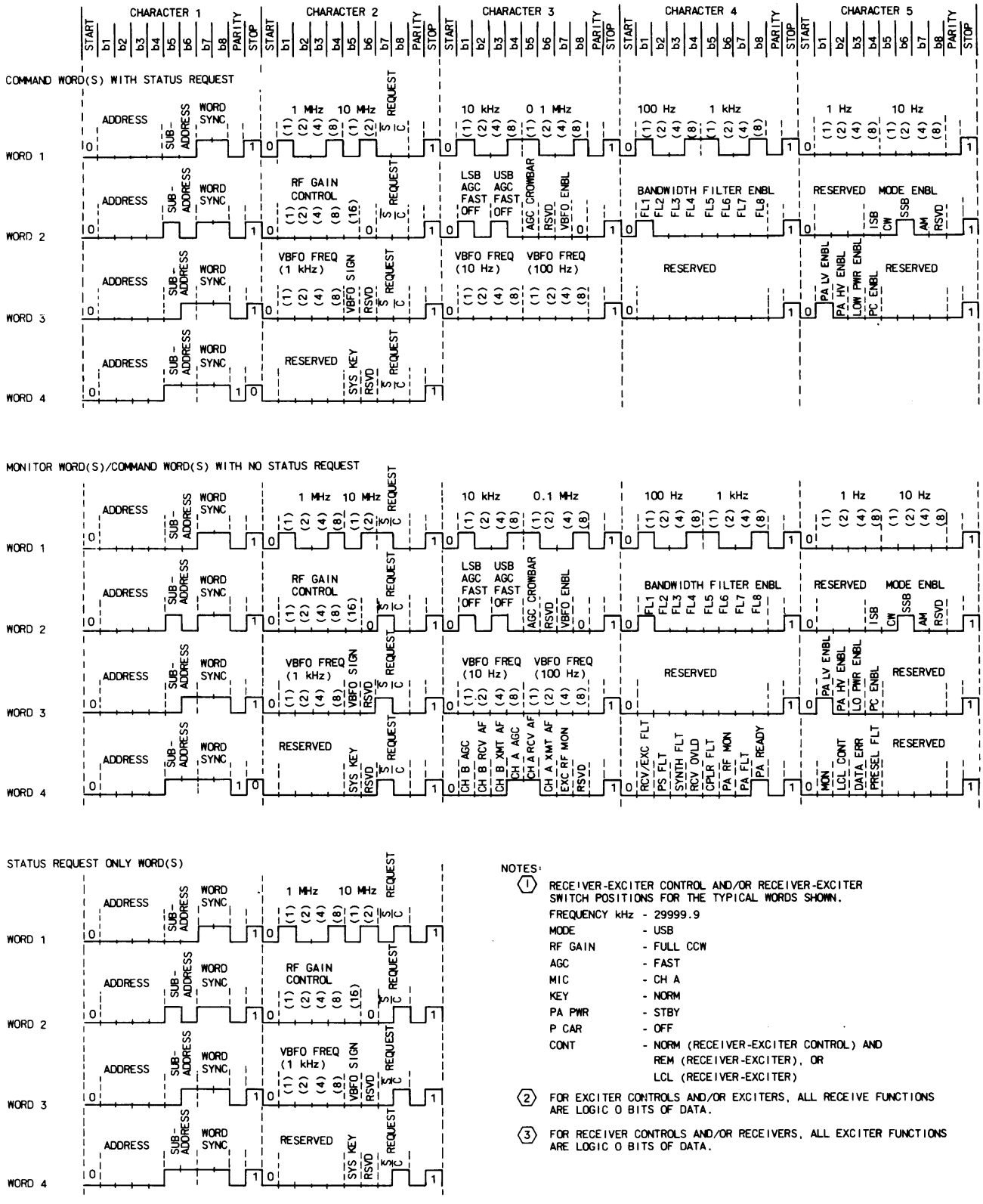
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
7. (Cont)	FREQUENCY KHZ indicators.	No change from step d.	Check U3, U4, U5, U27, U28, U29, U30, U8, and associated circuits. Check also busy circuit on parallel output.
	g. Note response signals on the control unit with the ADDRESS to each position 2 through 15.	Same as step f.	
8. Address	a. Set control unit ADDRESS to 0.		
	b. Ground serial interface pins J1-17 and J1-45.		
	c. Connect an oscilloscope to serial interface pin J1-13.		
	d. Change control unit ADDRESS through all positions 0 through 15 and back to 0 while watching oscilloscope.	A pulse is generated at J1-13 at every change in ADDRESS switch position.	Check U27 and associated circuits.
	e. Remove J1-17 and J1-45 grounds.		
9. Status request	a. Set local unit cont switch to REM.		
	b. Set control unit ADDRESS to 0.		
	c. Connect a dual-trace oscilloscope: One trace to TP6 (blue), and one trace to J1-24.		
	d. Apply a logic 1 pulse to oscilloscope trigger for both traces and A12TP7 (violet) simultaneously.		
	e. Note oscilloscope waveforms.	One trace (TP6) should look similar to status request only words 1 through 4 (refer to figure 22).	If TP6 abnormal check U8, U28, U29, U30, U41, and associated circuits.
		Other trace (J1-24) goes to logic 1 and remains there until status request only word 4 is transmitted and then returns to logic 0.	If J1-24 abnormal check U31, U50, U52, and associated circuits.
	f. Repeat steps c and d as often and as quickly as necessary to obtain a good result.	***Note*** With local unit cont switch in LCL position J1-24 remains at logic 1.	

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
10. Word 4 continuous transmit	a. Set control unit ADDRESS to 0. b. Set control unit CONT switch to NORM. c. Connect oscilloscope to TP6 (blue). Sweep time = 20 ms. Trigger = INTERNAL. Vert scale = 1 V per division. Horiz sweep = NORMAL. d. Apply a ground to J1-30. e. Remove J1-30 ground.	Continuous data monitored on oscilloscope should look similar to status request only word, word 4. Continuous data on oscilloscope is terminated.	Check U37, U38, U48, U40, U41, U9, and associated circuits. Check U17-U18, U19, U23, U24, U25, U26, and associated circuits.
11. Data loop back (Cont)	a. Set control unit address to 0. b. Disconnect control unit from local unit. c. Set control unit CONT switch to TEST. d. Connect a dual-trace storage oscilloscope with upper trace to TP6 (blue) and lower trace to TP5 (green). e. Set oscilloscope as follows: Sweep time = 20 ms. Trigger = INTERNAL. Vert scale = 1 V per division. Horiz sweep = NORMAL. f. Apply a ground to J1-30. g. Set control unit front-panel controls as follows: FREQUENCY KHZ to 29999.0 (9). MODE to SSB/CW or USB. BANDWIDTH to USB (receiver only). RF GAIN to full ccw (receiver and receiver-exciter only). AGC to FAST (receiver and receiver-exciter only). MIC to CH A (exciter and receiver-exciter only). KEY to NORM (exciter and receiver-exciter only). PA PWR to STBY (exciter and receiver-exciter only). P CAR to OFF (exciter and receiver-exciter only).	Continuous data monitored on both traces of oscilloscope should look similar to status request only word, word 4, (refer to figure 27). Continuous data on oscilloscope.	Check U47, U38, U48, U40, U41, U9, and associated circuits. Same as step e.

Table 2. Serial Interface, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
11. (Cont)	h. Set oscilloscope display to STORE.		
	i. Erase display. Set FREQUENCY KHZ to 29999.9(9).	Both oscilloscope traces are identical and look similar to command word with status request, word 1. (Refer to figure 22.)	Same as step e.
	j. Erase display. Set MODE control to AM.	Both oscilloscope traces are identical and look similar to command word with status request, word 2. (Refer to figure 22.)	
	k. Erase display. Set PA PWR to HIGH PWR.	Both oscilloscope traces are identical and look similar to command word with status request, word 3. (Refer to figure 22.)	
	l. Erase display. Set KEY control to LOCK.	Both oscilloscope traces are identical and look similar to command word with status request, word 4. (Refer to figure 22.)	Same as step e.
	m. Set control unit CONT switch to NORM.		
	n. Repeat steps h through k.	Upper trace same as steps h through k. Lower trace, straight line.	
	o. Remove ground from J1-30.		
12. Baud rate check	a. Note baud rate strapped in unit.	Reference.	
	b. Strap baud rate for 75.		
	c. Repeat test 10.	Same as test 10 except monitor word spacing increases as baud rate decreases and vice versa.	Same as test 10.
	d. Strap baud rate for 19 200.		
	e. Repeat test 10.		
	f. Return to baud rate strapping referenced in step a.		



NOTES:

(1) RECEIVER-EXCITER CONTROL AND/OR RECEIVER-EXCITER SWITCH POSITIONS FOR THE TYPICAL WORDS SHOWN.

FREQUENCY kHz	- 29999.9
MODE	- USB
RF GAIN	- FULL CCW
AGC	- FAST
MIC	- CH A
KEY	- NORM
PA PWR	- STBY
P CAR	- OFF
CONT	- NORM (RECEIVER-EXCITER CONTROL) AND REM (RECEIVER-EXCITER), OR LCL (RECEIVER-EXCITER)

(2) FOR EXCITER CONTROLS AND/OR EXCITERS, ALL RECEIVE FUNCTIONS ARE LOGIC 0 BITS OF DATA.

(3) FOR RECEIVER CONTROLS AND/OR RECEIVERS, ALL EXCITER FUNCTIONS ARE LOGIC 0 BITS OF DATA.

TP5-4943-015

Command and Monitor Word Waveforms
Figure 22

4. ALIGNMENT/ADJUSTMENT

4.1 Control Data Strapping (Refer to figure 23.)

4.1.1 FSK Control

a. Remove all R and MIL straps.
b. Set all F straps in place.
c. Set Y strap in place.
d. Set baud rate straps in place. Set baud rate for 75, 150, 300, or 600 bauds (refer to paragraph 4.2).
e. If address recognition required, strap for address (refer to paragraph 4.5).
f. If parity recognition required, strap for parity (refer to paragraph 4.4).

4.1.2 EIA RS-232C Control

a. Remove all F and MIL straps.
b. Set all R straps in place.
c. Set Y strap in place.
d. Set baud rate straps in place, for any baud rate (refer to paragraph 4.2).
e. If address recognition required, strap for address (refer to paragraph 4.5).
f. If parity recognition required, strap for parity (refer to paragraph 4.4).

4.1.3 MIL-STD-188C Control

a. Remove all F straps.
b. Set all R straps in place.
c. Set MIL strap in place.
d. Set Y strap in place.
e. Set baud rate straps in place, for any baud rate (refer to paragraph 4.2).
f. If address recognition required, strap for address (refer to paragraph 4.5).
g. If parity recognition required, strap for parity (refer to paragraph 4.4).

4.2 Baud Rate Strapping

Strap for applicable baud rate as shown in table 3.

4.3 Test Strapping

For test purposes only, remove Y strap. For normal operation, Y strap must be set in place.

4.4 Parity Strapping

4.4.1 Odd Parity

For odd parity recognition, remove E strap and set O strap in place.

4.4.2 Even Parity

For even parity recognition, remove O strap and set E strap in place.

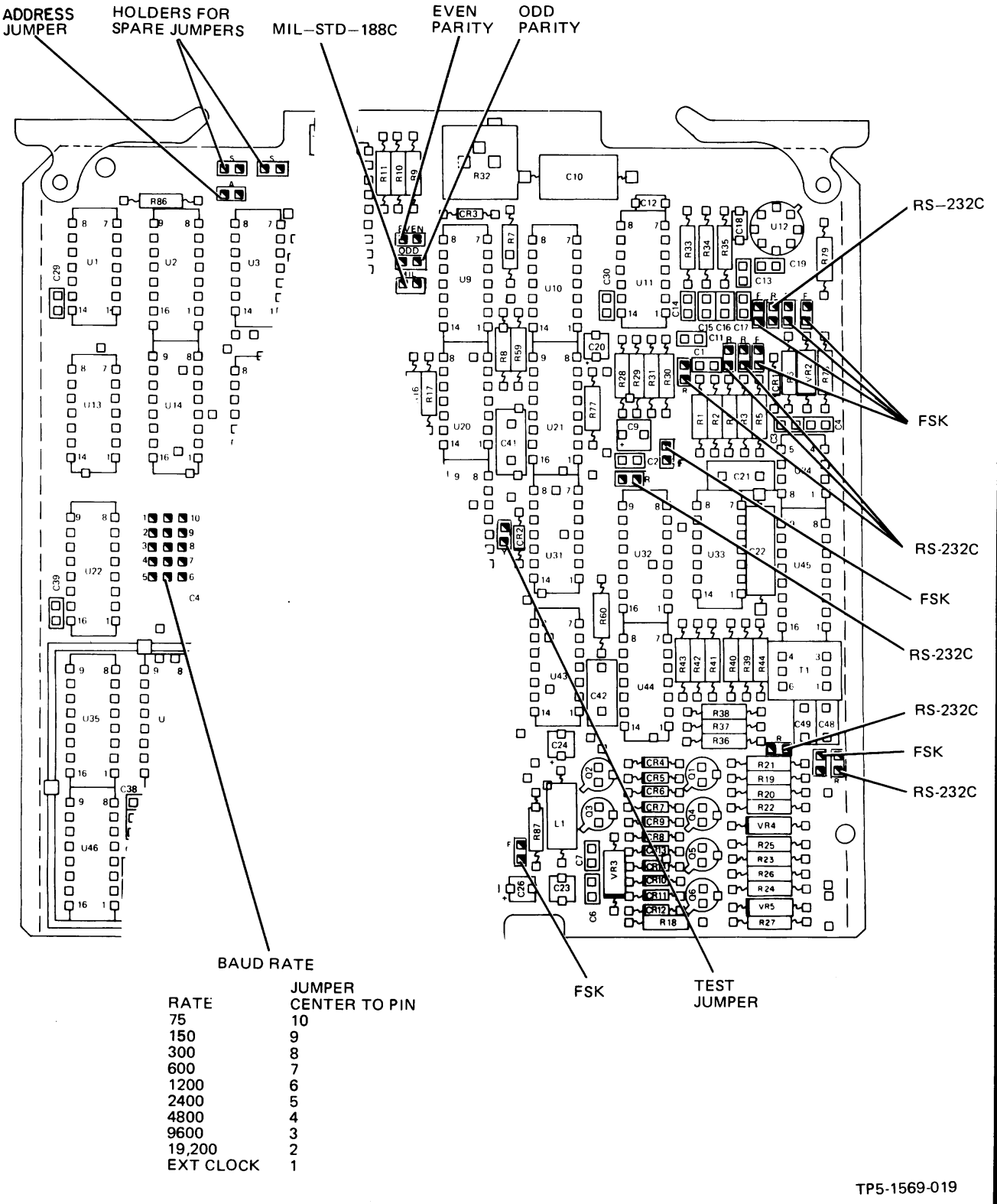
4.4.3 No Parity

If parity recognition is not required, remove both the O and E straps.

Table 3. Baud Rate Strapping.

BAUD RATE (BAUDS)	BAUD STRAP	FSK	RS-232C OR MIL-STD-188C USING	
			CONTROL	PROCESSOR
75	10 to center	X	X	
150	9 to center	X	X	
300	8 to center	X	X	
600	7 to center	X	X	
1200	6 to center		X	X
2400	5 to center			X
4800	4 to center			X
9600	3 to center			X
19 200	2 to center			X
External	1 to center	*	*	*

*Any rate from 75 to 19 200 bauds (baud is 1/16 of applied frequency). FSK cannot exceed 600 bauds.



RATE	JUMPER CENTER TO PIN
75	10
150	9
300	8
600	7
1200	6
2400	5
4800	4
9600	3
19,200	2
EXT CLOCK	1

Serial Interface Strapping
Figure 23

4.5 Address Recognition Strapping

a. If an address is to be recognized, set A strap in place.
b. Strap unit rear connector for specific address recognition as shown in unit installation section.

4.6 Adjustment of FSK Detector Symmetry

a. Perform test setup of table 2, test 1.
b. Strap card for FSK signaling (refer to paragraph 4.1.1).
c. Strap card for 1200 bauds (refer to paragraph 4.2).
d. Strap for odd parity (refer to paragraph 4.4.1).
e. Apply a 0-dB mW FSK signal with a symmetrical 1:1 (mark, space) data pattern between P1-54 and P1-55.
f. Using an oscilloscope, monitor the waveform at TP5 (green) to ground (TP1, brown).
g. Adjust R32 to obtain best symmetry of the waveform at TP5.

5. REPAIR

Repair of the serial interface card is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

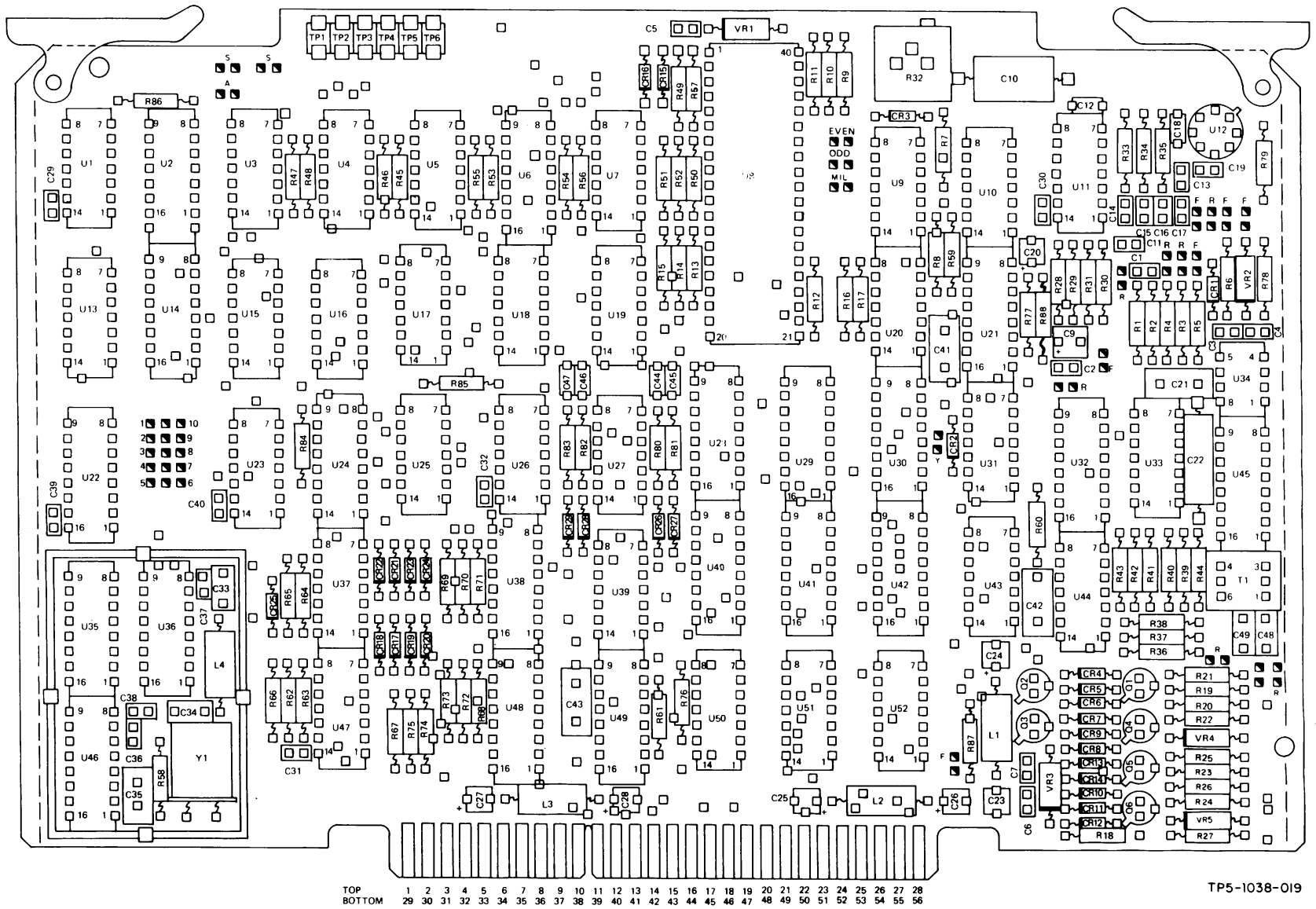
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figure 24). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description is listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Serial Interface	635-0742-001	REV J



Serial Interface, Schematic Diagram
Figure 24 (Sheet 1 of 6)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	SERIAL INTERFACE 635-0742-001		
CR1-CR29	SEMICOND DEVICE, 1N4454	353-3644-010	
C1-C7	CAPACITOR, FXD, CER DIEL, 0.1 μF, 20%, 50V	913-3279-680	
C8	NOT USED		
C9	CAPACITOR, FXD, ELCTLT, 15 μF, 20%, 15V	184-9102-130	
C10	CAPACITOR, FXD, PLSTC DIEL, 0.047 μF, 10%, 200V	933-1039-040	
C11	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-680	
C12	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C13, C14	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-680	
C15-C17	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C18	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C19	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-680	
C20	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	
C21	CAPACITOR, FXD, MICA DIEL, 470pF, 5%, 500V	912-2864-000	
C22	CAPACITOR, FXD, PLSTC DIEL, 0.0056μF, 10%, 80V	933-1039-320	
C23-C28	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	
C29-C32	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-680	
C33, C34	CAPACITOR, FXD, CER DIEL, 1μF, 20%, 50V	913-3279-270	
C35	CAPACITOR, FXD, MICA DIEL, 15pF, 5%, 500V (B3)	912-3839-000	
C35	CAPACITOR, FXD, MICA DIEL, 47pF, 5%, 500V	912-3856-001	
C36-C40	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-680	
C41	CAPACITOR, FXD, MICA DIEL, 200pF, 10%, 500V	912-2838-000	
C42	CAPACITOR, FXD, MICA DIEL, 200pF, 10%, 500V (A1) (A2) (B2)	912-2838-000	
C42	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 500V	912-3879-000	
C43	CAPACITOR, FXD, MICA DIEL, 200pF, 10%, 500V	912-2838-000	
C44-C47	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C48,C49	CAPACITOR, FXD, CER DIEL, 1μF, 20%, 50V	913-3279-270	
L1-L4	COIL, RF, 1000μH	240-2540-000	
Q1	TRANSISTOR, 2N2907A	352-0551-010	
Q2	TRANSISTOR, 2N2222A	352-0661-020	
Q3	TRANSISTOR, 2N2907A	352-0551-010	
Q4	TRANSISTOR, 2N2222A	352-0661-020	
Q5	TRANSISTOR, 2N2907A	352-0551-010	
Q6	TRANSISTOR, 2N2222A	352-0661-020	
R1,R2	RESISTOR, FXD, CMPSN, 47kΩ, 10%, 1/4W	745-0809-000	
R3	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R4	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R5,R6	RESISTOR, FXD, CMPSN, 0.47MΩ, 10%, 1/4W	745-0845-000	
R7,R8	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R9-R20	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R21	RESISTOR, FXD, CMPSN, 1.5kΩ, 10%, 1/4W	745-0755-000	
R22,R23	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W	745-0749-000	
R24	RESISTOR, FXD, CMPSN, 390Ω, 10%, 1/4W	745-0734-000	
R25	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W	745-0749-000	
R26,R27	RESISTOR, FXD, CMPSN, 680Ω, 10%, 1/4W	745-0743-000	
R28	RESISTOR, FXD, CMPSN, 15kΩ, 10%, 1/4W	745-0791-000	
R29	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R30,R31	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R32	RESISTOR, VAR, WW, 5kΩ, 5%, 3/4W	381-1721-060	
R33-R35	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R36-R38	RESISTOR, FXD, FILM, 20.5kΩ, 1%, 1/8W	705-1059-000	
R39,R40	RESISTOR, FXD, FILM, 48.7kΩ, 1%, 1/8W	705-1077-000	
R41,R42	RESISTOR, FXD, FILM, 10kΩ, 1%, 1/8W	705-1044-000	
R43	RESISTOR, FXD, FILM, 20.5kΩ, 1%, 1/8W	705-1059-000	
R44	RESISTOR, FXD, CMPSN, 560Ω, 10%, 1/4W	745-0740-000	
R45-R46	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R49-R57	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R58	RESISTOR, FXD, CMPSN, 10MΩ, 10%, 1/4W	745-0893-000	
R59	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R60	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W (A1) (A2)	745-0773-000	
R61	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	
R62-R65	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R66	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R67-R77	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R78	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 14W	745-0761-000	
R79	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	

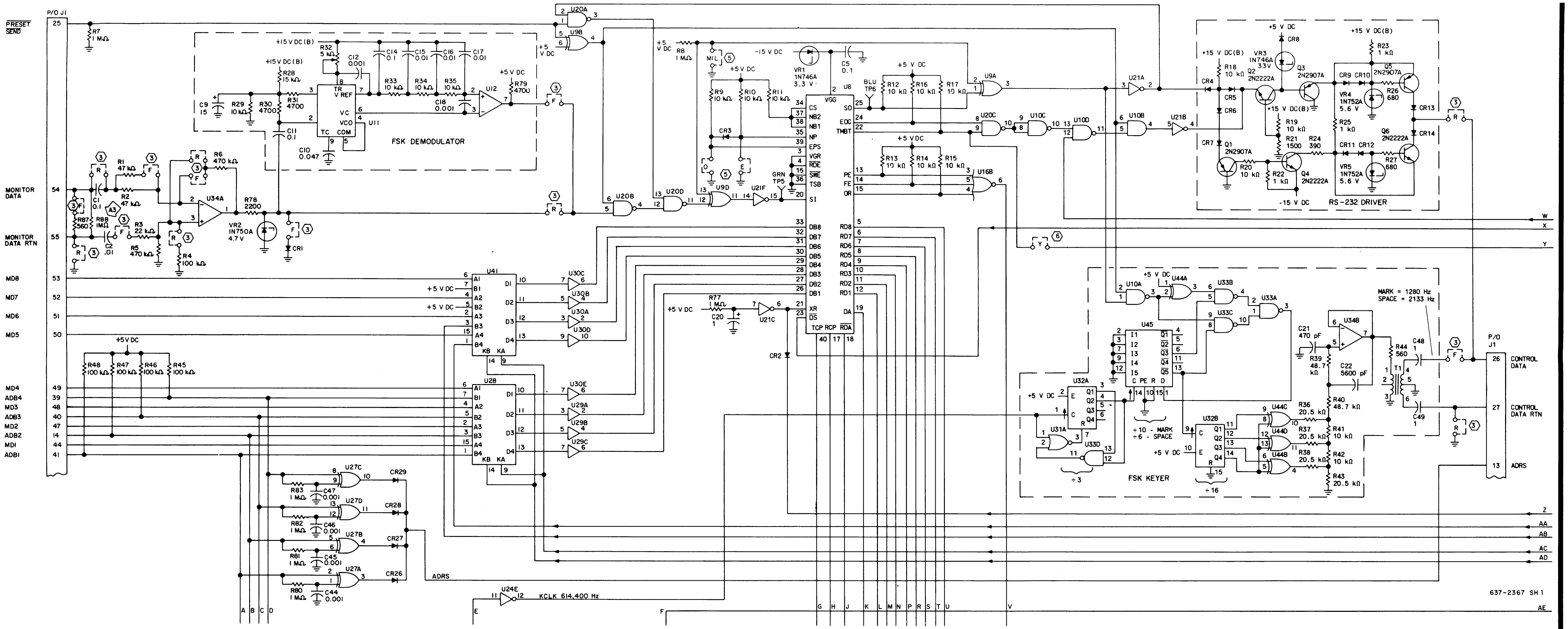
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
R80-R83	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R84	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R85,R86	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R87	RESISTOR, FXD, CMPSN, 560Ω, 10%, 1/4W	745-0740-000	
R88	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W (A3)	745-0857-000	
T1	TRANSFORMER, AF	677-0324-320	
TP1	JACK, TIP, BRN	360-0484-070	
TP2	JACK, TIP, RED	360-0484-020	
TP3	JACK, TIP, ORN	360-0484-050	
TP4	JACK, TIP, YEL	360-0484-060	
TP5	JACK, TIP, GRN	360-0484-040	
TP6	JACK, TIP, BLU	360-0484-080	
U1	INTEGRATED CKT, MC14025CP	351-8159-150	
U2	INTEGRATED CKT, F4029BPC	351-8159-250	
U3	INTEGRATED CKT, MC14001CP	351-8159-020	
U4	INTEGRATED CKT, F4030BPC	351-8159-190	
U5	INTEGRATED CKT, MC14011CP	351-8159-040	
U6	INTEGRATED CKT, F4021BPC	351-8159-230	
U7	INTEGRATED CKT, F4013BPC	351-8159-110	
U8	INTEGRATED CKT, AY5-1013A	351-8173-010	
U9	INTEGRATED CKT, F4030BPC	351-8159-190	
U10	INTEGRATED CKT, MC14011CP	351-8159-040	
U11	INTEGRATED CKT, LM565CN	351-1114-010	
U12	INTEGRATED CKT, LM311H	351-1094-060	
U13	INTEGRATED CKT, MC14025CP	351-8159-150	
U14	INTEGRATED CKT, F4049BPC	351-8159-210	
U15	INTEGRATED CKT, MC14011CP	351-8159-040	
U16	INTEGRATED CKT, MC14025CP	351-8159-150	
U17, U18	INTEGRATED CKT, F4013BPC	351-8159-110	
U19, U20	INTEGRATED CKT, MC14011CP	351-8159-040	
U21	INTEGRATED CKT, F4049BPC	351-8159-210	
U22	INTEGRATED CKT, F4040BPC	351-8159-240	
U23	INTEGRATED CKT, F4024BPC	351-8159-100	
U24	INTEGRATED CKT, F4049BPC	351-8159-210	
U25	INTEGRATED CKT, F4013BPC	351-8159-110	
U26	INTEGRATED CKT, MC14001CP	351-8159-020	
U27	INTEGRATED CKT, F4030BPC	351-8159-190	
U28	INTEGRATED CKT, F4019BPC	351-8159-080	
U29, U30	INTEGRATED CKT, F4050BPC	351-8159-220	
U31	INTEGRATED CKT, MC14001CP	351-8159-020	
U32	INTEGRATED CKT, F4520PC	351-8315-010	
U33	INTEGRATED CKT, MC14011CP	351-8159-040	
U34	INTEGRATED CKT, MC1458P1	351-1071-070	
U35, U36	INTEGRATED CKT, F4027BPC	351-8159-180	
U37	INTEGRATED CKT, F4013BPC	351-8159-110	
U38	MOS, ANLG MXR, F4052PC	351-8227-020	
U39	INTEGRATED CKT, MC14011CP	351-8159-040	
U40	INTEGRATED CKT, F4029BPC	351-8159-250	
U41	INTEGRATED CKT, F4019BPC	351-8159-080	
U42	INTEGRATED CKT, F4049BPC	351-8159-210	
U43	INTEGRATED CKT, MC14001CP	351-8159-020	
U44	INTEGRATED CKT, F4030BPC	351-8159-190	
U45	INTEGRATED CKT, MC14018 BCP	351-8253-010	
U46	INTEGRATED CKT, F4049BPC	351-8159-210	
U47	INTEGRATED CKT, F4013BPC	351-8159-110	
U48	MOS, ANLG MXR, F4052PC	351-8227-020	
U49	INTEGRATED CKT, F4027BPC	351-8159-180	
U50, U51	INTEGRATED CKT, F4013BPC	351-8159-110	
U52	INTEGRATED CKT, MC14011CP	351-8159-040	
VR1	SEMICOND DEVICE, 1N746A	353-2938-000	
VR2	SEMICOND DEVICE, 1N750A	353-2708-000	
VR3	SEMICOND DEVICE, 1N746A	353-2938-000	
VR4, VR5	SEMICOND DEVICE, 1N752A	353-2712-000	
Y1	XTAL UNIT, QTZ, 3.6864 MHz	289-7120-060	

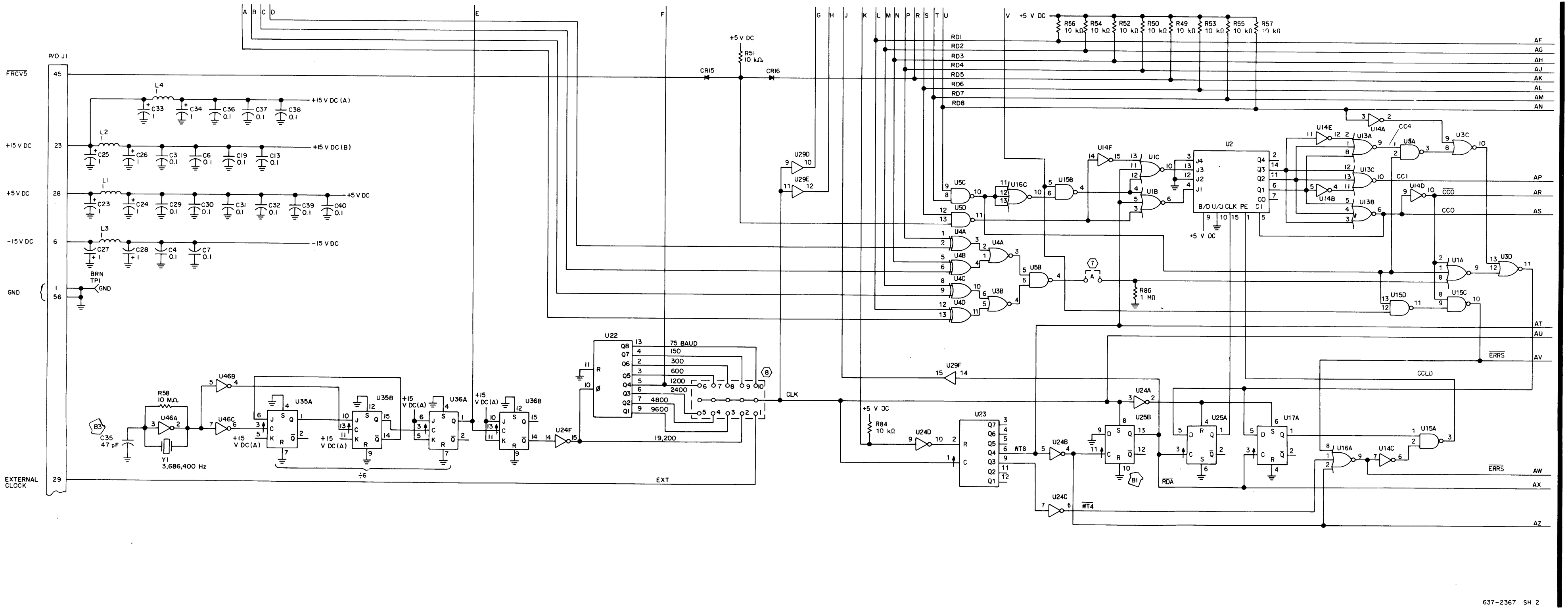
MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Removed C42, 200pF. Removed R60, 4700Ω.	REV B
A2	Added C42, 200pF. Added R60, 4700Ω.	REV C and above
A3	Added R88, 1 MΩ.	REV D
B1	Removed connection from U25B-12 to U17B-11 and U19C-9.	REV F and above
B2	Changed C42 from 200pF to 100pF.	REV G and above.
B3	Removed C35, 15pF from across R58. Added C35, 47pF.	REV J and above

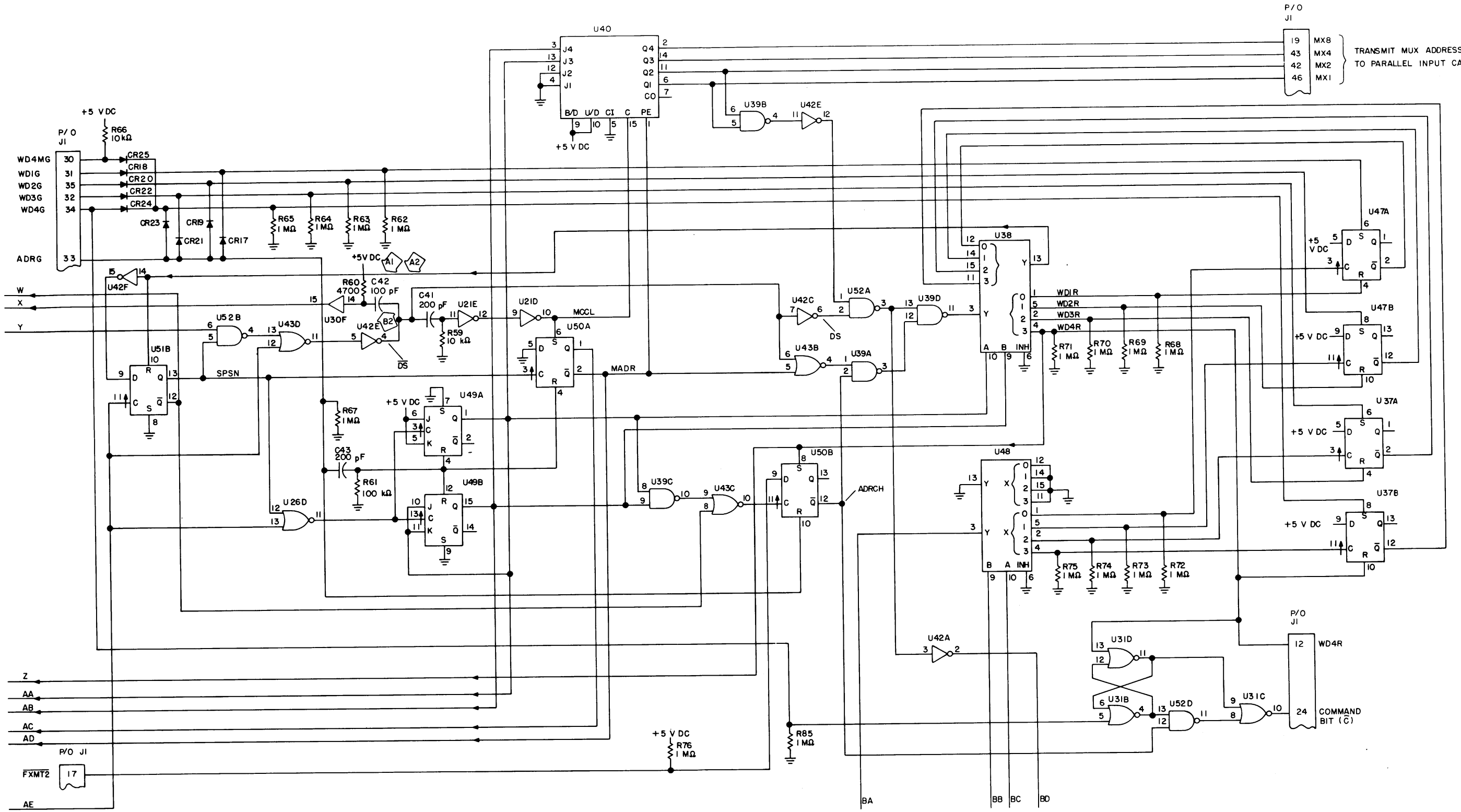
Serial Interface, Schematic Diagram
Figure 24 (Sheet 2)



Serial Interface, Schematic Diagram
Figure 2, (Sheet 3)



Serial Interface, Schematic Diagram
Figure 24 (Sheet 4)



NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, INDUCTANCE VALUES ARE IN MILLIHENRIES AND DIODES ARE TYPE IN4454.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. FOR FSK OPTION, JUMPERS LABELED "F" (QTY 7) ARE INSTALLED. FOR RS-232C OPTION, JUMPERS LABELED R (QTY 7) ARE INSTALLED.
4.
5. "E" STAPPED FOR EVEN PARITY, "O" STRAPPED FOR ODD PARITY, NEITHER STRAPPED FOR NO PARITY, "MIL" STRAPPED FOR MIL-STD-188C DATA LOGIC LEVELS, NOT STRAPPED WHEN USING FSK DATA OPTION, OR RS-232-C DATA LOGIC LEVELS.
6. PINS LABELED "Y" USED FOR TEST PURPOSE ONLY- JUMPER FOR NORMAL OPERATION.
7. PINS LABELED "A" JUMPERED TO ENABLE ADDRESS RECOGNITION. PINS LABELED "S" ARE USED TO HOLD SPARE JUMPERS.
8. BAUD RATE SELECT.

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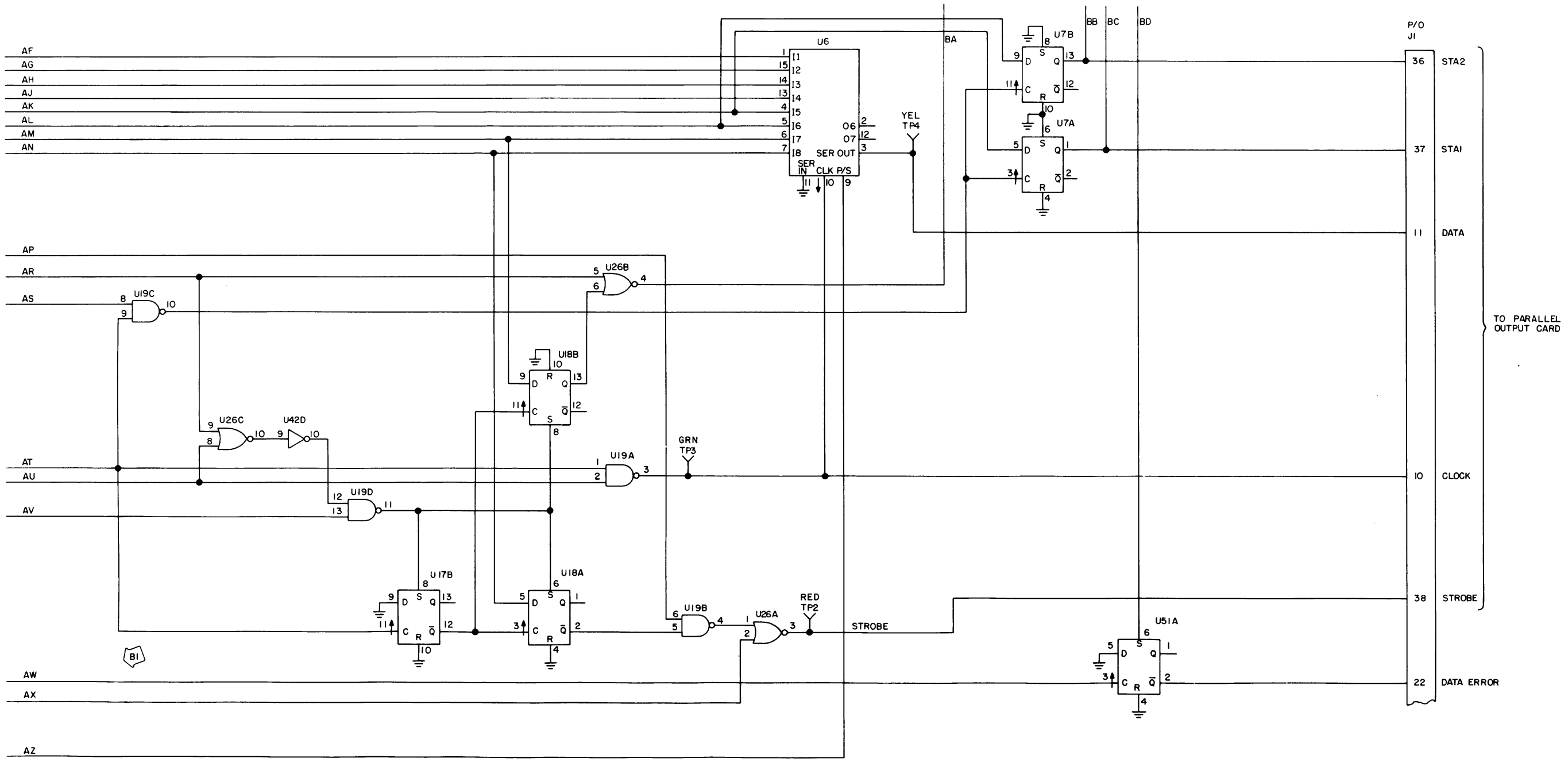
Serial Interface, Schematic Diagram
Figure 24 (Sheet 5)



MICROCIRCUIT POWER AND GROUND CONNECTIONS

U NO.	TYPE	POWER (V DC)				
		+15(A)	+15(B)	+5	GND	-15
U1,U13,U15	MC14025CP			14	7	
U2,U40	F4029BPC			16	8	
U3,U26,U31,U43	MC14001CP			14	7	
U4,U9,U27,U44	F4030BPC			14	7	
U5,U10,U15,U19, U20,U33,U39,U52	MC14011CP			14	7	
U6	F4021BPC			15	8	
U7,U17,U18,U25, U37,U47,U50,U51	F4013BPC			14	7	
U8	AY-5-1013A			1	3	
U11,	LM565CN		10		1	
U12	LH311H		8		4,1	
U14,U21,U24,U42	F4049BPC			1	8	
U46	F4049BPC	1			8	
U22	F4040BPC			16	8	
U23	F4024BPC			14	7	
U28,U41	F4019BPC			16	8	
U29,U30	F4050BPC			1	8	
U32	F4520PC			16	8	
U34	MC1458P1		8			4
U35,U36	F4027BPC	16			8	
U49	F4027BPC			16	8	
U38,U48	F4052PC			16	8 7	
U45	MC14018BCP			16	8	

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Serial Interface, Schematic Diagram
Figure 24 (Sheet 6)