



**Rockwell
International**

instructions

Collins Telecommunications Products Division

523-0767962-003211

3rd Edition, 1 January 1979

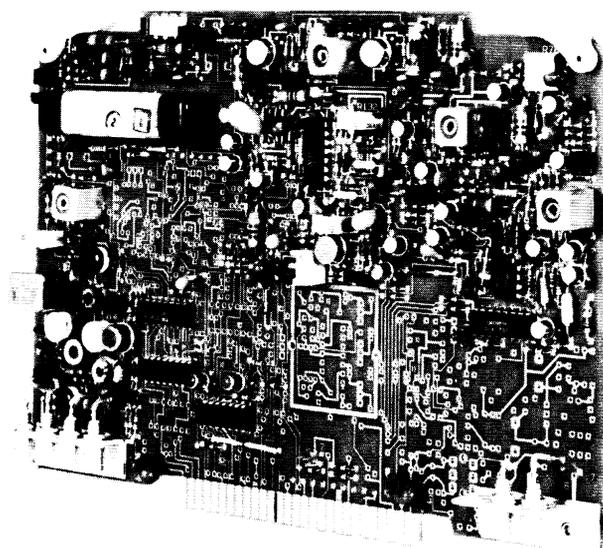
Channel A IF (637-2650-())

Printed in USA

1. DESCRIPTION

Channel A IF 637-2650-(), shown in figure 1, is a 2-layer planar card with 56-pin edge-on connector (2 layers, 28 pins each). The channel A if card has subminiature rf connectors for connecting to channel B if input (J1), 9.45-MHz receive input (J2), 9.9-MHz injection input (J3), channel B if output (J4), 450-kHz injection input (J5), and 450-kHz receive if input (J6).

The channel A if card consists of filter control, channel A if, channel A audio detector, and channel A AGC circuits.



TP5 - 2344 - 017

Channel A IF
Figure 1

The channel A if configuration differences are as follows:

- a. 637-2650-001, FL1 has 2.75-kHz bandwidth (250 to 3000 Hz, USB).
- b. 637-2650-002, FL1 has 3.05-kHz bandwidth (250 to 3300 Hz, USB).
- c. 637-2650-003, FL1 has 3.10-kHz bandwidth (300 to 3400 Hz, USB).
- d. 637-2650-004, reserved.
- e. 637-2650-005, FL1 has 5.80-kHz bandwidth (200 to 6000 Hz, USB).

2. PRINCIPLES OF OPERATION

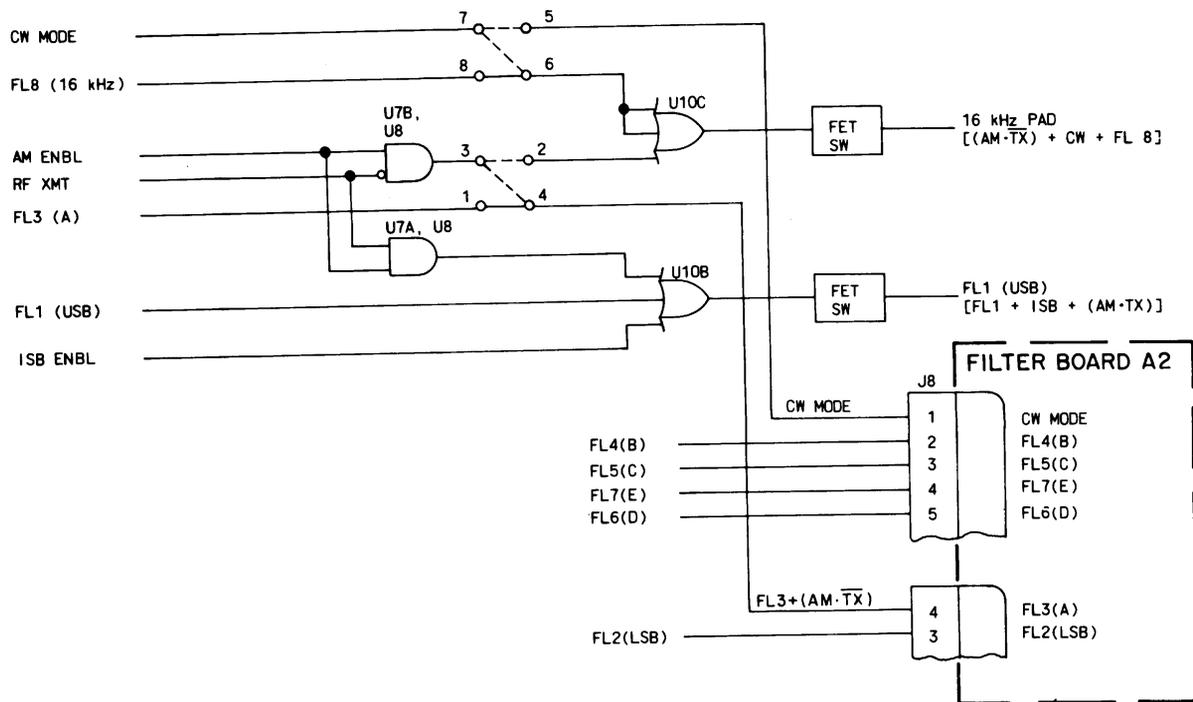
2.1 General

The channel A if receives the 9.45-MHz receive if input; mixes it with a 9.9-MHz fixed injection signal; filters the resulting 450-kHz receive if signal; and provides (1) 450-kHz receive if output, (2) AM audio output, (3) a product detected channel A SSB audio output, and (4) AGC control signals.

2.2 Bandpass Filter Control Circuits (Refer to figure 2.)

The channel A if provides filter selection for receive if signals. Filter selection is initiated by the mode control signal, bandwidth control signal, and/or rf transmit signal. This means only that these signals are applied to the channel A if card to initiate filter selection and does not reflect a mode of operation, selection of a bandwidth, or transmission of an rf signal.

NOTICE: This section replaces second edition dated 1 June 1978.



TP5-2279-013

Bandpass Filter Control Circuits
Figure 2

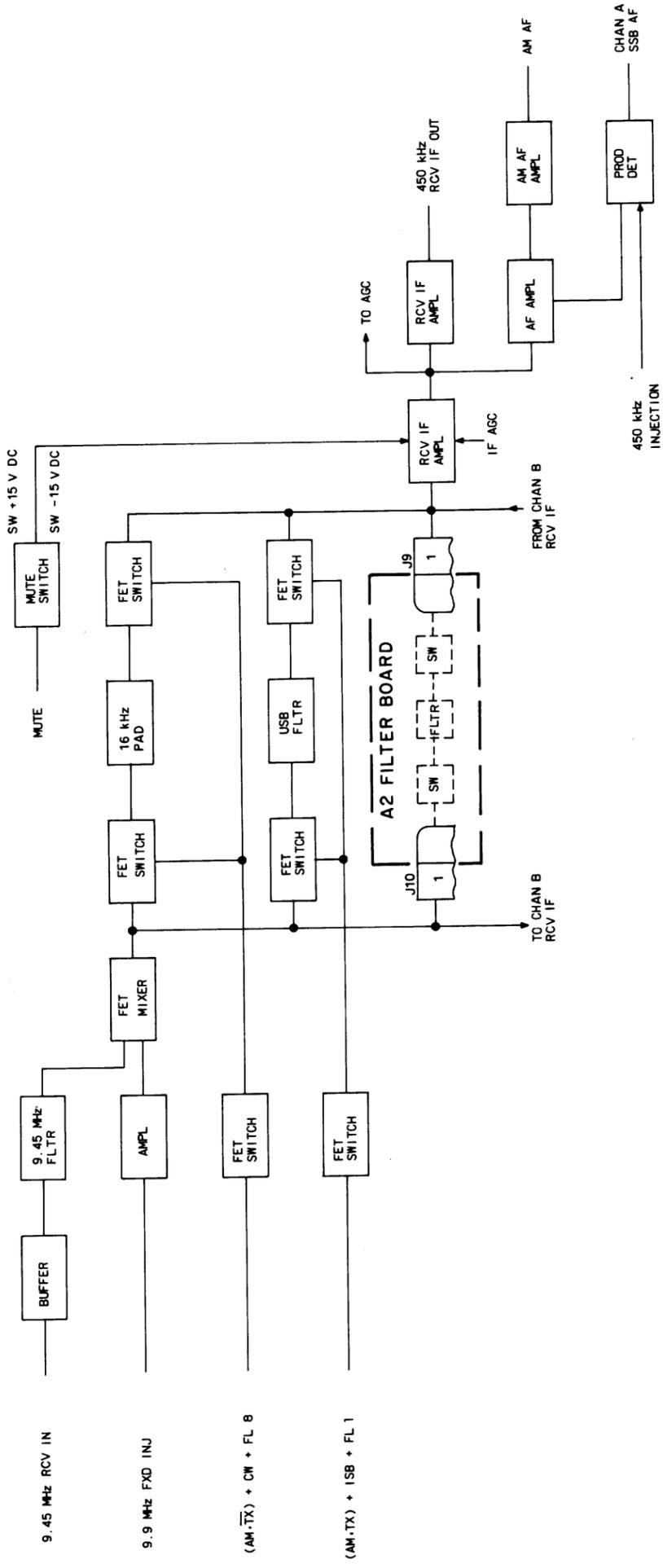
FL1 (USB) is selected when an FL1 (USB) enable signal, an ISB enable signal, and/or AM enable and rf transmit signals are applied to the channel A if card.

When strapped, 8-6 and 1-4: FL8 (16-kHz pad) is selected when an FL8 (16 kHz) enable signal is applied to the channel A if card. FL3 (A) is selected on A2 filter board when an FL3 (A) enable signal is applied to channel A if card (A2 is optional board).

FL2 (LSB), FL4 (B), FL5 (C), FL6 (D), and FL7 (E) are selected when the associated enable signal is applied to the channel A if card. These filters are mounted (if used) on the optional A2 filter board.

2.3 Channel A IF Circuits (Refer to figure 3.)

The channel A if card receives 9.45-MHz receive if through a buffer and a 9.45-MHz filter. The 9.45-MHz receive if is mixed in an FET mixer with a 9.9-MHz fixed injection signal and supplies a 450-kHz if frequency to the bandpass filter networks. Bandpass filters are located on the channel A if card, the A2 filter board, and/or an associated channel B if card. After mode/bandwidth selection, the 450-kHz if signal is supplied through the associated bandpass filter and amplified. The amplified 450 kHz is then



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Channel A IF Circuits
Figure 8

applied to AGC circuits, a receive if amplifier as an external 450-kHz receive if output, an audio amplifier to an AM audio detector, and/or the SSB audio product detector. The AM audio amplifier detects the audio and provides an AM audio output. The SSB product detector receives the receive if and a 450-kHz injection and supplies a product detected SSB audio output.

2.4 AGC Circuits (Refer to figure 4.)

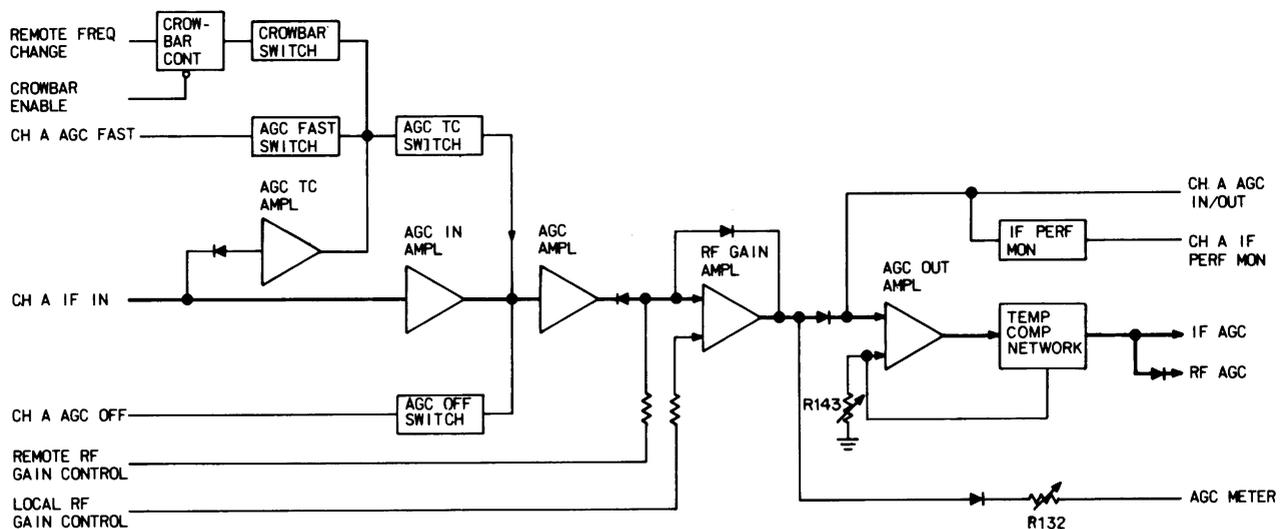
Channel A if is received by the AGC input amplifier. The AGC input amplifier and associated AGC time constant switches develop the AGC level and decay time to be used by the receiver. The AGC level is amplified and applied through rf gain amplifier and supplied to the if performance monitor and AGC output amplifier. The if AGC and rf AGC signals are developed and supplied to the associated attenuator circuits. With the AGC control in the SLOW position, only the AGC time constant amplifier and AGC time constant switch are enabled and establish a 1.0-second AGC decay time. (The AGC to amplifier and AGC to switch are enabled for all AGC functions.)

With the AGC control in the FAST position, the AGC fast switch is enabled reducing the time constant of the AGC circuits and establishing a 0.1-second AGC decay time. With the AGC control in the OFF position, the output of the AGC input amplifier is disabled and removed from the input of the AGC amplifier.

With the receiver in remote control and a crowbar enable applied, a remote frequency change enables the crowbar switch and reduces the AGC time constant and establishes the AGC decay time at about 2 milliseconds. The crowbar function is used for fast frequency hopping or scanning operation under processor control.

The gain of the rf gain amplifier is controlled by a local rf gain control signal. The dc voltage level applied to the noninverting input of the rf gain amplifier establishes its gain. The remote rf gain control signal establishes the minimum gain output of the rf gain amplifier.

R132 sets the level for the correct reading of the AGC meter (0 dB at 1- μ V input to 100 dB above the 1- μ V input).



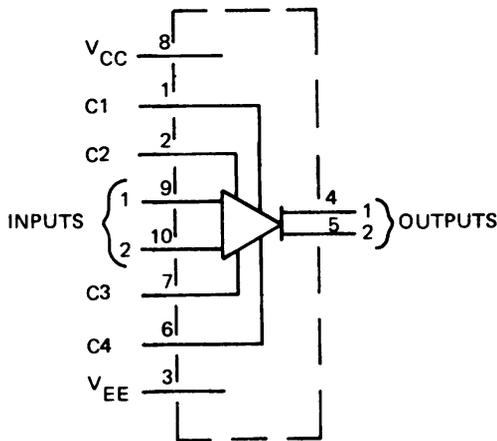
TP5-2281-013

AGC Circuits
Figure 4

From the rf gain amplifier, the AGC output is supplied to channel A AGC output for use by other cards and to the channel A if performance monitor for channel A AGC indications. The rf gain amplifier output is supplied to AGC output amplifier that develops the if/rf AGC outputs. R143 and temperature compensating network are used to keep the if/rf AGC outputs constant throughout the temperature range.

2.5 Differential Output Operational Amplifier 351-1050-030 (Refer to figure 5.)

The 351-1050-030 is a wide-band general-purpose operational amplifier that features both differential inputs and outputs. Open loop gain is adjustable with external feedback components.



2.6 Quad Operational Amplifier 351-1141-030 (Refer to figure 6.)

The 351-1141-030 consists of four independent, high gain, internally frequency-compensated operational amplifiers that are designed to operate from a single power supply over a wide range of voltages. Common applications include transducer amplifiers, dc gain blocks, and all conventional operational amplifier circuits.

2.7 Dual Operational Amplifier 351-1071-070 (Refer to figure 7.)

The 351-1071-070 consists of two operational amplifiers in one package designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components.

CHARACTERISTICS

SUPPLY VOLTAGE: V_{CC} +8 V DC MAX.,
 V_{EE} -8 V DC MAX.

INPUT DIFF VOLTAGE: ± 8 V DC MAX.

INPUT COMMON MODE VOLTAGE:
 ± 3.0 V PEAK

INPUT RESISTANCE: 2.0 M OHM TYPICAL

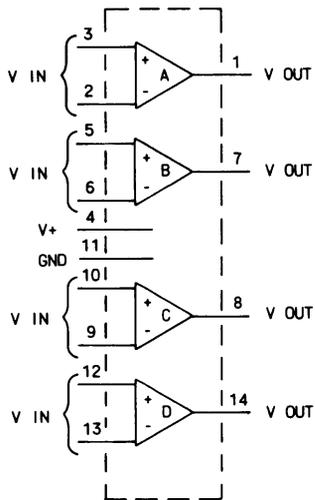
OUTPUT RESISTANCE: 50 OHM TYPICAL

OPEN LOOP GAIN: SINGLE ENDED -
750 V/V MIN, 1500 V/V TYPICAL;
DIFFERENTIAL - 1500 V/V MIN.,
3000 V/V TYPICAL

BANDWIDTH: OPEN LOOP - 2.0 MHz TYPICAL;
CLOSED LOOP - 10.0 MHz TYPICAL

TP5-2282-011

Differential Output Operational Amplifier 351-1050-030
Figure 5



CHARACTERISTICS

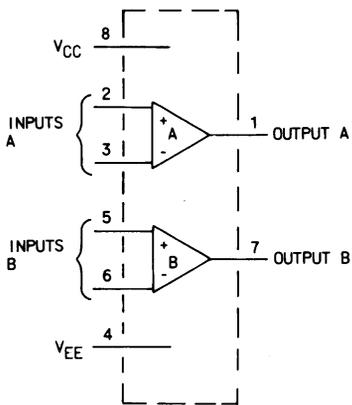
SUPPLY VOLTAGE (V+): 32 V DC MAX
 INPUT DIFF VOLTAGE: 32 V DC MAX
 INPUT COMMON MODE VOLTAGE: V+ (-1.5 V DC)
 OUTPUT SHORT CIRCUIT DURATION:
 CONTINUOUS (1)
 VOLTAGE GAIN: 25 MIN

NOTE:

(1) SUPPLY VOLTAGE EQUAL TO OR LESS THAN 15 V.

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Quad Operational Amplifier 351-1141-030
 Figure 6



CHARACTERISTICS

SUPPLY VOLTAGE: V_{CC} +18 V DC MAX
 V_{EE} -18 V DC MAX
 INPUT DIFF VOLTAGE: ±30 V MAX
 INPUT COMMON MODE VOLTAGE:
 ±15 V MAX (1)
 OUTPUT SHORT CIRCUIT DURATION:
 CONTINUOUS (2)
 INPUT RESISTANCE: 300 kΩ MIN, 2.0 MΩ MAX
 OUTPUT RESISTANCE: 75Ω TYPICAL
 VOLTAGE GAIN: 15 MIN

NOTES:

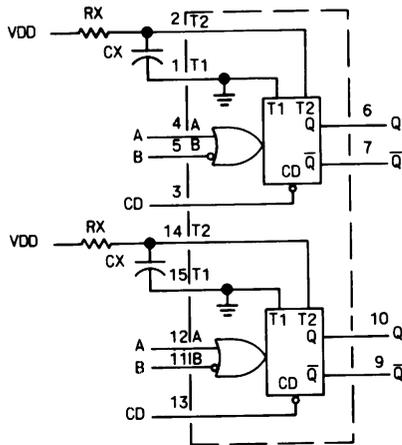
(1) FOR SUPPLY VOLTAGE LESS THAN ±15.0 V, MAX INPUT VOLTAGE EQUAL TO SUPPLY VOLTAGE.
 (2) SUPPLY VOLTAGE EQUAL TO OR LESS THAN 15 V.

TP5-2285-013

Dual Operational Amplifier 351-1070-070
 Figure 7

2.8 Dual Monostable Multivibrator 351-8278-010
(Refer to figure 8.)

The 351-8278-010 is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X .



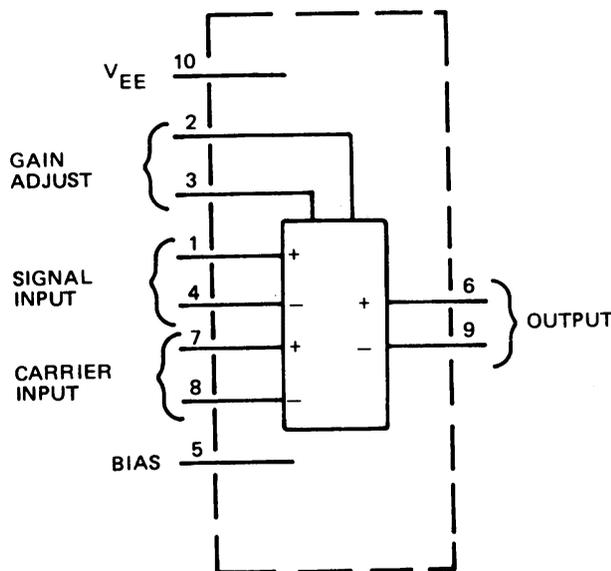
NOTE:
RX AND CX ARE EXTERNAL COMPONENTS.

CHARACTERISTICS:
SUPPLY VOLTAGE (VDD): -0.5 TO +18 V DC.
INPUT VOLTAGE: EQUAL TO VDD, MAX.

CHARACTERISTIC	VDD		
	5.0 V DC	10.0 V DC	15.0 V DC
OUTPUT VOLTAGE	"0" 0.05 V DC MAX. "1" 4.95 V DC MIN.	0.05 V DC MAX. 9.95 V DC MIN.	0.05 V DC MAX. 14.95 V DC MIN.
INPUT VOLTAGE	"0" 2.25 V DC MAX. "1" 2.75 V DC MIN.	4.50 V DC MAX. 5.50 V DC MIN.	6.75 V DC MAX. 8.25 V DC MIN.
EXTERNAL TIMING	RX 1000 Ω MIN. CX NO LIMITS	1000 Ω MIN. NO LIMITS	1000 Ω MIN. NO LIMITS

TP5-2290-013

Dual Monostable Multivibrator 351-8278-010
Figure 8



CHARACTERISTICS

APPLIED VOLTAGE: 30 V DC MAX PIN-TO-IN.
DIFFERENTIAL INPUT VOLTAGE: ± 5 V DC MAX
CARRIER SUPPRESSION: 65 dB TYPICAL AT 0.5 MHz; 50 dB TYPICAL AT 10 MHz.
TRANSADMITTANCE BANDWIDTH:
CARRIER INPUT-300 MHz TYPICAL;
SIGNAL INPUT-80 MHz TYPICAL
SINGLE-ENDED INPUT RESISTANCE (SIGNAL INPUT): 200 k OHM TYPICAL (AT 5.0 MHz)
SINGLE-ENDED INPUT RESISTANCE (SIGNAL INPUT): 40 k OHM TYPICAL (AT 10 MHz)
DIFFERENTIAL OUTPUT VOLTAGE SWING: 8.0 V P-P TYPICAL

TP5-2291-011

Balanced Modulator-Demodulator 351-0043-020
Figure 9

3. TESTING/TROUBLESHOOTING PROCEDURES

permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the channel A if card are listed in the maintenance section of this instruction book.

Note

In emergencies, Channel A IF 637-2650-() can be replaced by Channel A IF 635-0819-(). In this type of repair, use the test procedures given in table 1 to test Channel A IF 635-0819-().

3.2 Testing

The test procedures in table 1 check total performance of the channel A if card. These test procedures

Table 1. Channel A IF, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of unit containing the channel A if that is to be tested. b. Remove channel A if. Install it on an extender card and place it in the unit. c. Set unit LINE SELECTOR switch to 115 V. d. Connect unit to 115-V ac power source and set power on. e. Measure dc voltages between the following pins and ground (TP1, brown): P1-23 and P1-51 P1-27 P1-6	+15 ±1.0 V dc +5 ±0.5 V dc -15 ±1.0 V dc	Check associated power supply.
2. FL1 (USB) filter enable	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to A. b. Measure dc voltage at TP2 to ground. c. Set front panel BANDWIDTH switch to USB. d. Measure dc voltage at TP2 to ground. e. Set front panel MODE switch to ISB. f. Measure dc voltage at TP2 to ground. g. Set front panel MODE switch to AM and BANDWIDTH switch to A. h. Measure dc voltage at TP2 to ground. i. Connect a 4700-Ω resistor between P1-41 and +5 V dc. j. Measure dc voltage at TP2 to ground. k. Set front panel MODE switch to SSB/CW. l. Measure dc voltage at TP2 to ground. m. Remove 4700-Ω resistor from P1-41 and +5 V dc. FL1 (USB) FILTER ENABLE TESTING COMPLETE	-9.5 ±1.0 V dc NMT 0.5 V dc NMT 0.5 V dc -9.5 ±1.0 V dc NMT 0.5 V dc -9.5 ±1.0 V dc	Proceed to step n. Proceed to step o. Proceed to step p. Proceed to step q. Proceed to step r. Proceed to step s.
(Cont)			

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
<p>2. (Cont)</p> <p>(Cont)</p>	<p>TROUBLESHOOTING</p> <p>n. Measure dc voltages at the following pins:</p> <p style="padding-left: 40px;">P1-14</p> <p style="padding-left: 40px;">P1-35</p> <p style="padding-left: 40px;">P1-41</p> <p style="padding-left: 40px;">P1-44</p> <p>o. Measure dc voltage at P1-14.</p> <p>p. Measure dc voltage at P1-44.</p> <p>q. Measure dc voltages at the following pins:</p> <p style="padding-left: 40px;">P1-14</p> <p style="padding-left: 40px;">P1-35</p> <p style="padding-left: 40px;">P1-41</p> <p style="padding-left: 40px;">P1-45</p> <p>r. Measure dc voltage at P1-35.</p>	<p>NMT 0.5 V dc</p> <p>NMT 0.5 V dc</p> <p>NMT 0.5 V dc</p> <p>NMT 0.5 V dc</p> <p>If voltages in step n are all normal, check U7, U8, U10, Q32, and associated circuit.</p> <p>NLT +3.0 V dc. Check U10, Q32, and associated circuit.</p> <p>NLT +3.0 V dc. Check U10, Q32, and associated circuit.</p> <p>NMT 0.5 V dc</p> <p>NLT +3.0 V dc</p> <p>NMT 0.5 V dc</p> <p>NMT 0.5 V dc</p> <p>If voltages in step q are all normal, check U7, U8, U10, Q32, and associated circuit.</p> <p>NLT +3.0 V dc. If voltage is normal, check U7, U8, U10, Q32, and associated circuit.</p>	<p>Check FL1 (USB) input circuit.</p> <p>Check AM enable input circuit.</p> <p>Check rf transmit input circuit.</p> <p>Check ISB enable input circuit.</p> <p>Check FL1 (USB) input circuit.</p> <p>Check ISB enable input circuit.</p> <p>Check FL1 (USB) input circuit.</p> <p>Check AM enable input circuit.</p> <p>Check rf transmit input circuit.</p> <p>Check ISB enable input circuit.</p> <p>Check AM enable input circuit.</p>

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	<p>TROUBLESHOOTING</p> <p>k. Measure dc voltage at P1-15.</p> <p>l. Measure dc voltage at P1-15.</p> <p>m. Measure dc voltage at P1-35.</p> <p>n. Measure dc voltage at P1-35.</p> <p>o. Measure dc voltage at P1-41.</p>	<p>NMT 0.5 V dc. Check that a strap is installed from 1 to 4, and that no other strap is attached to 4.</p> <p>NLT +3.0 V dc. Check that a strap is installed from 1 to 4.</p> <p>NMT 0.5 V dc. Check U7, U8, and associated circuit. Check that a strap is installed from 3 to 4.</p> <p>NLT +3.0 V dc. Proceed to step o.</p> <p>NMT 0.5 V dc. Check U7, U8, and associated circuit. Check that a strap is installed from 3 to 4, and that no other strap is attached to 4.</p>	<p>Check FL3 (A) input circuit.</p> <p>Check FL3 (A) input circuit.</p> <p>Check AM enable input circuit.</p> <p>Check AM enable input circuit.</p> <p>Check rf transmit input circuit.</p>
4. FL4 (B), FL5 (C), FL6 (D), and filter enable FL (E) (Cont)	<p>a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to 16.</p> <p>b. Measure dc voltage at each of the following pins:</p> <p>J8-2</p> <p>J8-3</p> <p>J8-5</p> <p>J8-4</p> <p>c. Set BANDWIDTH switch to B.</p> <p>d. Measure dc voltage at J8-2.</p> <p>e. Set BANDWIDTH switch to C.</p> <p>f. Measure dc voltage at J8-3.</p> <p>g. Set BANDWIDTH switch to D.</p> <p>h. Measure dc voltage at J8-5.</p>	<p>NMT 0.5 V dc</p> <p>NMT 0.5 V dc</p> <p>NMT 0.5 V dc</p> <p>NMT 0.5 V dc</p> <p>NLT +3.0 V dc</p> <p>NLT +3.0 V dc</p> <p>NLT +3.0 V dc</p>	<p>Proceed to step k.</p> <p>Proceed to step l.</p> <p>Proceed to step m.</p> <p>Proceed to step n.</p>

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	<p>d. Measure dc voltage at TP4 to ground.</p> <p style="text-align: center;">Note</p> <p>With channel A if strapped 6-7, perform steps e thru i.</p> <p>e. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to B.</p> <p>f. Measure dc voltage at TP4 to ground.</p> <p>g. Apply +5.0 V dc at P1-38.</p> <p>h. Measure dc voltage at TP4 to ground.</p> <p>i. Remove +5.0 V dc from P1-38.</p> <p style="text-align: center;">Note</p> <p>With channel A if strapped 2-3, perform steps j thru p.</p> <p>j. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to B.</p> <p>k. Measure dc voltage at TP4 to ground.</p> <p>l. Set front panel MODE switch to AM.</p> <p>m. Measure dc voltage at TP4 to ground.</p> <p>n. Apply +5.0 V dc at P1-41.</p> <p>o. Measure dc voltage at TP4 to ground.</p> <p>p. Remove +5.0 V dc from P1-41.</p> <p>FL8 (16 kHz) FILTER ENABLE TESTING COMPLETE</p>	<p>NMT 0.5 V dc</p> <p>-9.5 ±1.0 V dc</p> <p>NMT 0.5 V dc</p> <p>-9.5 ±1.0 V dc</p> <p>NMT 0.5 V dc</p> <p>-9.5 ±1.0 V dc.</p>	<p>Proceed to step r.</p> <p>Proceed to step s.</p> <p>Check U10, Q33, and associated circuit. Check that a strap is installed from 6 to 7.</p> <p>Proceed to step t.</p> <p>Proceed to step u.</p> <p>Check U7, U8, U10, Q33, and associated circuit.</p>
(Cont)	<p style="text-align: center;">TROUBLESHOOTING</p> <p>q. Measure dc voltage at P1-46.</p>	<p>NMT 0.5 V dc. Check U10, Q33, and associated circuit. Check that a strap is installed from 6 to 8 and that no other strap is attached to 6.</p>	<p>Check FL8 (16 kHz) input circuit.</p>

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
8. (Cont)	<ul style="list-style-type: none"> a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB. b. Set AGC switch to OFF. c. Set receive input at J2 for 9.4483 MHz. d. Using an rf voltmeter (with high impedance probe), measure rf voltage at J4. Adjust receive input level and frequency for a 70-mV peak reading at J4. e. Adjust input frequency down until rf voltage at J4 is 3 dB below level of step d. Note input frequency. f. Adjust input frequency up until rf voltage at J4 is 3 dB below level of step d. Note input frequency. 	<p>Reference</p> <p>NMT 9.447 000 MHz</p> <p>NLT 9.449 750 MHz</p>	<p>Check FL1, Q4, Q8, and associated circuit.</p> <p>Check FL1, Q4, Q8, and associated circuit.</p>
8A. 3.05-kHz USB filter measurement	<p style="text-align: center;">Note</p> <p>This test applies only to 3.05-kHz USB filter (526-9980-010).</p> <ul style="list-style-type: none"> a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB. b. Set AGC switch to OFF. c. Set receive input at J2 for 9.4482 MHz. d. Using an rf voltmeter (with high impedance probe), measure rf voltage at J4. Adjust receive input level and frequency for a 70-mV peak reading at J4. e. Adjust input frequency down until rf voltage at J4 is 3 dB below level of step d. Note input frequency. f. Adjust input frequency up until rf voltage at J4 is 3 dB below level of step d. Note input frequency. 	<p>Reference</p> <p>NMT 9.446 700 MHz</p> <p>NLT 9.449 750 MHz</p>	<p>Check FL1, Q4, Q8, and associated circuit.</p> <p>Check FL1, Q4, Q8, and associated circuit.</p>
8B. 3.10-kHz USB filter measurement (Cont)	<p style="text-align: center;">Note</p> <p>This test applies only to 3.10-kHz USB filter (526-9985-010).</p> <ul style="list-style-type: none"> a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB. b. Set AGC switch to OFF. c. Set receive input at J2 for 9.4482 MHz. 		

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
8B. (Cont)	<p>d. Using an rf voltmeter (with high impedance probe), measure rf voltage at J4. Adjust receive input level and frequency for a 70-mV peak reading at J4.</p> <p>e. Adjust input frequency down until rf voltage at J4 is 3 dB below level of step d. Note input frequency.</p> <p>f. Adjust input frequency up until rf voltage at J4 is 3 dB below level of step d. Note input frequency.</p>	<p>Reference</p> <p>NMT 9.446 600 MHz</p> <p>NLT 9.449 700 MHz</p>	<p>Check FL1, Q4, Q8, and associated circuit.</p> <p>Check FL1, Q4, Q8, and associated circuit.</p>
8C. 5.80-kHz USB filter measurement	<p style="text-align: center;">Note</p> <p>This test applies only to 5.80-kHz USB filter (526-9976-010).</p> <p>a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.</p> <p>b. Set AGC switch to OFF.</p> <p>c. Set receive input at J2 for 9.4459 MHz.</p> <p>d. Using an rf voltmeter (with high impedance probe), measure rf voltage at J4. Adjust receive input level and frequency for a 70-mV peak reading at J4.</p> <p>e. Adjust input frequency down until rf voltage at J4 is 3 dB below level of step d. Note input frequency.</p> <p>f. Adjust input frequency up until rf voltage at J4 is 3 dB below level of step d. Note input frequency.</p>	<p>Reference</p> <p>NMT 9.444 000 MHz</p> <p>NLT 9.449 800 MHz</p>	<p>Check FL1, Q4, Q8, and associated circuit.</p> <p>Check FL1, Q4, Q8, and associated circuit.</p>
9. AGC attack and decay times (Cont)	<p>a. Set receive input at J2 to 9.4483 MHz at 1 mV at output of switching device. Set the switching device for 0.25 s on and 2.5 s off.</p> <p style="text-align: center;">Note</p> <p>If a switching device is not available, one may be fabricated using figure 10.</p> <p>b. Set front panel AGC switch to FAST.</p> <p>c. Using an oscilloscope, measure AGC attack time at Q18-C.</p>	<p>NMT 5 ms</p>	

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
9. (Cont)	and the point when the rf envelope reaches 70% of the final value. f. Repeat steps d and e with the front panel AGC switch at SLOW.	1 to 2 s	Check U3 and associated circuits.
10. 450-kHz injection frequency suppression	a. Set receive input at J2 to 9.4483 MHz at 1000 μ V. b. Set AGC switch to FAST. c. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB. d. Using a spectrum analyzer, measure the desired if out at J6 (CH A IF jack on rear panel). e. Measure the 450-kHz injection frequency leakage at the receive if out jack J6 (CH A IF jack on rear panel).	Note level. NLT 40 dB down from receive if above <div style="border: 1px solid black; padding: 2px; width: fit-content; margin: 5px auto;">Note</div> It may be necessary to remove the receive input to locate the 450-kHz leakage. Measure if with the receiver input applied.	Check U6, Q2, and associated circuit.
11. Receive audio distortion	a. Set receive input at J2 to 9.4483 MHz at 500 μ V. b. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB. c. Using an audio distortion analyzer, measure the audio distortion at RCV AF 600 Ω - A on rear panel (TB1-1, -3).	NMT 0.5%	Check U14, U1, U2, Q14, Q17, Q18, and associated circuits.
12. AGC range (Cont)	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB. b. Set AGC switch to FAST. c. Set receive input at J2 to 9.4483 MHz at 0 μ V. d. Connect dvm to P1-21. e. Increase receive input until dvm just begins to increase from 70 mV dc. f. Using an rf voltmeter, note rf level at J6 (CH A IF jack on rear panel).	Note input level at this point. (Nominally 5 μ V rms) Reference	

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
12. (Cont)	g. Increase receive input 80 dB higher than the input level noted in step e. h. Note the rf level at J6 (CH A IF jack on rear panel) and that no sign of an overload exists on Q18-C.	NMT 6 dB above that noted in step f. No overload on Q18-C.	Check U1, U2, and associated circuits.
13. Remote rf gain	<div style="border: 1px solid black; padding: 2px; width: fit-content; margin: 0 auto 10px auto;">Note</div> This test applies only to unit with a remote control connected. a. Set receive input at J2 to 9.4483 MHz at 5 μ V. b. Set front panel CONT switch to REM. c. Set remote control MODE switch to SSB/CW and BANDWIDTH switch to USB. d. Set remote control AGC switch off. e. Adjust remote control RF GAIN control full counterclockwise. Increase receive input at J2 until if output level equals reference of step c. f. Set receive input for 60 dB above 5- μ V input. Adjust remote control RF GAIN control until if output level equals reference of step c. g. Note the input at P1-11. h. Set front panel CONT switch to LCL.	Reference if output level at J6 (CH A IF jack on rear panel). Total attenuation over RF GAIN control range 80 dB minimum. -5.0 \pm 0.1 V dc	Check U3 and associated circuits. Same as step c.
14. Local rf gain	a. Set receive input at J2 to 9.4483 MHz at 5 μ V. b. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB. c. Set front panel AGC switch to OFF. d. Adjust front panel RF GAIN control full counterclockwise. Increase receive input at J2 until if output level equals reference of step b. e. Set receive input for 60 dB above 5- μ V input. Adjust RF GAIN control until if output level equals reference of step b. f. Note the input at P1-39.	Reference if output level at J6 (CH A IF jack on rear panel). Total attenuation over RF GAIN control range 80 dB minimum. +2.8 \pm 0.3 V dc	Check U3 and associated circuits. Same as step d.

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

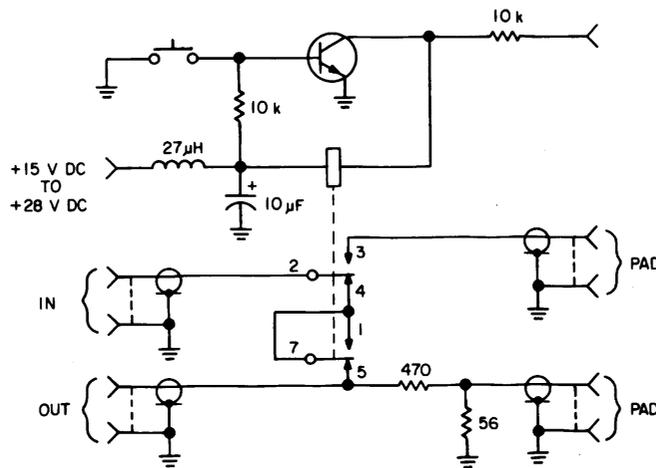
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
15. AGC in/out	<ul style="list-style-type: none"> a. Set the front panel MODE switch to SSB/CW and BANDWIDTH switch to USB. b. Set front panel AGC switch to FAST. c. Set receive input at J2 to 9.4483 MHz at 5 μV. d. Check the AGC in/out voltage at P1-21 with this input applied. e. Increase the receive input at J2 by 80 dB. f. Check the AGC in/out voltage at P1-21 with this input applied. 	<p>\cong 70 mV dc</p> <p>7.8 \pm0.8 V dc</p>	<p>Check U3B and associated circuits.</p> <p>Same as step d</p>
16. RF AGC	<ul style="list-style-type: none"> a. Set the front panel MODE switch to SSB/CW and BANDWIDTH switch to USB. b. Set front panel AGC switch to FAST. c. Set receive input at J2 to 9.4483 MHz at 5 μV. d. Using a dvm, monitor the rf AGC voltage at P1-18. e. Adjust front panel RF GAIN control for 0 V dc at P1-18. f. Note the rf AGC voltage while slowly increasing the receive input to 80 dB above level in step c. 	<p>Reference</p> <p>Rf AGC increases at a constant rate from 0 to 3 V dc. (60-dB point = NLT 3.0 V dc)</p>	<p>Check Q19, U3A, U3B, and associated circuits.</p>
17. Mute	<ul style="list-style-type: none"> a. Set the front panel MODE switch to SSB/CW and BANDWIDTH switch to USB. b. Set receive input at J2 to 9.4483 MHz at 50 μV. c. Using an rf voltmeter, monitor the if output at J6 (CH A IF jack on rear panel). d. Apply a ground at P1-13. e. Remove P1-13 ground. 	<p>Output signal is present.</p> <p>Output signal is muted.</p> <p>Output signal is restored.</p>	<p>Check U1, U2, and associated circuits.</p> <p>Check Q10 thru Q13 and associated circuits.</p>

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
18. Performance monitor	<p>a. Set the front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.</p> <p>b. Set receive input at J2 to 9.4483 MHz at 50 μV.</p> <p>c. Using a dvm, measure the dc voltage at P1-2.</p> <p>d. Remove receive input and measure the dc voltage at P1-2.</p>	<p>0.5 \pm0.5 V dc</p> <p>+4.5 \pm0.5 V dc</p>	<p>Check Q25 and associated circuit.</p> <p>Same as step c.</p>
19. AGC meter voltage	<p>a. Set the front panel MODE switch to SSB/CW and BANDWIDTH switch to USB.</p> <p>b. Set receive input at J2 to 9.4483 MHz at 5 μV.</p> <p>c. Using a dvm, measure the dc voltage at P1-12.</p> <p>d. Increase the receive input voltage and verify that the dc voltage at P1-12 increases.</p>	<p>0.5 \pm0.5 V dc (with front panel METER switch at any position other than RCV SIG)</p> <p>Increased voltage</p>	<p>Check U3A, U3B, and associated circuits.</p>
20. Crowbar enable	<p>a. Set the front panel CONT switch to REM.</p> <p>b. Apply +5 V dc to P1-37.</p> <p>c. Using an oscilloscope, monitor the waveform at U5-7.</p> <p>d. Note dc level and duration of U5-7 pulse while slowly changing the remote control frequency settings.</p> <p>e. Using an oscilloscope, monitor the waveform at P1-18.</p> <p>f. Remove +5 V dc from P1-37.</p> <p>g. Set the front panel CONT switch to LCL.</p>	<p>NLT +3.0 V dc</p> <p>0.5 \pm0.5 V dc for 20 \pm10 ms between each frequency change</p> <p>During the logic 0 pulse, waveform at P1-18 shall be 0.5 \pm0.5 V dc.</p>	<p>Check U5 and associated circuits.</p> <p>Same as step b.</p> <p>Check Q29 and associated circuit.</p>
21. AM audio	<p>a. Set front panel MODE switch to AM and BANDWIDTH switch to 16.</p> <p>b. Set receive input at J2 to 9.4500 MHz at 500 μV, AM modulated at 1000 Hz and 50%.</p> <p>c. Using an audio distortion analyzer, measure the audio signal level at P1-8 (A6TP2) and the audio distortion at RCV AF 600 Ω-A on rear panel (TB1-1, -3).</p>	<p>Output: 10 \pm2 mV. Distortion NMT 3.0%.</p>	<p>Check Q21 and associated circuits.</p>

Table 1. Channel A IF, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
22. Sensitivity	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB. b. Set AGC switch to OFF. c. Using an audio voltmeter, monitor the audio at P1-34 (A6TP2) (with no receive input). d. Set receive input at J2 to 9.4483 MHz. e. Adjust receive input for +10 dB (s+n)/n at P1-34 (A6TP2). f. Note the receive input level.	Reference NMT 1 μ V rms (into 50- Ω , 2- μ V rms open circuit)	Check U1, U2, and associated circuits.
23. If output	a. Set front panel MODE switch to SSB/CW and BANDWIDTH switch to USB. b. Set receive input at J2 to 9.4483 MHz at 15 μ V. c. Set front panel AGC switch to FAST. d. Using an rf voltmeter, measure the receive if output at J6 (CH A IF jack on rear panel).	27 \pm 10 mV rms	Check Q15, Q16, and associated circuits.



TPA -1345 -013

AGC Switching Device
Figure 10

4. ALIGNMENT/ADJUSTMENT

4.1 Input Strapping

Inputs to FL3 and FL8 are strapped as required for special applications. FL3(A) through FL7(E) band-pass filters are located on piggyback filter board A8A2 if used. Refer to table 2 for input-strap-filter relationships.

Table 2. Input Strapping.

INPUT	STRAP	FILTER
FL3 (A) (P1-15)	1-4	FL3 (A) (J10-4)
FL8 (P1-46)	8-6	FL8 (16 kHz)

**4.2 Filter Amplifier Gain Adjustments
(Adjustment of R6 and Selection of R49, R56, R94, and R97)**

- a. Set front panel MODE switch to SSB/CW and the BANDWIDTH switch to USB. Set AGC switch to FAST.
- b. Measure signal level at J1 with no receive input signal (9.9 MHz from Q5 mixer). Adjust R6 for a signal null at J1.
- c. Connect receive input of 9.4483 MHz to J2. Measure gain from J2 to J1. Should be ≈ 3 to 1. (Receive input must be set higher than 9.9-MHz leakage.)

Note

Perform step d only if FL1, Q8, and/or Q9 circuits have been repaired.

- d. Set receive signal to 50 μ V (9.4483 MHz). Find a passband response minimum between 9.4493 and 9.4489 MHz at J4. Measure voltage gain between J1 and J4. Should be 8.2 ± 2.0 dB. Select values of R94 and R97 (200 through 1000 Ω) to give a voltage gain of 8.2 ± 2.0 dB.
- e. Set front panel MODE switch to AM and the BANDWIDTH switch to 16.

Note

Perform step f only if Q6 and/or Q7 circuits have been repaired.

- f. Find a passband response minimum between 9.4493 and 9.4489 MHz at J4. Measure voltage gain between J1 and J4. Should be 8.2 ± 2.0 dB. Select values of R49 and R56 (200 through 1000 Ω) to give a voltage gain of 8.2 ± 2.0 dB.

4.3 Receive Gain Adjustment (Adjustment of C5, C8, L10, L13, R78, and R143)

- a. Set front panel MODE switch to SSB/CW and the BANDWIDTH switch to USB. Adjust R78 for minimum gain (full ccw). Increase receive input until AGC voltage (measured at P1-21) increases to about +1.0 V dc.
- b. Adjust C5, C8, L10, and L13 for a peak AGC voltage. Decrease the receive input as necessary to maintain AGC voltage at about +1.0 V dc.
- c. Repeat step b until no further increase in peak AGC voltage is possible.
- d. Set the receive input to 5.0 μ V (9.4483 MHz) and adjust R78 for +70 ± 5 mV dc AGC voltage (measured at P1-21).
- e. Increase receive input to 5.0 mV (9.4483 MHz) and adjust R143 until AGC voltage (measured at P1-21) equals +5.0 ± 0.1 V dc.
- f. Repeat steps d and e until no further improvement is possible.

4.4 SSB Output Level Adjustment (Adjustment of R262)

- a. Set front panel MODE switch to SSB/CW and the BANDWIDTH switch to USB.
- b. Set receive input for 15.0 μ V (9.4483 MHz) and adjust R262 for 10 ± 0.5 -mV rms audio output (measured at P1-34).

4.5 AGC Meter Level Adjustment (Adjustment of R132)

AGC meter level adjustment is made at the unit level for the level required by the associated meter circuit.

5. REPAIR

Repair of the channel A if card is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

This paragraph assists in identification, requisition, and issuance of parts and in maintenance of equipment. A parts location illustration, schematic

diagram, parts list tabulation, and modification history are included in the schematic diagram (figures 11 and 12). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

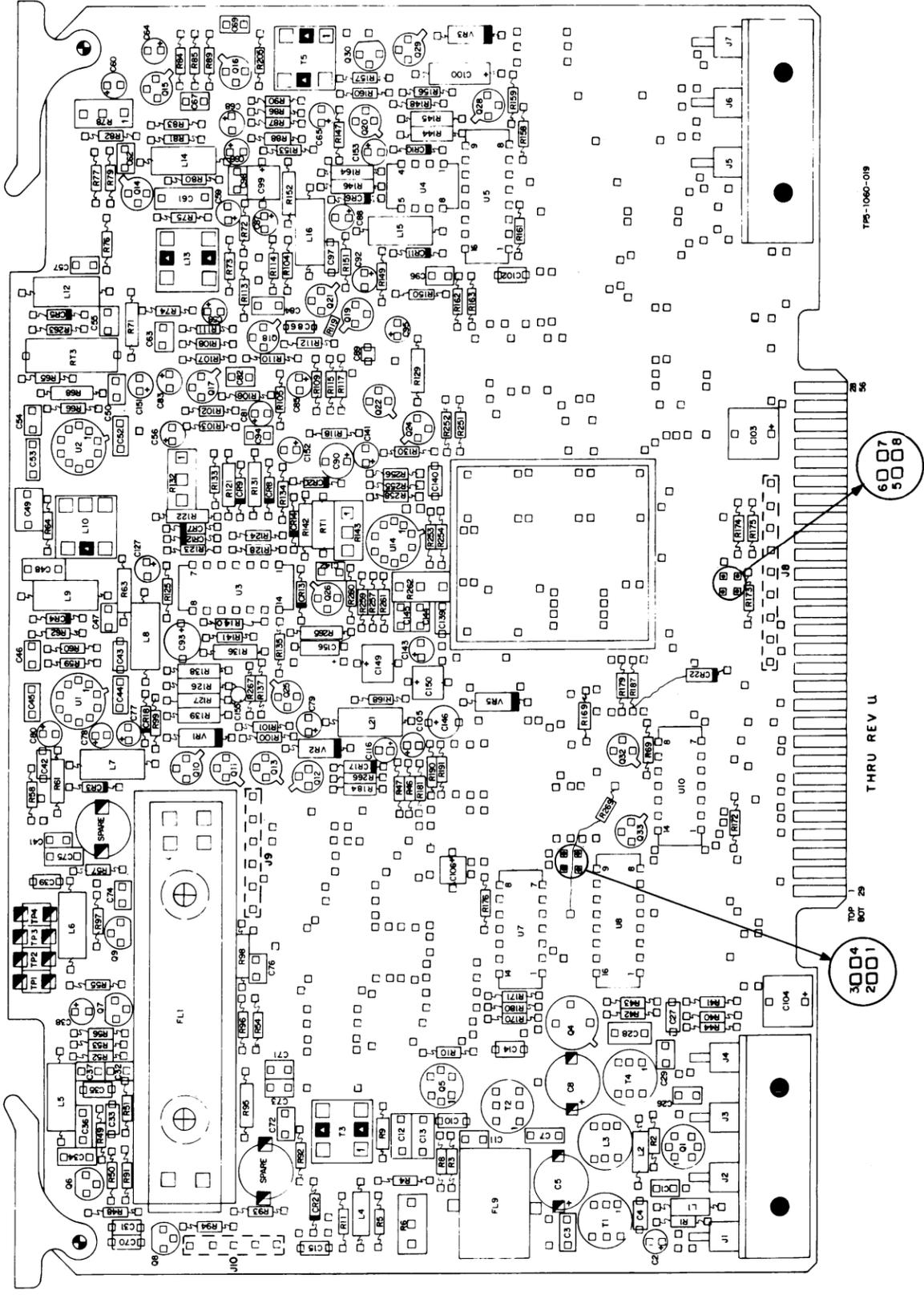
Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV)

stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

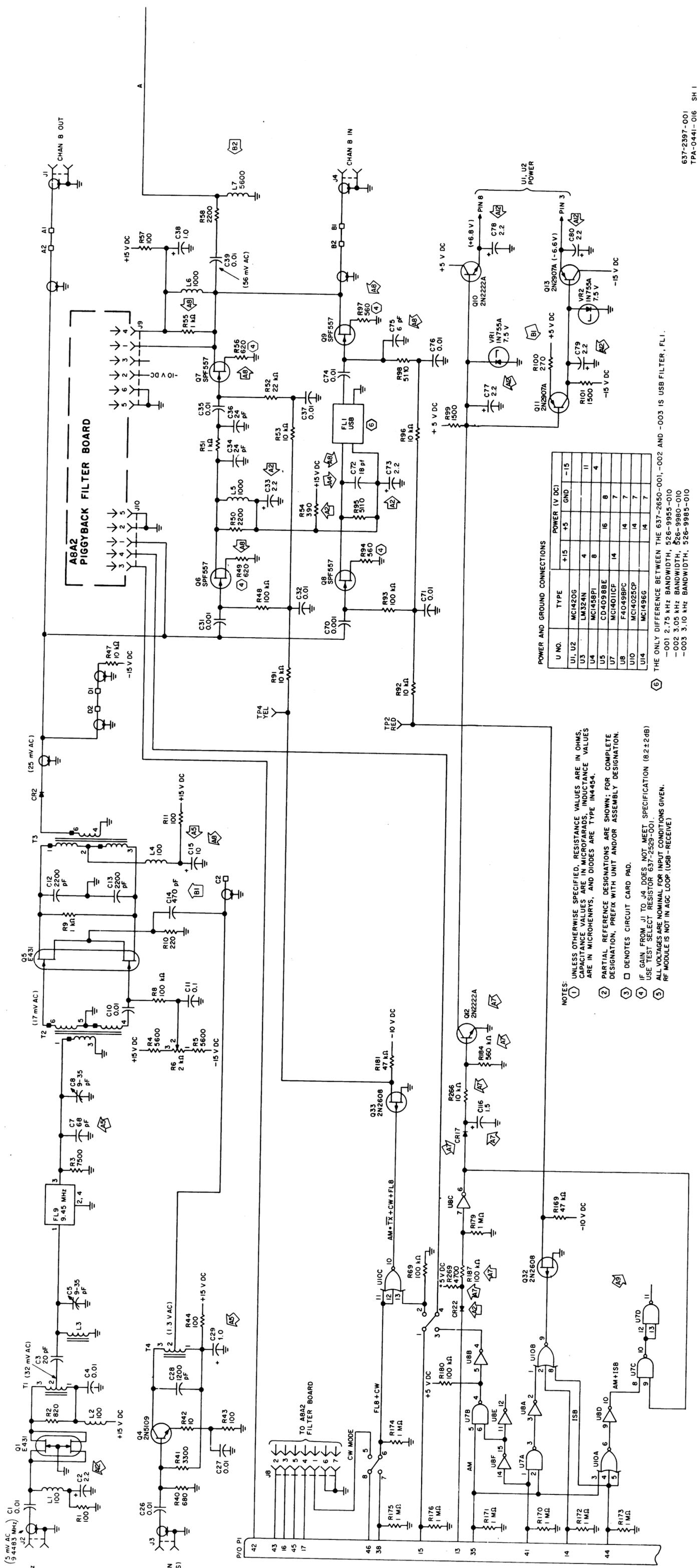
Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

<u>CIRCUIT CARD/ SUBASSEMBLY</u>	<u>COLLINS PART NUMBER</u>	<u>LATEST EFFECTIVITY</u>
Channel A if	637-2650-001	REV AD
Channel A if	637-2650-002	REV AD
Channel A if	637-2650-003	REV AC
Channel A if	637-2650-004	*
Channel A if	637-2650-005	*

*Not covered in this printing.



Channel A IF, Through REV AC, Schematic Diagram
Figure 11 (Sheet 1 of 5)



Channel A IF, Through REV A C, Schematic Diagram Figure 11 (Sheet 3)

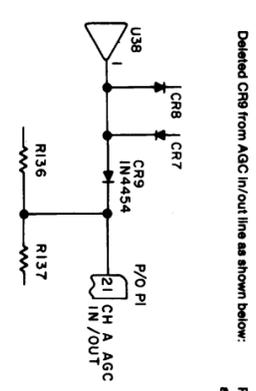
637-2397-001
TPA-0441-016 SH 1

PARTS LIST (Cont)

REF	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
R181	RESISTOR-FXD CHPSN, 47K, 10%, 1/8W	745-2401-000	
R182	NOT USED		
R183	RESISTOR-FXD CHPSN, 560K, 10%, 1/8W (A7)	745-2440-000	
R184	NOT USED		
R185	RESISTOR-FXD CHPSN, 100K, 10%, 1/8W (A7)	745-2413-000	
R186	NOT USED		
R187	RESISTOR-FXD CHPSN, 3.9K, 10%, 1/8W	745-2362-000	
R188	NOT USED		
R189	RESISTOR-FXD CHPSN, 22K, 10%, 1/8W (A9)	745-2389-000	
R190	NOT USED		
R191	RESISTOR-FXD CHPSN, 22 OHMS, 10%, 1/8W	745-2280-000	
R192	NOT USED		
R204	RESISTOR-FXD CHPSN, 1K, 10%, 1/8W	745-2341-000	
R205	NOT USED		
R206	RESISTOR-FXD CHPSN, 1K, 10%, 1/8W	745-2341-000	
R207	RESISTOR-FXD CHPSN, 220 OHMS, 10%, 1/8W	745-2338-000	
R208	RESISTOR-FXD CHPSN, 56 OHMS, 10%, 1/8W	745-2295-000	
R209	RESISTOR-FXD CHPSN, 100 OHMS, 10%, 1/8W	745-2304-000	
R210	RESISTOR-FXD CHPSN, 1K, 10%, 1/8W	745-2341-000	
R211	RESISTOR-FXD CHPSN, 1.3K, 5%, 1/8W	745-1863-520	
R212	RESISTOR-FXD CHPSN, 180 OHMS, 10%, 1/8W	745-2314-000	
R213	RESISTOR-FXD CHPSN, 3K, 5%, 1/8W	745-1863-400	
R214	RESISTOR-FXD CHPSN, 10K, 10%, 1/8W	745-2377-000	
R215	RESISTOR-FXD CHPSN, 10K, 10%, 1/8W	745-2341-000	
R216	RESISTOR-FXD CHPSN, 1K, 10%, 1/8W	745-2341-000	
R217	RESISTOR-FXD CHPSN, 1K, 10%, 1/8W	582-0052-440	
R218	RESISTOR-FXD CHPSN, 2.2K, 10%, 1/8W	745-2353-000	
R219	RESISTOR-FXD CHPSN, 100 OHMS, 10%, 1/8W	745-0713-000	
R220	RESISTOR-FXD CHPSN, 10K, 10%, 1/8W (A2)	745-2377-000	
R221	RESISTOR-FXD CHPSN, 330K, 5%, 1/8W (A2)	745-1864-130	
R222	RESISTOR-FXD CHPSN, 430K, 5%, 1/8W	745-1864-150	
R223	NOT USED		
R224	RESISTOR-FXD CHPSN, 4.7K, 10%, 1/8W (A7)	745-2345-000	
R225	RESISTOR-FXD CHPSN, 10K, 10%, 1/8W	340-0484-020	
R226	JACK, TIP ORN	360-0484-020	
R227	JACK, TIP RED	360-0484-050	
R228	JACK, TIP YEL	360-0484-060	
R229	TRANSFORMER, RF	278-0430-180	
R230	TRANSFORMER, RF	278-0430-180	
R231	TRANSFORMER, RF	278-0432-010	
R232	TRANSFORMER, RF	278-0432-010	
R233	TRANSFORMER, RF	278-0432-030	
R234	TRANSFORMER, RF	278-0432-030	
R235	TRANSFORMER, RF	351-1050-030	
R236	TRANSFORMER, RF	351-1141-030	
R237	TRANSFORMER, RF	351-1071-070	
R238	TRANSFORMER, RF	351-0278-010	
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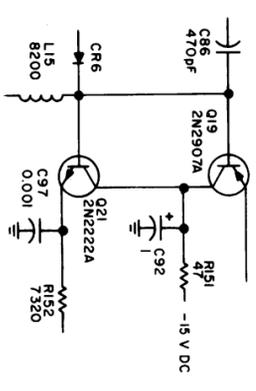
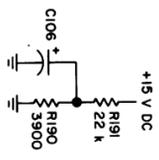
MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Deleted CR8 from AGC in/out line as shown below:	REV E and above



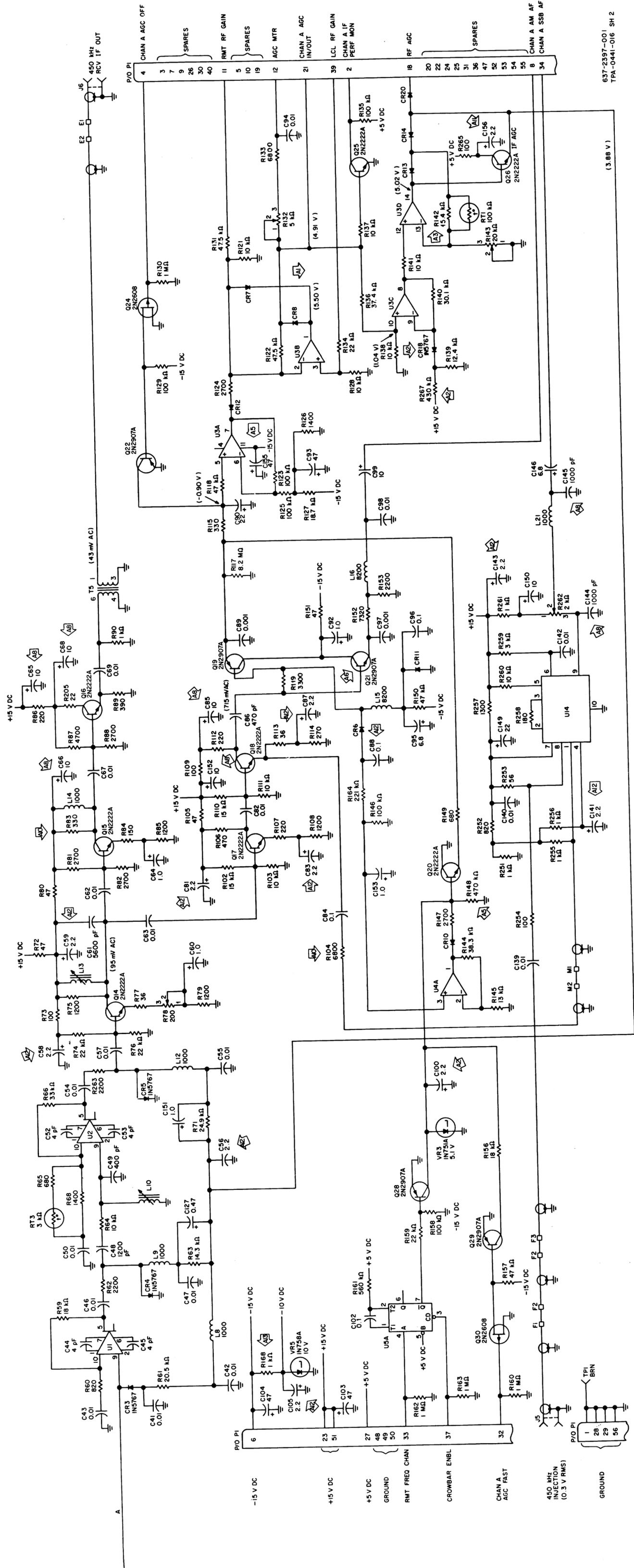
MODIFICATION HISTORY (Cont)

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A2	Added CR22, 1N4454.	REV E and above
A3	Changed: CR18 from 1N616 to 1N5767. CR23 from 0.01µF to 2.2µF. CR29 from 0.01µF to 2.2µF. CR78 from 4.7µF to 22µF. CR100 from 1KΩ to 380Ω. R54 from 1KΩ to 380Ω. R267 from 300KΩ, 10% to 430KΩ, 5%. Changed R142 from 22.8KΩ to 15.4KΩ.	REV F and above
A4	Removed CR2, 150F from across R95 (input to FL, USB filter).	REV G and above
A5	Added CR155, 47µF electrolytic.	REV G and above
A6	Changed: CR7 from 47F to 889F. CR15 from 0.01µF ceramic to 1.0µF electrolytic. CR29 from 0.01µF to 1.0µF. CR78 from 0.01µF to 470KΩ. R148 from 270KΩ to 470KΩ.	REV G and above
A7	Added CR17, 1N4454. Added CR18, 1.5µH. Added CR12, 2N2222A. Added R184, 580KΩ. Added R187, 100KΩ. Added R286, 10KΩ. Added R288, 4700Ω.	REV H and above
A8	Added CR2, 18pF.	REV K and above
A9	Removed CR106, 8.8µF; R190, 3800Ω, and R191, 22KΩ from circuit as shown below:	REV K and above
A10	Changed: R83 from 470Ω to 390Ω. R85 from 10KΩ to 6800Ω.	REV N and above
A11	Added C156, 2.2µF electrolytic.	REV P and above
A12	Changed: CR2 from 0.1µF to 2.2µF. CR8 from 0.1µF to 2.2µF. CR89 from 0.1µF to 2.2µF. CR98 from 0.1µF to 2.2µF. CR77 from 0.1µF to 2.2µF. CR78 from 0.1µF to 2.2µF. CR79 from 0.1µF to 2.2µF. CR80 from 0.1µF to 2.2µF. CR81 from 0.1µF to 2.2µF. CR83 from 0.1µF to 2.2µF. CR87 from 0.1µF to 2.2µF. CR88 from 0.1µF to 2.2µF. CR89 from 0.1µF to 2.2µF. CR98 from 0.1µF to 2.2µF. CR105 from 0.1µF to 2.2µF. CR141 from 0.1µF to 2.2µF. CR143 from 0.1µF to 2.2µF.	REV R and above
A13	Changed R188 from 2200Ω to 1KΩ.	REV T and above
B1	Changed: C14 from 0.01µF to 470pF. R100 from 470Ω to 270Ω.	REV AA and above
B2	Changed L7 from 2700µH to 5800µH.	REV AC and above



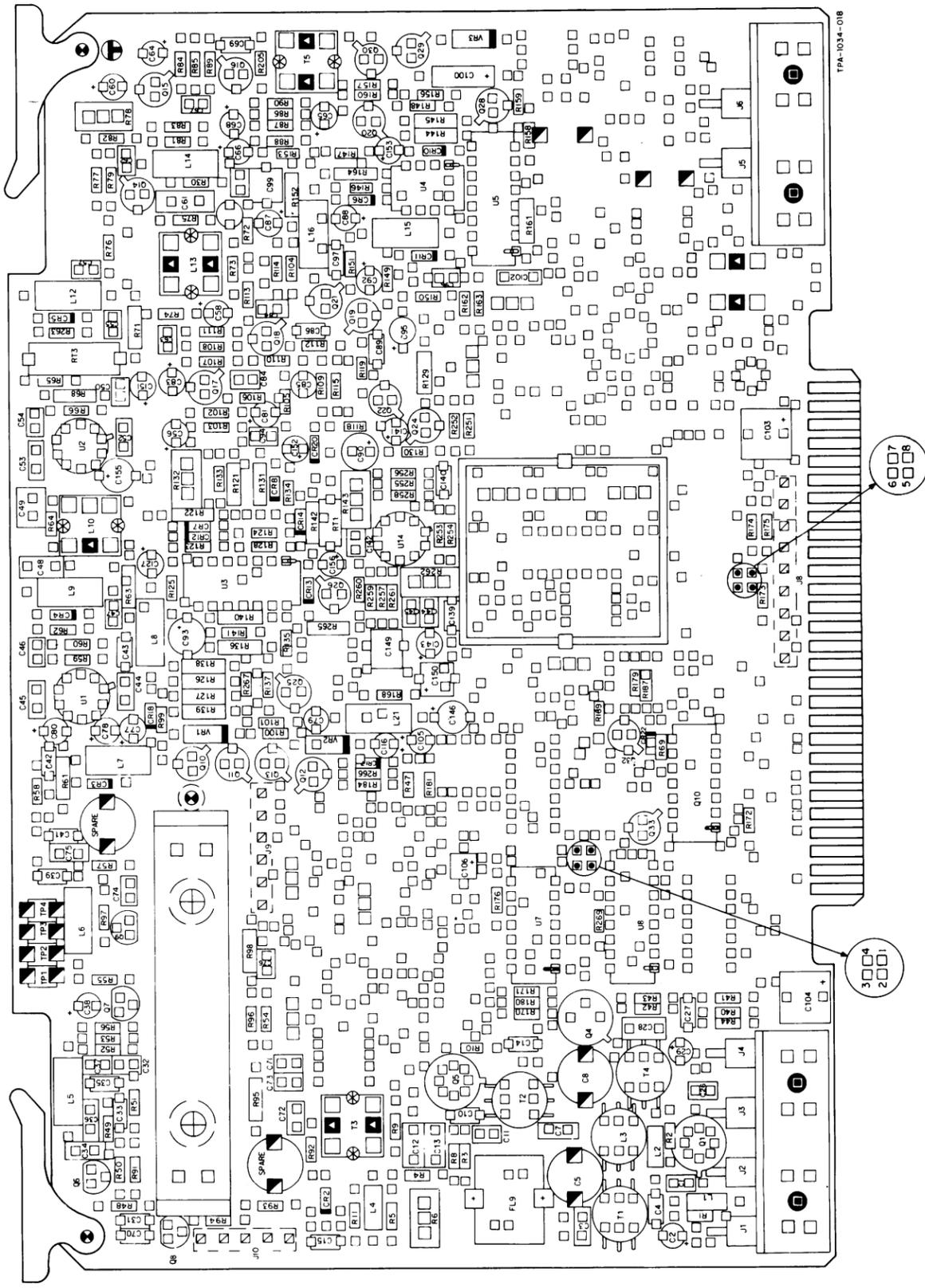
Changed:
 C15 from 1.0µF to 10µF.
 C85 from 1.0µF to 10µF.
 C88 from 0.1µF to 10µF.
 C88 from 1.0µF to 10µF.

Channel A IF Through REV A.C. Schematic Diagram
 Figure 11 (Sheet 4)

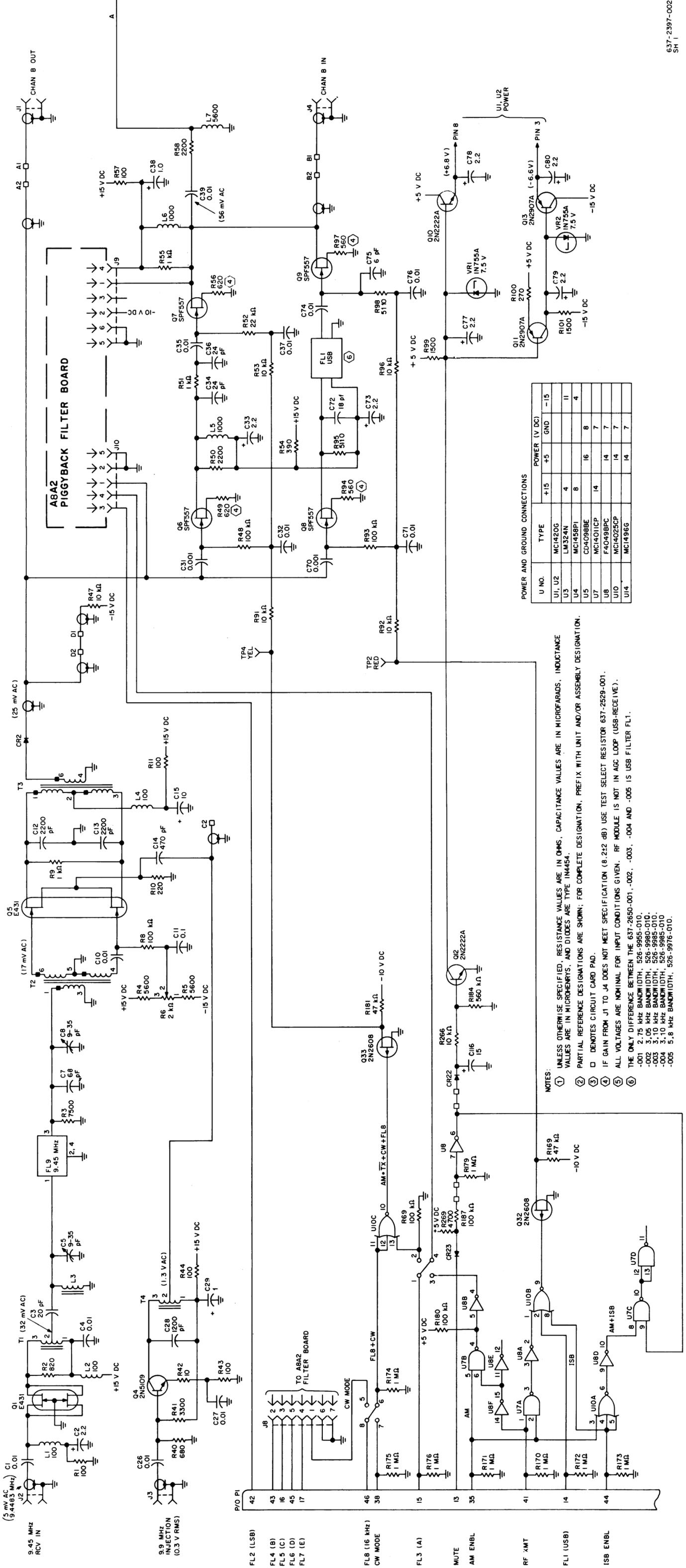


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Channel A IF Throughput REV AC Schematic Diagram
Figure 11 (Sheet 5)



Channel A IF, REV AD and Above, Schematic Diagram
Figure 12 (Sheet 1 of 5)



Channel A IF, REV A.D and Above, Schematic Diagram
Figure 12 (Sheet 3)

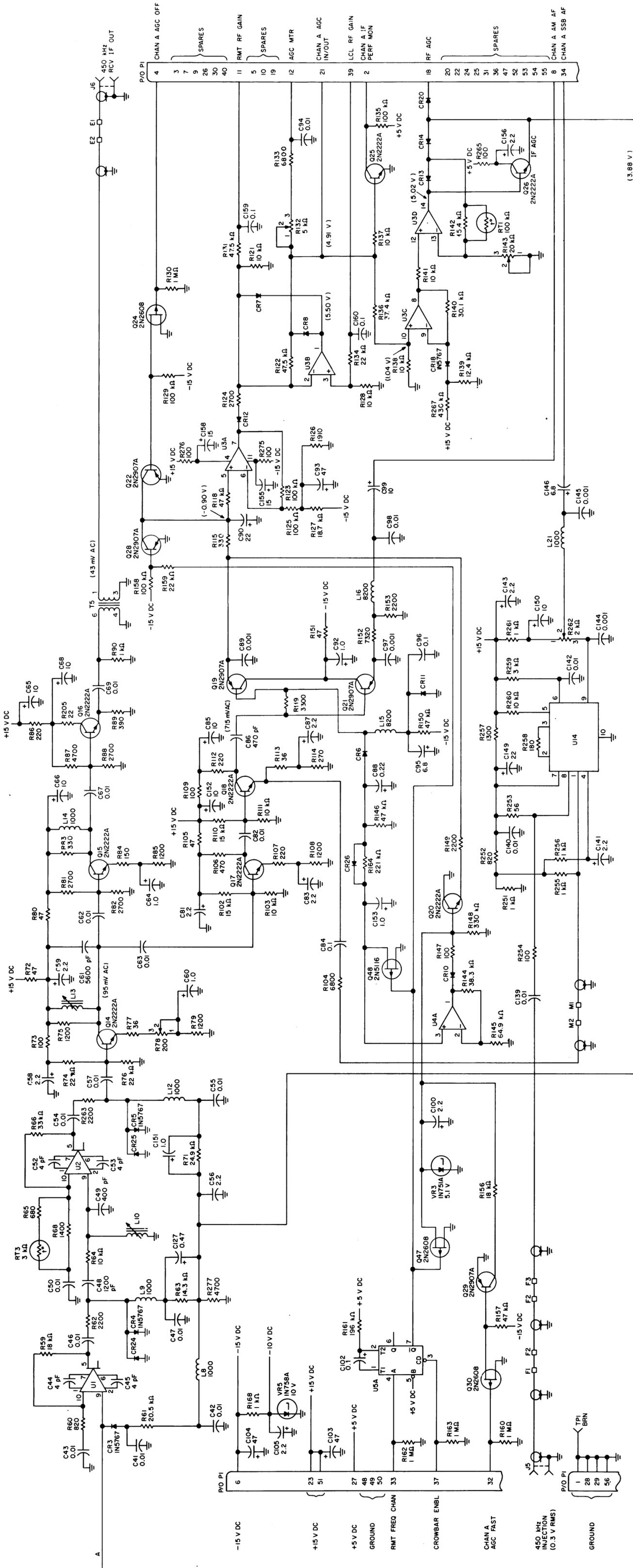
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
U4	INTEGRATED CIR IC14986	351-1071-070	
U5	INTEGRATED CIR CD40988E	351-2278-010	
U6	NOT USED	351-2159-040	
U7	INTEGRATED CIR CD40116	351-2159-210	
U8	INTEGRATED CIR CD4047A	351-2159-210	
U9	NOT USED		
U10	INTEGRATED CIR CD4025A	351-2159-150	
U11-U13	NOT USED		
U14	INTEGRATED CIR IC14986	351-0043-020	
VR1,VR2	SEMICONV DEVICE JN751A	353-2718-000	
VR3	SEMICONV DEVICE JN751A	353-2718-000	
VR4	NOT USED		
VR5	SEMICONV DEVICE JN754A	353-2724-000	
R49,R50	RESISTOR FROD/CPNSN, 2000HM THRU 1K, 5%, 1/8W	637-2529-001	
R59,R59	(TEST SELECT)		

MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
None	None	AD and above
	For configuration before REV AD, refer to figure 10.	
	Changed layout of base planar board.	
	Deleted C117, 1N4454 R117, 8.2 M Ω	
	Changed C98 from 0.1 μ F to 0.22 μ F C155 from 47 μ F to 15 μ F R128 from 1400 Ω to 1910 Ω R145 from 13k Ω to 64.9k Ω R146 from 100k Ω to 47k Ω R147 from 2700 Ω to 100 Ω R148 from 470k Ω to 390k Ω R149 from 680 Ω to 220 Ω	
	Added CR23, 1N4454 CR24, 1N4454 CR25, 1N4454 CR26, 1N4454 C156, 15 μ F electrolytic C160, 0.1 μ F C162, 0.1 μ F R276, 100 Ω R278, 100 Ω R277, 4700 Ω Q47, 2N2808 Q48, 2N5116	

Channel A IF, REV AD and Above, Schematic Diagram
Figure 12 (Sheet 4)



Channel A IF, REV AD and Above, Schematic Diagram Figure 12 (Sheet 5)